# 〈論文〉 4-2-5

# 인버터 에어컨을 위한 고역률 단상능동정류기

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# High Power Factor Single-Phase Active Rectifier for Inverter Air-Conditioner

Yong-Chae Jung and Kyung-Ahn Kwon

요 약

본 논문에서는 IEC 61000-3-2와 같은 고조파 전류 국제규제에 만족하기 위해서 인버터 에어컨을 위한 고역률 단상능동정류기 (SAR)[4-6]를 적용하였다. 입력전류의 왜곡을 최소화하고 FA5331, UC3854, ML4821 등과 같은 제어IC를 적용하기 위해서 입력전압 및 전류에 대한 새롭고 적절한 검출회로를 제안하였다. 효율 및 가격의 관점에서 SAR를 인버터 에어컨에 적용하기 위한 두가지 방법이 있다. 이런 두가지 방식에 대해서 수동소자의 선정방법을 제시하였다. 결정된 소자들을 사용하여 SAR 효율의 증가 여부를 확인하기 위해서 손실분석을 행하였다. 3kW급의 이러한 두가지 방식에 대한 프로트형 SAR회로를 제작하고 실험결과를 통해서 역률제어능력을 갖는 회로의 동작과 성능을 확인하였다.

#### **ABSTRACT**

In this paper, the high power factor Single-phase Active Rectifier (SAR) <sup>14-6</sup> for inverter air-conditioner is adopted to satisfy the international harmonic current standards such as IEC 61000-3-2. To minimize the input current distortion and to apply the control ICs, such as FA5331, UC3854, ML4821 and so forth, the new adequate sensing circuits of the input voltage and current are proposed. There are two methods applicable the SAR to inverter air-conditioner from the viewpoints of efficiency and cost. The selecting methods of the passive components are presented for the two approaches. Using the determined components, the loss analyses are carried out in order to ascertain whether the efficiency of the SAR is enhanced. The proto-type SAR circuits of these two approaches with 3kW power consumption are built and the operation and performance of the circuits with power factor correction capability are verified through the experimental results.

Key Words: High power factor, Single-phase active rectifier, Inverter air-conditioner

## 1. Introduction

Recently, the international activities for energy saving have been intensively executed. To keep in step with this trend, the adoption of the inverter technology has been extensively expanded in the home appliance, such as airconditioner, refrigerator, washing machine and so on.

However, because they operate by rectifying the

input ac line voltage and filtering it with large electrolytic capacitor, the input current has poor power factor and rich harmonics. Although the power factor of the conventional inverter air conditioner can be improved about 0.9 using the LC passive filter, input current harmonics do not meet the forthcoming international standard, IEC 61000-3-2. Both to satisfy this harmonic regulation and to improve the inverter

performance through the stabilization of the DC link voltage, it is a trend to add the power factor correction circuit to the conventional inverter air-conditioner.

Several topologies are available for the power factor correction and the harmonic current reduction. Among them, the most popular topology is the boost circuit [1-3]. Although the boost topology has the enhanced performance, the total efficiency becomes lower because the main current always flows through three semiconductor devices.

Thus, in this paper, a Single-phase Active Rectifier (SAR)[4~6] with high power factor capability for the inverter air-conditioner is adopted to satisfy the international standards of input current harmonics, IEC 61000-3-2. Comparing the conventional boost power factor correction circuit, one diode drop is reduced in the power flow path of the SAR topology, so the system efficiency can be improved. In this case, there are two approaches in order to apply the SAR to the inverter air-conditioner fed from single-phase ac source. One is the high efficiency approach and the other is the low cost approach, respectively. In the former case, the switching frequencies of the abovementioned two topologies (SAR and Boost) are equalized. On the other hand, in the low cost approach, the switching frequency of the SAR is increased to reduce the additional cost in the latter and thereby the each size of choke inductor and filter components can be reduced.

To minimize the input current distortion, we propose the new detecting circuits of the input voltage and current. The selecting methods of the passive components are presented. Using the designed components, the loss analyses are performed. The

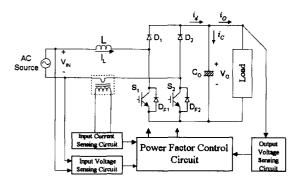


Fig. 1 The single-phase active rectifier with the control block diagram

proto-type SAR circuits of these two approaches with 3kW power consumption are built and tested to verify the operation and performance of the circuits with power factor correction capability.

#### 2. Operational Principle

Fig. 1 shows the single-phase active rectifier and the control block diagram. As can be seen in the reference 14561, according to the input voltage polarity, the power factor correction is attained by  $S_1$ ,  $D_1$ , and  $D_{P2}$  for the positive value and  $S_2$ ,  $D_2$ , and  $D_{F1}$  for the negative value, respectively.

First of all, consider the case that the input voltage is positive. If  $S_1$  is turned on as shown in Fig. 2 (a), the input voltage  $V_{\mbox{\scriptsize IN}}$  appears across the choke inductor L through  $V_{IN}$ -L- $S_1$ - $D_{F2}$  path and the inductor current IL increases linearly with the positive slope of V<sub>IN</sub>/L. At the same time, the output capacitor is discharged to the load. If S<sub>1</sub> is turned off by the control signal as shown in Fig. 2 (b), the difference voltage (V<sub>O</sub>-V<sub>IN</sub>) is applied in the opposite direction across the choke inductor L through  $V_{IN}$ -L- $D_1$ - $C_O$ - $D_{F2}$  path and the inductor current I<sub>L</sub> decreases linearly with negative slope of  $(V_0 - V_{IN})/L$ . In this case, the output capacitor is charged through the choke inductor.

When the input voltage is negative, the similar operations are achieved by  $S_2$ ,  $D_2$ , and  $D_{F1}$  as shown in Fig. 2 (c) and (d).

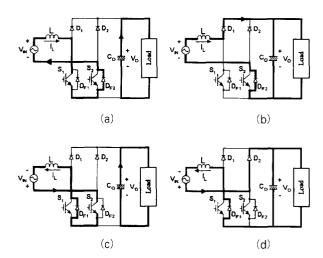


Fig. 2 The operational modes of the SAR

### 3. The Proposed Sensing Circuit

The proper sensing circuits, such as input current, input voltage and output voltage, are indispensable for raising the power factor correction performance. As can be seen in Fig. 3, the input voltage sensing circuit referred to 66 has a severe problem. When the input voltage is negative and the switch S2 is turned on as shown in Fig. 3(a), V<sub>a</sub> becomes zero and V<sub>b</sub> has the negative value. The sensing voltage  $\boldsymbol{V}_{\!\scriptscriptstyle{sen}}$  is also to be zero. In the circuit, if there is no the series resistor R<sub>o</sub>, the circuit is shorted through the path,  $V_{\mbox{\tiny IN}}\mbox{-}S_2\mbox{-}D_{\mbox{\tiny UR}}\mbox{, and}$ damaged seriously. Therefore, the resistor is in dispensable to the sensing circuit. When the switch  $\boldsymbol{S}_{\!\scriptscriptstyle 2}$ is turned off, the sensing voltage V<sub>sen</sub> increases from zero to DC output voltage, V<sub>O</sub>, through the path of Fig. 3 (b). On the other hand, when the input voltage is positive, it is nicely detected on account of conducting the diode D<sub>F2</sub> at all times. Thus, the sensing voltage Vsen is to be the periodic distorted waveform as shown in Fig. 4.

To resolve the problem, we interpose the voltage

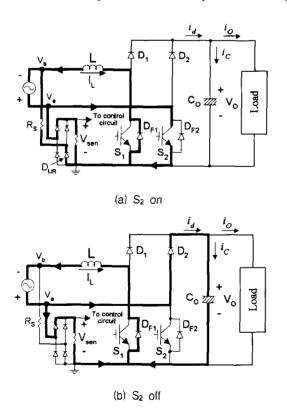


Fig. 3 The sensing paths of the input voltage sensing circuit referred to (6)

transformer between the ac input line and the diode bridge as depicted in Fig. 5 (a). In the circuit, the minimum valley voltage of the sensing value floats on the ground, then we insert the high frequency RC filter with the 1.2kHz cut-off frequency.

Fig. 5 (b) shows the input current sensing circuit composed of current transformer (CT), offset resistors  $(R_{rs1}, R_{rs2})$ , diode bridge and sensing resistor  $(R_{sen})$ . To transmit favorably the high frequency sensing information, the turn ratio

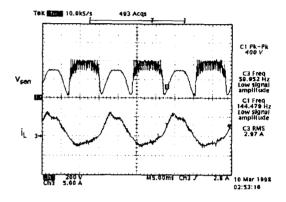
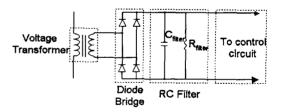
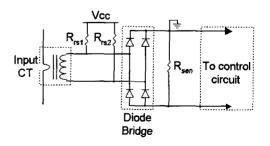


Fig. 4 The experimental waveforms in the case of Fig.3



(a) Input voltage sensing circuit



(b) Input current sensing circuit

Fig. 5 The proposed sensing circuits

of the CT should be sufficiently enlarged. When the input current is low, the sensing voltage has some noises due to the forward recovery phenomenon of the bridge diode. To reduce the problem, the upper two diodes of the bridge are turned on in advance using the offset resistors. Its are twofold roles. One is to remove the noise components of the sensing voltage and the other is to force the SAR circuit to operate with maximum duty when the input voltage is in the vicinity of zero cross. The currents flowing through the offset resistors are constant as  $(V_{\text{cc}} {-} V_{\text{d}})/R_{\text{rs1}}$  and  $(V_{\text{cc}} {-}$  $V_d)/R_{rs2}$  where  $V_d$  is the on-voltage of diode. These

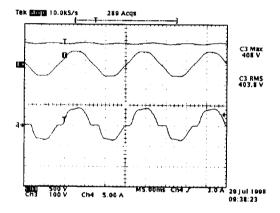


Fig. 6 The experimental waveforms without the offset resistors (upper: output voltage, middle: input voltage, lower: input current)

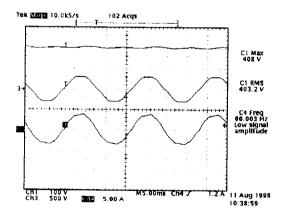


Fig. 7 The experimental waveforms with the offset resistors (upper: output voltage, middle: input voltage, lower:input current)

currents are somewhat arbitrarily selected to about 1mA. To ascertain the effect of the offset resistors, Fig. 6 and 7 show the experimental results without and with these resistors. respectively. As can be seen in Fig. 7, the crossover distortion of the input current has been dramatically reduced.

## 4. The Selection Method of The Passive Components

1) Choke Inductor : To select the choke inductor. the peak inductor current  $(I_{nk})$  should be calculated. This current can be expressed by:

$$I_{pk} = \sqrt{2} P_{lN} / V_{lN \min} + \Delta I / 2 \tag{1}$$

where  $P_{\mbox{\tiny IN}}$  is the input power,  $V_{\mbox{\tiny IN,min}}$  is the minimum input voltage and  $\Delta I$  is the ripple current of the choke inductor. In this equation, the first term means the maximum rms input current. At the condition of (1), that is, the peak value of the minimum input voltage, the duty D can be calculated as follows:

$$D = \frac{V_o - V_{IN,\min}(peak)}{V_o} \tag{2}$$

In this case, the inductance of the choke inductor can be determined by the following equation.

$$L = \frac{V_{lN,\min}(peak) \times D}{\Delta I \times f_s}$$
 (3)

2) Output Capacitor: To obtain the appropriate output capacitor, it is necessary to know both the permissible ripple current capability and the capacitance of the output electrolytic capacitor in advance. Although there is a somewhat difference for a motor load, to regard this result as a guide, we assume the load is resistive. In this case, the rms value of the load current  $i_o$  as shown in Fig. 8 is expressed by

$$I_{o,rms} = \frac{P_{IN} \cdot \eta_{PFC}}{V} \tag{4}$$

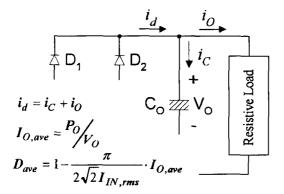


Fig. 8 Some notations and the related equations to calculate the capacitor ripple current

where  $\eta_{\rm PFC}$  is the efficiency of the SAR circuit. The diode current is calculated as follows :

$$I_{d.rms} = \frac{P_{IN}}{V_{IN.min}} \cdot \sqrt{1 - D_{ave}}$$
 (5)

where  $D_{av}$  as expressed in the next equation is the average duty ratio of the switch for a period of 120Hz.

$$D_{ave} = 1 - \frac{\pi}{2} \cdot \frac{I_{o,rms}}{\sqrt{2}I_{D,rms}} \tag{6}$$

In this equation,  $I_{N,ms}$  is the rms value of the input current. Thus, using the above equations, the permissible ripple current of the capacitor can be obtained by the following equation.

$$I_{c,rms} = \sqrt{I_{d,rms}^2 - I_{o,rms}^2} \tag{7}$$

In this case, the required capacitance should be satisfied with the following condition.

$$C = \frac{I_{c.rms}}{\omega \cdot \Delta V} \tag{8}$$

where  $\omega$  is the angular frequency of the rectified voltage and  $\Delta V$  is the permissible output ripple voltage as can be expressed as follows:

$$\Delta V = \frac{\% ripple \times V_o}{2\sqrt{2}} \tag{9}$$

where *%ripple* is the ripple percentage defined by the user.

#### 5. Loss Analysis

To verify the high efficiency property of the SAR, we perform the loss analysis in this section. IGBT and diode losses can be calculated by a manufacturer specified model that includes an offset voltage in series with a resistance. Each loss equation can be expressed as follows.

$$P_{BD} = I_{IN,cons} \cdot V_F \cdot 2 = \frac{P_{IN}}{V_{IN}} \cdot V_F \cdot 2$$

$$(\text{Bridge diode loss}) \qquad (10)$$

$$P_{off} = \sum_{n=1}^{T_{IN}/T_{sw}} \frac{i_{C,n}^2 \cdot t_{off}^2}{48 \cdot C_o}$$

$$(\text{Turn-off switching loss}) \qquad (11)$$

$$P_{con,sw} = \frac{1}{T_{IN}} \int_0^{T_{IN}} \left( V_{o,sw} + R_{s,sw} \cdot i_C \right) \cdot i_C dt$$

$$(\text{Switch conduction loss}) \qquad (12)$$

$$P_{con,d} = \frac{1}{T_{IN}} \int_0^{T_{IN}} \left( V_{o,d} + R_{s,d} \cdot i_d \right) \cdot i_d dt$$

$$(\text{Diode conduction loss}) \qquad (13)$$

$$P_L = \frac{1}{T_{IN}} \int_0^{T_{IN}} i_L^2 \cdot R_L dt$$

$$(\text{Choke inductor ESR loss}) \qquad (14)$$

where  $V_F$  is the diode forward voltage,  $T_{NV}$  and  $T_{NV}$  are periods of the rectified voltage and the switching frequency,  $i_{C}$ ,  $t_{\mathrm{eff}}$  and  $C_{\mathrm{o}}$  are the collector current, the turn-off time and the output capacitance of the switch,  $V_{O,\infty}$  in series with  $R_{s,\infty}$  are the manufacturer specified model of the switch,  $V_{\mathcal{O},d}$  in series with  $R_{\mathbf{x},d}$ are the manufacturer specified model of the diode and  $i_t$  and  $R_t$  are the inductor current and the effective series resistance of the choke inductor, respectively. Table 1 shows the calculated losses through the computer simulation using the above equations assuming that the turn-off loss and the turn-on loss of the switch are the same. Moreover, Fig. 9 shows the experimental results for the comparison between the SAR and the boost topologies. As can be seen in these table and figure, the efficiency of the SAR is about 0.5% greater than one of the boost. Therefore, to attain the low cost approach, the switching frequency can be increased to 40kHz with the similar efficiency. In this case, since the each size of the choke inductor

Table 1 The calculated losses for two topologies

	Boost	SAR
Choke Inductor ESR Loss	12.62[W]	12.62[W]
Switch Conduction Loss	23.7[W]	23.7[W]
Switch Switching Loss	15.35[W]	15.35[W]
Total Switch Loss	39.05[W]	31.53[W]
Diode Loss	8.66[W]	8.66[W]
Bridge Diode Loss	36.7[W]	
Total Loss	97.03[W]	84.34[W]
Efficiency	96.8[%]	97.2[%]

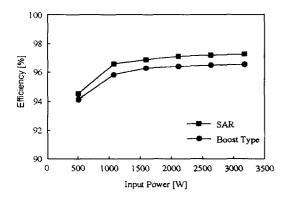


Fig. 9 Efficiencies according to the input powers by the test

and the filter components can be reduced, the cost can be cut down.

### 6. Experimental Results

To verify the above mentioned operation and to assure the performance of the power factor correction, the proto-type SAR circuits with operation at the 25kHz and 40kHz switching frequency are manufactured and tested with the experimental conditions as shown in Table 2, choke inductor. The safe operation up to 30(A) has been ensured as shown in this figure. Fig. 11 shows the experimental waveforms at the rated power for these two SAR circuits. In this case, to illustrate the performance of these two circuits, it is necessary to compare some characteristics such as power factor and THD. Fig. 12 shows the calculated limits and test results for the 25kHz SAR according to the

Table 2 The experimental conditions

	High Efficiency SAR	Low Cost SAR
Switching Frequency	25[kHz]	40[kHz]
Choke inductance	530[ µ H] / 30[A]	354[ µ H] / 30[A]
Output Capacitance	680[ µ F] / 450[V]	680[µF]/450[ <b>\]</b>
Output Voltage	400[√]	400[V]
Input Power	220[V] / 3[kW]	220[V] / 3[kW]
Average Duty	0.5	0.5

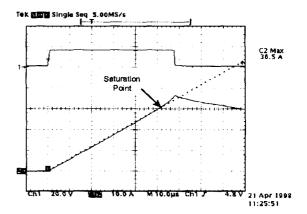


Fig. 10 The saturation test of the choke inductor

input power. In these figures, assuming that the displacement power factor(DPF) is unity, the calculated limits has been yielded as following two equations:

$$THD_{i} = \frac{\sqrt{I_{2}^{2} + I_{3}^{2} + \dots + I_{39}^{2} + I_{40}^{2}}}{I_{1}} \times 100$$

$$= \frac{3.041871}{P_{IN} / V_{IN}} \times 100$$

$$PF = \frac{1}{\sqrt{1 + (THD_{i} / 100)^{2}}}$$
(16)

where the constant, 3.041871, is the calculated value from the regulation limits of harmonic currents specified in international standard, IEC 61000-3-2.

Fig. 13 and Fig. 14 show the performances of the proposed circuits such as power factor and total harmonic distortion. As can be seen in these two figures, they have been thoroughly satisfied with the abovementioned international standard.

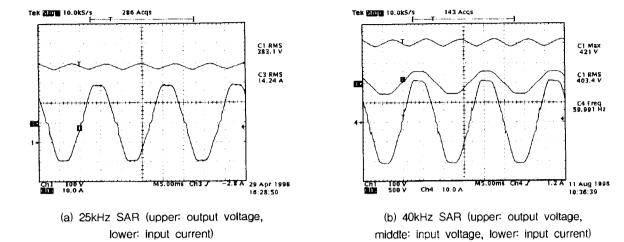


Fig. 11 The experimental results at the rated power for the two SAR circuits

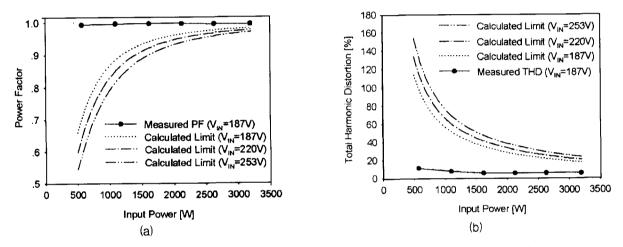


Fig. 12 Calculated limits according to the input power (Measured data : 25kHz SAR)

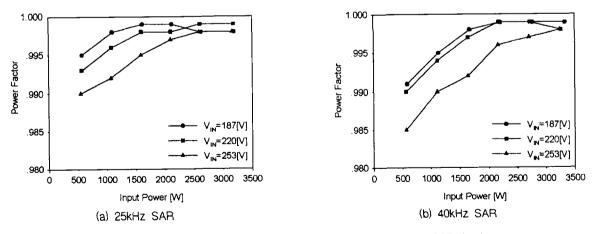
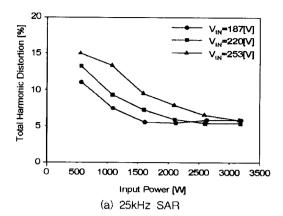


Fig. 13 The power factor according to the input power for the two SAR citcuits



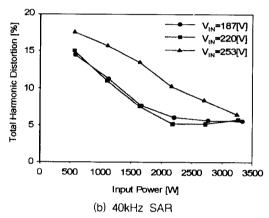


Fig. 14 The total harmonic distortion according to the input power for the two SAR citcuits

#### 7. Conclusion

In this paper, to meet the international standard of the input current harmonics for the inverter air-conditioner system, we adopt the single-phase active rectifier. 4 6. with high power factor capability. The new proper sensing circuits of the input voltage and current are proposed to reduce the input current distortion and to apply the available control ICs, such as FA5331. UC3854, ML4821 and so on. Also, we present the design methods of the passive components. Using the designed components, the loss analyses are performed. As a result, it has been established that the efficiency of the SAR topology is better than that of the conventional boost circuit. To ascertain the operation and performance of the two circuits, the proto-type SAR circuits operating at the 25kHz and 40kHz switching frequencies have been built and tested. Through the experimental results,

we have verified the capability of both the high efficiency approach and the low cost approach of the SAR topology.

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#### 자 \_소 개〉



#### 정용채(鄭龍采)

1966년 2월 28일생. 1989년 2월 한양대학교 전자공학과 졸업. 1991년 2월 한국과학기술원 전기 및 전자공학과 졸업 (석사), 1995년 8월 한 국과학기술원 전기 및 전자공학과 졸업 (공박). 1995년 - 현재 LG전자 홈 어플라이언스연구소

전력전자팀 선임연구원



#### 권경안(權京顏)

1962년 8월 22일생. 1985년 2월 연세대학교 전자공학과 졸업. 1997년 8월 동 대학원 전자공 학과 졸업 (석사). 1985년-1988년 삼성전자 종 합연구소. 현재 LG전자 홈 어플라이언스연구소 전력전자팀 책임연구원.