SRM 구동을 위한 새로운 ZVT-PWM 컨버어터

論 文
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Novel Zero Voltage Transition PWM Converter for Switched Reluctance Motor Drives

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Abstract - A novel zero-voltage-transition (ZVT) PWM converter for switched reluctance motor (SRM) drives is proposed. A simple auxiliary circuit which consists of one active switch, one resonant inductor, and three diodes provides ZVS condition to all main switches and diodes allowing high frequency operation of the converter with high efficiency. The auxiliary circuit is placed in parallel with the main power flow path and thus it handles only a small fraction of the main power. So, the power rating of the auxiliary circuit can be very small (about 30% of main power). So, the auxiliary circuit can be realized with small power rating and low cost. Operation, features and characteristics of the proposed converter are illustrated and verified on a 1.5 kW, 50 kHz IGBT based (a MOSFET for the auxiliary switch) experimental circuit.

Key Words : SRM, ZVT, PWM, Resonant

1. Introduction

Due to simple and rugged motor construction, high motor speeds, high torque-to-inertia ratio, and robust drive, SRM drives have received considerable attention for last decade[1-5]. Many converter topologies for SRM drives have been presented[1-5]. One of most popular converter topology is two switches per phase converter[1,2], referred to *2n*-converter, which has high and independent current control capability and low device voltage stress. One drawback is that too many switches are required, which increases the cost of drive system. A simpler circuit having most of advantages of the *2n*-converter is one and a half switches per phase converter[1], referred to *2(n-1)*-converter. This scheme is only for even number of phase machines. The number of switches, however, are optimized without losing current control capabilities such as fast commutation and current overlap.

With the increased demand for high performance and low audible noise, it is inevitable to increase the switching frequencies. Operating at high frequency with hard switching PWM converters is limited because of the substantial increase of switching loss. To reduce switching loss, soft switching technologies have been studied for many years in the field of switching converters and inverters. To date, a number of soft switching converters have been presented however most of them reduce switching loss only at the expense of much increased voltage and/or current stresses of the switches, which leads to a substantial increase in conduction loss. Recently, a new family of ZVT PWM converters were presented by adding a simple ZVT sub-circuit to hard switching PWM converters[6,7]. These converters have been widely used in the industry because of their distinctive advantages including simple circuit topology, wide ZVS range, and minimum device voltage and current stresses. For SRM drive circuit, however, a few soft switching converters have been presented.

A ZVT PWM converter for SRM drives was presented [5] (see Fig. 1). To achieve ZVT operation, a chopper with ZVT sub-circuit is added in series with the main power flow path. The chopper switch is operated with ZVS to control the phase current while the main switches in the 2(n-1)-converter part are operated only for selecting a phase. The switching loss can be reduced considerably thanks to ZVS and very slow switches can be used for the main switches since no choppings in the main switches occurs. The additional switch added in series with power flow path, however, increases the conduction loss and cost.

In this study, a novel ZVT PWM converter for SRM drives is presented. A simple ZVT sub-circuit[7] is added in parallel with the main power flow path without changing the original hard switching converter as shown in Fig. 2. The ZVS of the main switches are achieved without increasing conduction loss and device voltage and current stresses. The

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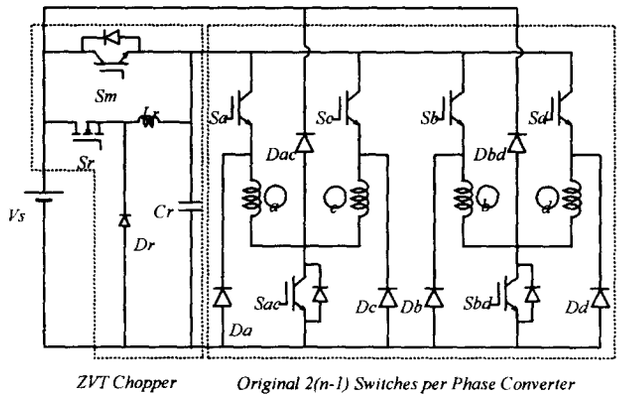


Fig. 1 Circuit topology of the previously presented ZVT PWM converter for SRM drives.[5]

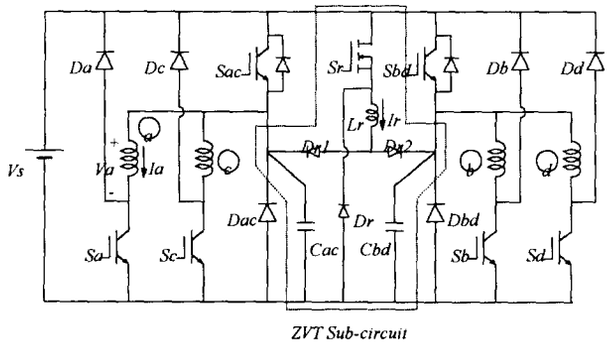


Fig. 2 Circuit topology of the proposed ZVT PWM converter for SRM drives.

ZVT sub-circuit handles only a small fraction of the main power. So, the power rating of ZVT sub-circuit is small and therefore, the cost increase is minor.

Operation principle and analysis are illustrated. A 7.5 kW, 50 kHz prototype is built and tested at 1.5 kW power level to verify the principle of operation.

2. Operation Principle

2.1 Inter-Phase Operation

The operation of the *2(n-1)*-converter is that the upper two switches are switching to control the phase current while the lower four switches are not switching but selecting one phase at a time sequentially as shown in Fig. 3. For an example, a-phase is selected by turning on Sa and the a-phase current is controlled by switching the Sac. After desired time, Sa and Sac are turned off and then the a-phase current flows through Da and Dac until it reaches zero and simultaneously, the b-phase is selected by turning on Sb and the b-phase current is controlled by switching the Sbd. In this manner, the c-phase and the d-phase are sequentially selected. The ZVT sub-circuit operates with Sac and Sbd to provide ZVS condition as shown in Fig. 3.

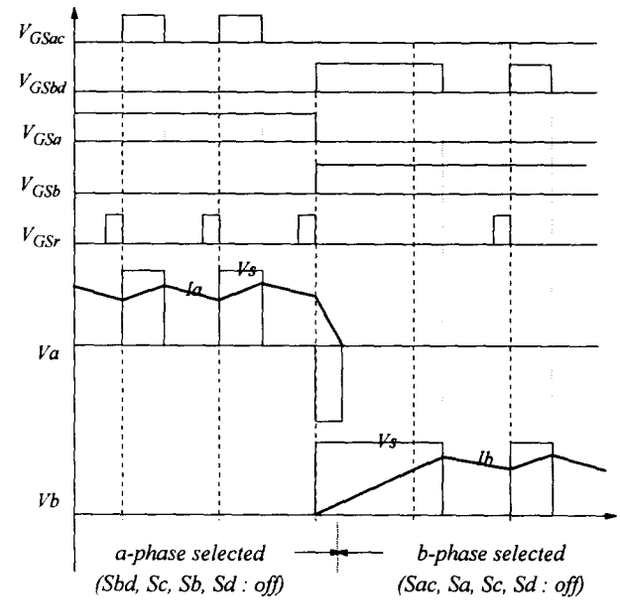


Fig. 3 Inter-phase operation waveforms of the proposed converter.

2.2 ZVT Operation

The basic ZVT operation is almost same as that of the other ZVT converters[5-7]. One switching period of Sac (or Sbd) is divided into eight operation mode and all operation mode diagrams and waveforms are shown in Figs. 4 and 5. To illustrate the steady state ZVT operation, it is assumed that all components and switches are ideal and the a-phase is selected. During the a-phase selected, Sa is turned on and Sb, Sc, Sd, and Dr_2 are turned off (Dr_2 is always reverse biased).

Mode 1: Sac is turned off and Sa and Dac is turned on. Thus, the phase current freewheels through Dac and Sa and decreases by the back-emf of the a-phase winding.

Mode 2: To turn on Sac with ZVS, the auxiliary circuit should be operated by turning on Sr and then, Ir is increased linearly through Dr1 and Dac as follows:

$$I_r(t) = \frac{V_s}{L_r} t \tag{1}$$

Mode 3: When the I_r reaches the phase current I_a, Dac is turned off with ZVS and Lr and Cac start resonating as follows:

$$I_r(t) = \frac{V_s}{Z_r} \sin(\omega_r t) + I_a \tag{2}$$

$$V_{Dac}(t) = V_s \cos(\omega_r t) \tag{3}$$

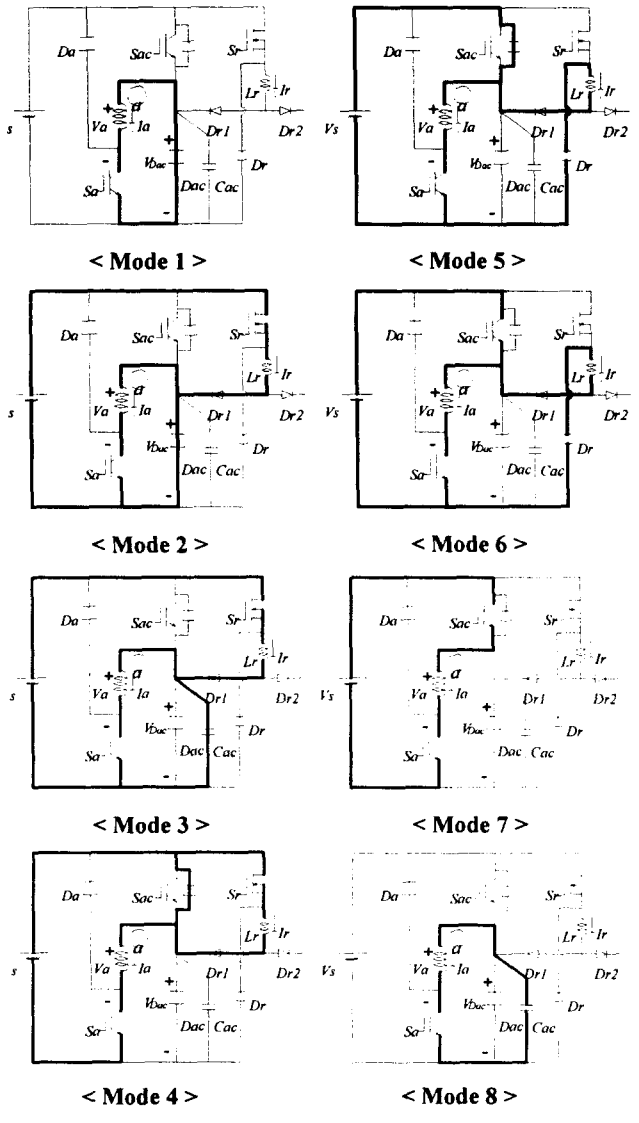


Fig. 4 ZVT operation mode diagrams.

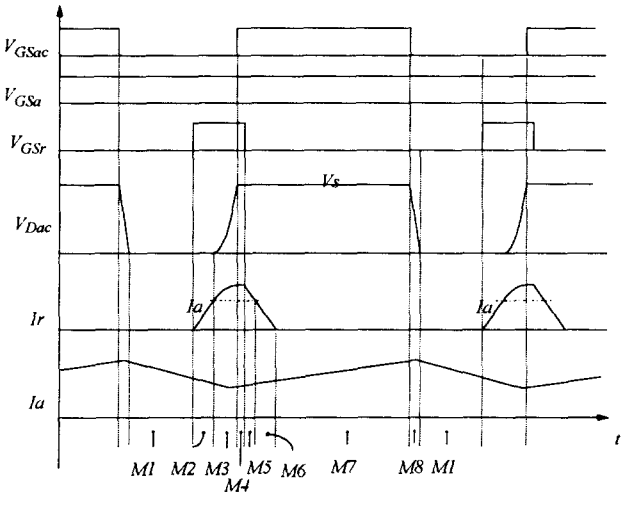


Fig. 5 ZVT operation waveforms.

where, $Z_r(t)=\sqrt{L_r/Cac}$, $\omega_r=1/\sqrt{L_r/Cac}$. The V_{Dac} increases until it reaches Vs. The time period of this mode T_{M3} can be obtained from the condition of $V_{Dac}(T_{M3})=V_s$ as follows:

$$T_{M3}=\frac{\pi}{2}\sqrt{L_rCac} \tag{4}$$

Mode 4: When V_{Dac} reaches Vs, the antiparallel diode of Sac is turned on and the resonance stops. The Sac can be turned on with ZVS. The phase current starts increasing. The time period of this mode can be varied according to the safety of the switching.

Mode 5: Sr is turned off and then, the stored energy in the Lr is recovered to the source. Then, I_r flows through Dr, Dr1, and the antiparallel diode of Sac and decreases linearly as follows:

$$I_r(t)=-\frac{V_s}{L_r}t+\frac{V_s}{Z_r}+I_a \tag{5}$$

Mode 6: When the I_r reaches I_a, the antiparallel diode of Sac is turned off. The Sac is now delivering the difference between I_a and I_r. The I_r is continuously decreased with the slope of (5) and the phase current I_a increases continuously during this mode.

Mode 7: The I_r reaches zero and all currents in the ZVT sub-circuit is completely eliminated and now, the Sac delivers the whole phase current. The phase current increases continuously during this mode.

Mode 8: By the given duty cycle, the Sac is turned off. Then, the phase current discharges C1 and V_{Dac} decreases almost linearly as follows:

$$V_{Dac}(t)=-\frac{I_a}{Cac}t+V_s \tag{6}$$

When V_{Dac} reaches zero, Dac is turned on and the phase current I_a freewheels through Dac and Sa again. The turn-off process of Sac is low loss if C1 is big enough to hold switch voltage at zero during turn-off transition. This is the ends of a switching cycle.

3. Experimental Results

The configurations and the ratings of SRM are as follows ;
Poles : 8/6 configuration
Pole arcs : 18 ° of stator and 22 ° of rotor
Air gap : 0.375mm
Min. L : 2.31mH, Max. L : 14.7mH
Power ratings : 400W

A 7.5 kW, 50 kHz prototype of the proposed converter has been built and tested at 1.5 kW power level to verify the principle of operation. Fig. 6 shows the experimental circuit with the part numbers of devices and components used. Four IRGKA050F06 (600V/50A) modules are used for the phase selecting devices (Sa-Da, Sb-Db, Sc-Dc, and Sd-Dd). Two IRGNA050F06 (600V/50A) modules are used for the switching devices (Sac-Dac and Sbd-Dbd). A IRFP460 MOSFET is chosen for the auxiliary switch since it handles low power but operates at high frequency. A C25P40FR diode module is used for Dr1-Dr2. A saturable reactor is inserted in series with Lr to eliminate the parasitic ringing between Lr and the parasitic capacitances of diodes and the switch in the auxiliary circuit and it is implemented with 4 turns on a Toshiba Spike Killer core SA 8x6x4.5.

Fig. 7 shows the waveforms of gating signal of the auxiliary switch, resonant inductor current, and chopping diode voltage and Fig. 8 shows their extended waveforms. All waveform are very clean due to ZVS and the same as the expected ones. Fig. 9 shows the ZVS switching waveforms of the chopping switch Sac. The ZVS turn-on

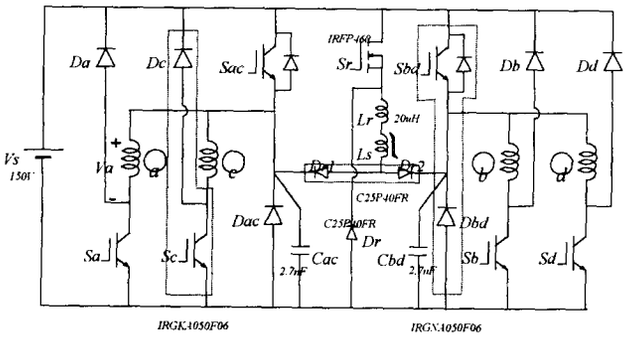


Fig. 6 Experimental circuit diagram of the proposed ZVT PWM converter.

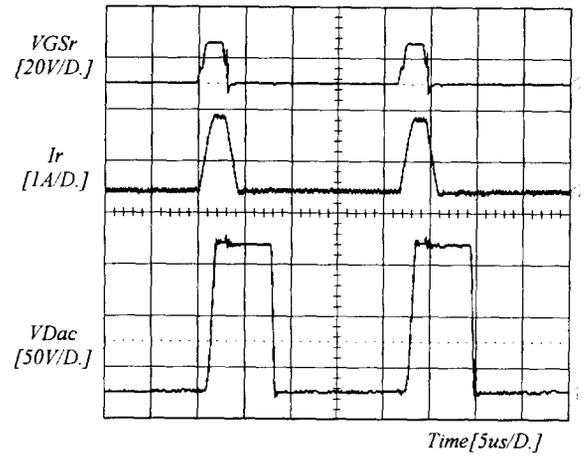


Fig. 7 Experimental waveforms gating signal of Sr, resonant inductor current, and Dac voltage.

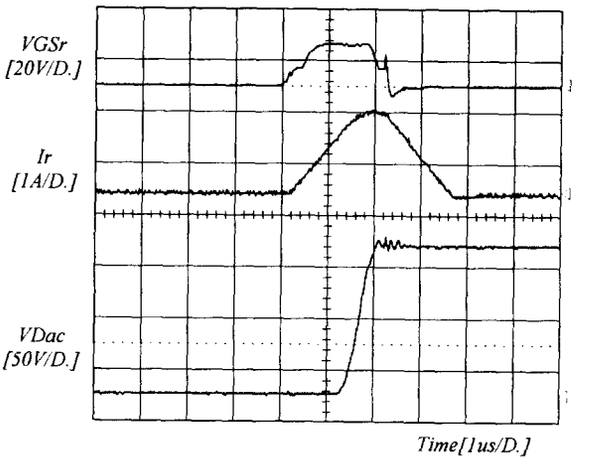
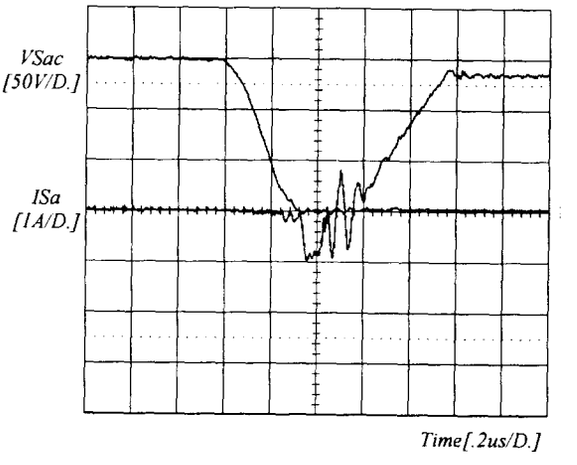
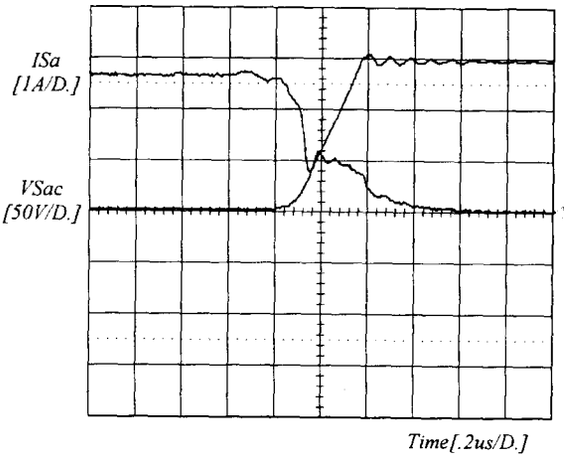


Fig. 8 Extended waveforms of Fig. 7.

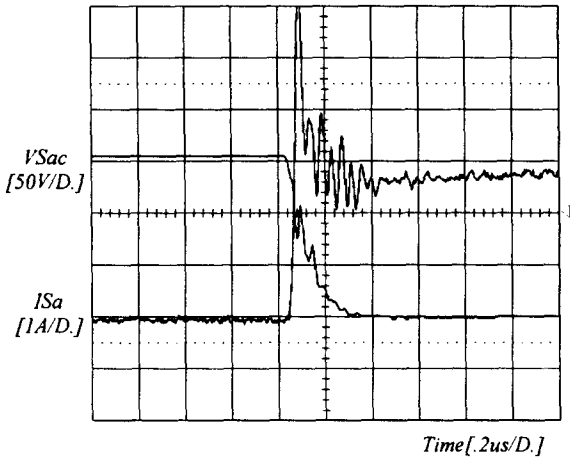


(a)

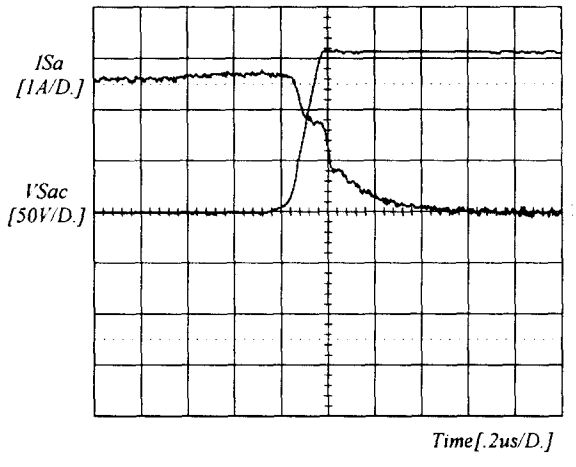


(b)

Fig. 9 ZVS waveforms of switch Sac: (a) turn-on, (b) turn-off



(a)



(b)

Fig. 10 Hard switching waveforms of switch Sac: (a) turn-on, (b) turn-off.

waveforms show a small ringing in the switch current when the current is transferred from the anti-parallel diode to the switch. This is caused by the stray inductance in the device module package. The ZVS turn-off waveforms show the typical IGBT tail current characteristic but the switching loss is considerably reduced by delaying the switch voltage applied. Fig. 10 shows the hard switching waveforms to compare with ZVS. The turn-on waveforms show high switching noise and loss which is caused by the diode reverse recovery of Dac. The turn-off waveforms show high switching loss by the IGBT tail current. Fig. 11 shows the a-phase current which has very low current ripple. Measuring efficiency of the converter for SRM drive is very difficult. To measure the efficiency of the converter, the R-L loads are connected to each phase instead of the SRM. The measured efficiency of the proposed converter at full load is 97% while the efficiency of the hard switching version is 94%.

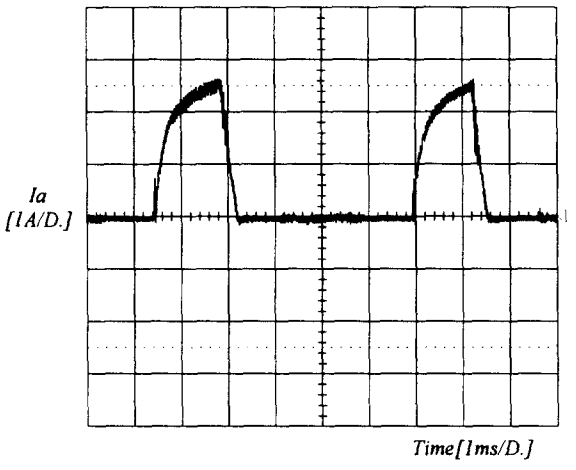


Fig. 11 Waveform of a-phase current.

4. Conclusion

A novel ZVT PWM converter for SRM drives is presented. Operation principle and analysis are illustrated and the experimental results from a 1.5 kW, 50 kHz prototype is shown to verify the principle of operation.

It is shown that a simple and low cost auxiliary circuit placed in parallel with the main power flow path provides ZVS condition to all switches and diodes without increasing device voltage and current stresses allowing high frequency operation with high efficiency and in turn fast system. The measured efficiency of the proposed converter at full load is 97% while the efficiency of the hard switching version is 94%.

It is shown that a simple and low cost auxiliary circuit response. The power rating of the auxiliary circuit is very small (about 30% of main power). So, the cost increase by the auxiliary circuit is minor. These advantages make the proposed converter very attractive for high performance SRM drives.

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