Characteristics of P-channel SOI LDMOS Transistor with Tapered Field Oxides

Jongdae Kim[a)], Sang-Gi Kim, Tae Moon Roh, Hoon Soo Park, Jin-Gun Koo, and Dae Yong Kim

A new tapered TEOS oxide technique has been developed to use field oxide of the power integrated circuits. It provides better uniformity of less than 3 % and reproducibility. On-resistance of P-channel RESURF (REduced SURface Field) LDMOS transistors has been optimized and improved by using a novel simulation and tapered TEOS field oxide on the drift region of the devices. With the similar breakdown voltage, at $V_{gs} = -5.0\ V$, the specific on-resistance of the LDMOS with the tapered field oxide is about $31.5\ m\Omega \cdot cm^2$, while that of the LDMOS with the conventional field oxide is about $57\ m\Omega \cdot cm^2$.

I. INTRODUCTION

The Lateral Double Diffused MOSFET (LDMOSFET) is considered to be one of the most desirable devices in smart power integrated circuit applications at voltage below 300V, due to its low on state resistance. The LDMOS structure on Silicon-On-Insulator (SOI) substrate has been widely used in intelligent power applications because of the implementation of low voltage CMOS signal processing circuits in conjunction with high voltage LDMOS drivers on the same chip. It has also been the advantages of process compatible to VLSI process and is easy to integrate with other process.

For power devices, specific on-resistance (R_{sp}) and breakdown voltage are critical to device performance. Advances in process technology have improved transistor's packing density and, consequently, transistor's specific on-resistance. Different techniques have been used to reduce specific on-resistance while keeping the breakdown voltage high. Many studies on the R_{sp} and breakdown voltage improvement of LDMOSFET device have been reported [1]–[4]. However, improvements in specific on-resistance have been limits in conventional design geometries because of the long drift region. Furthermore, the breakdown voltage of this lateral structure is highly dependent on the distance between the end of the gate and drain diffusion, called the drift length.

In this paper, a novel p-channel LDMOS structure on SOI substrate with new tapered TEOS field oxides on the drift region is proposed in order to prevent boron out-diffusion at high temperature and reduce current path in the drift region, leading to the improvement of device on resistance. To ensure the high voltage capability, the REduceed SURface Field (RESURF) technique [5] and field plates [6] are used. The breakdown, dc and transient characteristics of the device are investigated both

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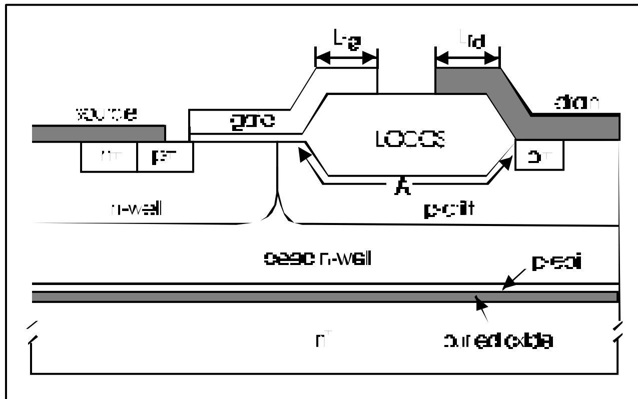

Fig. 1. The cross section of p-channel SOI LDMOSFET with LOCOS field oxide.

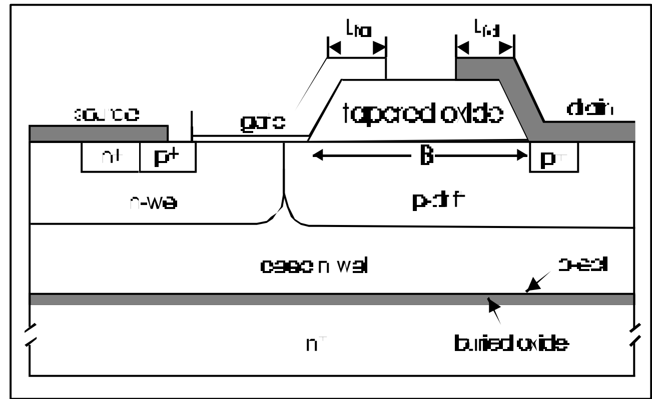

Fig. 2. The cross section of p-channel SOI LDMOSFET with a tapered field oxide. The drift length (B) is shorter compared to that (A) shown in Fig. 1.

theoretically and experimentally. Optimization of the process parameters involved in the design of the structure is presented. This tapered oxide technology can also be used on good step coverage and junction extension [7]–[9].

II. PROPOSED DEVICE STRUCTURE AND OPTIMIZATION

A conventional LDMOS structure is shown in Fig. 1. For the structure of the device, field oxide using a conventional LOCOS method is added on the drain side and drift region. The R_{sp} is increased significantly due to the longer current path (A) underneath the field oxide and impurity out-diffusion that occurs during the growth phase of the thick field oxide at high temperature [10]–[11]. In order to decrease the R_{sp}, the current path and the impurity out-diffusion need to be reduced. The LDMOS structure with a new tapered field oxide (Fig. 2) on the drift region is proposed here to improve R_{sp} by reducing the current path (B) and preventing impurity redistribution in the drift region.

It is important to improve the device performance by optimizing on-resistance for a given area and a breakdown voltage. A cost effective and elegant method to utilize such a trade-off between on-resistance and breakdown voltage is to optimize the device layout. Both experimental measurements and device and process simulations can achieve this goal. In the development of the p-LDMOS structure, two dimensional DIOS and DESSIS [12] simulations were performed for the structures of Figs. 1 and 2 to obtain the electrical characteristics, doping profile, junction depth, and studies on high-voltage p-LDMOS devices. We investigated different device structure and design parameters for device optimization. The simulation results are compared with experimental data for two different device layouts, namely, the conventional and the tapered structures.

Process simulations were performed using DIOS and the results were incorporated into 2-D structures as shown in Fig. 3.

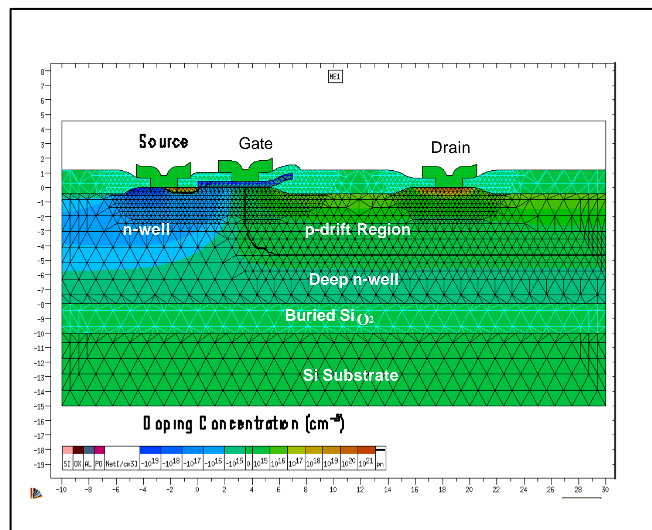

Fig. 3. Simulated LDMOS structure with doping of stripe cell lateral DMOS using DIOS simulator. This structure shows SOI substrate, drift and well region with impurity concentration and junction depth.

The optimized results were obtained when the impurity concentrations of the drift region with the junction depth of 4 ~ 5 µm, the channel, and the source/drain regions were $6\times10^{15}/cm^3$, $7\times10^{16}/cm^3$, and $5\times10^{19}/cm^3$ respectively. The optimized values of the drift length (A or B), the length of gate field plate over the drain region (L_{fg}), and the length of the drain field plate (L_{fd}) over the drift region were 15, 5, and 5 µm respectively.

Device simulations were performed using DESSIS based on the date from the DIOS. Figure 4 shows the simulated potential distribution of the LDMOS with the conventional field oxide, while the simulated potential distribution of the LDMOS with the tapered field oxide is represented in Fig. 5. As observed in these figures, the breakdown voltage for the structure of Fig. 1 is limited to 296 V, while the breakdown voltage for the struc-

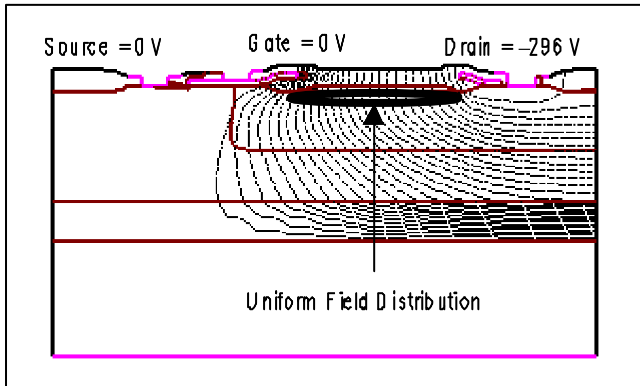

Fig. 4. Equipotential lines in off-state of the p-LDMOS with conventional field oxide, Vg = 0 V and Vd = −296 V (spacing between adjacent lines = 10 V)

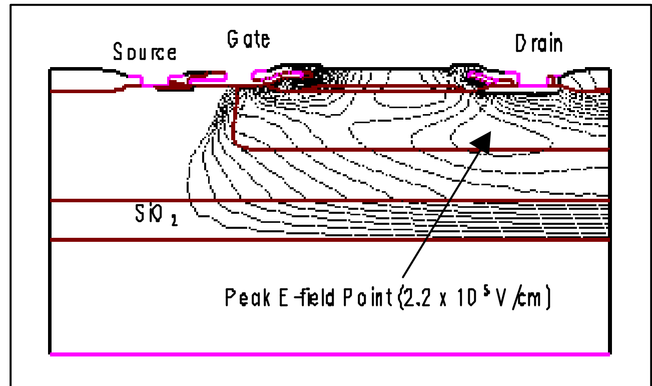

Fig. 6. Electric field distribution of the p-LDMOS with conventional field oxide (spacing between adjacent lines = 2×10^4 *V/cm*). The electric field crowds at the junction of the p-drift and deep n-well inside bulk.

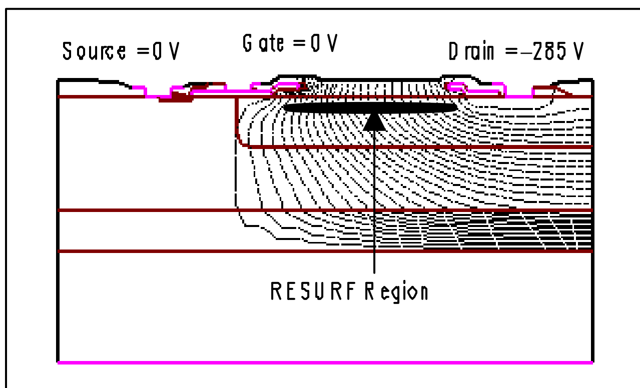

Fig. 5. Equipotential lines in off-state of the p-LDMOS with tapered field oxide, Vg = 0 V and Vd = −285 V (spacing between adjacent lines = 10 V)

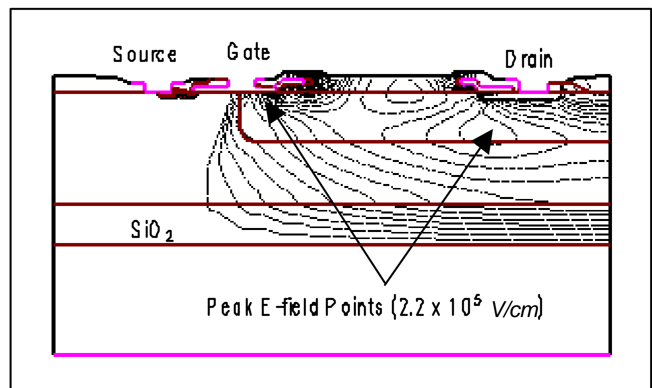

Fig. 7. Electric field distribution of the p-LDMOS with tapered field oxide (spacing between adjacent lines = 2×10^4 *V/cm*). The critical field region is the silicon surface near the gate and the junction of the p-drift and deep n-well inside bulk.

ture of Fig. 2 is 285 V. They can clearly be seen that the electrical field is much more uniformly distributed at the drift region. This means that, when the supplying voltage increases, the p-drift region is completely depleted, yielding an optimized RES URF condition and generation of a critical electrical field inside bulk.

The simulated field distributions in the structures of Figs. 1 and 2 are presented in Figs. 6 and 7, respectively. It can be seen that for the structure in Fig. 1, the electric field in the silicon surface near the drain is reduced because of RESURF principle and the highest electric field is located inside the bulk, as shown in Fig. 6. Therefore, avalanche breakdown occurs inside the bulk. In the proposed structure shown in Fig. 7, the highest electric field ($2.2\times10^5\, V/cm$) exists both on the silicon surface near the gate edge and inside the bulk. Therefore, the breakdown is only dependent on the impurity concentration in the drift region of the structures of Figs. 1 and 2, to both of which RESURF technique was applied.

Figures 8 and 9 plot impact ionization contours in devices Figs. 1 and 2. Due to the completely resurfed drift region, the electrical field is very high inside the bulk. As a result, there is very high impact generation rate inside the bulk leading to the breakdown of the device, as shown in Fig. 8. In addition to impact ionization inside the bulk, Fig. 9 shows high impact ionization rate near the gate side. This is due to the curvature near the gate edge, leading to the high electric field and another impact ionization region. The impact ionization region near the gate edge causes a decrease in impact ionization rate inside bulk. As a result of division of the im pact ionization region into two, the total impact ionization rate within the device is effectively decreased, corresponding to the breakdown voltage improvement. The current flows along the silicon surface and the inside bulk of the conventional and the proposed stru ctures.

The simulated specific on-resistances of the LDMOS device with LOCOS field oxide and the tapered filed oxide were obtained $55\,m\Omega\cdot cm^2$ and $32\,m\Omega\cdot cm^2$ at the breakdown voltages of 298 V and 285 V, respectively when the gate voltage of −5 V is applied. These values are consistent with the experimental ones although the breakdown voltage is lower than that of the experimental one.

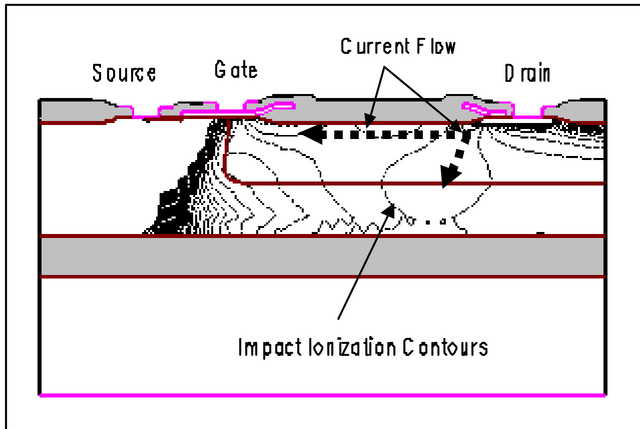

Fig. 8. Impact ion distribution and current flow in drift region of the p-LDMOS with the conventional field oxide.

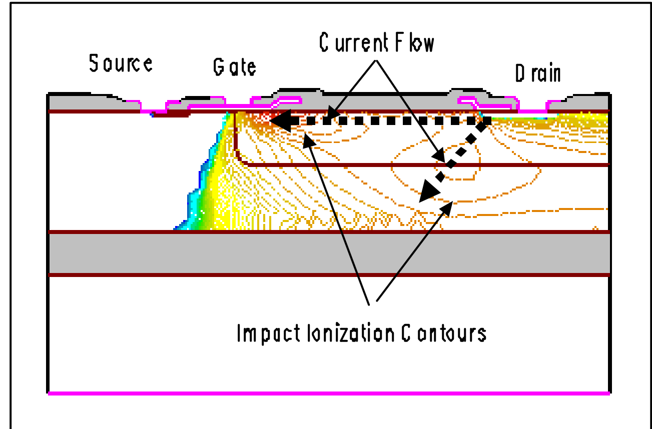

Fig. 9. Impact ion distribution and current flow in drift region of the p-LDMOS with the tapered field oxide.

III. TAPERED OXIDE TECHNIQUE AND PROCESS SEQUENCE

The new tapered TEOS field oxide was made through 200 Å of thermally grown (850 °C) screen oxide, thick TEOS oxide (8000 Å) annealed at 850°C in N_2, and thin TEOS oxide (2000 Å) [13]. In the double-layer structure of the thick TEOS/thin TEOS layer, the upper layer is etched extremely fast in the buffered HF solution, while the etch rate of the lower layer is slow. The SEM photograph of the tapered field oxide is shown in Fig. 10, which shows the taper angle of 40°. The taper angle of the TEOS oxide varies from near 60° to 20° with no steep portion at the top of the step. The feature sizes of the tapered field oxides have been measured with the SEM, as shown in Fig. 10. Five different wafers were provided from different runs and twenty different regions of each wafer (total 100 points) have been observed. The new technique provides better uniformity of less than 3% and reproducibility. This technology is very simple and low temperature process, compared to others [5]–[7].

It is well known that the thermal oxidation of silicon at high temperature causes redistribution of impurities at the silicon-silicon dioxide interface. An effect of the thermal oxidation on the distribution of impurity, especially boron, in drift region of LDMOSFETs performs very important role in making a device optimization. The distribution of boron after field oxidation using conventional LOCOS or the tapered TEOS oxide technique has been reported [13]. In the previously reported paper, the boron impurity concentration in the drift region of the device prior to field oxidation was $6.7\times10^{15}\ cm^{-3}$. Boron out-diffusion into the field oxide is, however, observed from the surface of the drift region with conventional field oxide, resulting in the concentration of $4.2\times10^{15}\ cm^{-3}$, while boron out-diffusion into the field oxide is very small ($\sim6.7\times10^{15} cm^{-3}$) when the tapered TEOS field oxide is used as a field oxide of the p-LDMOSFETs.

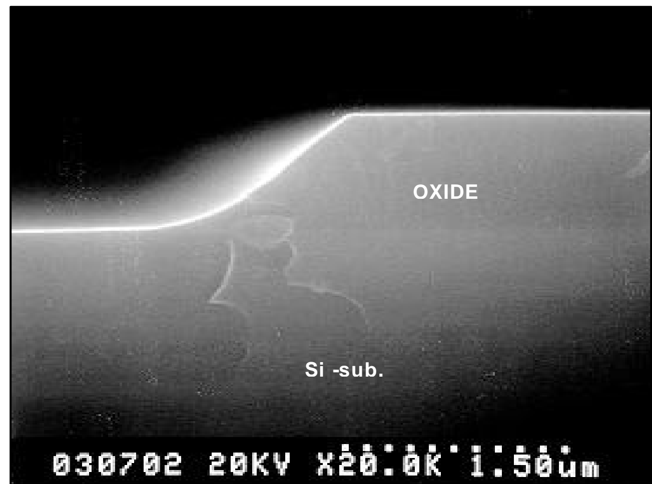

Fig. 10. SEM picture of the new tapered field oxide. The taper angle of the field oxide shows 40° whose value can be changed by TEOS oxide thickness and annealing temperature.

The p-channel LDMOSFETs were fabricated on SOI wafers with 2 µm buried oxide and 8 µm p-epi layer using a standard 1.2 µm twin well CMOS process to apply RESURF principle and enhance compatibility with CMOS process. The standard LOCOS technology or the tapered TEOS oxidation technology was used for the field oxide on the lightly doped RESURF region of the device. A p-well, which forms the drift region of p-LDMOSFET is implemented by using boron with implant doses of $2.0\sim9.5\times10^{12}/cm^2$. This implant dose is carefully controlled so that the RESURF principle is satisfied. The n-well implant dose of $1.0\sim4.0\times10^{13}/cm^2$ using phosphorus at 125 keV is followed for the channel region of the high voltage p-LDMOSFET. The n- and p-well are annealed at 1150 °C to obtain 3.0 ~ 4.5 µm junction depth. The gate oxide of 500 Å and second metal of 1.5 µm were used. The remaining process is a standard 1.2 µm analog CMOS process.

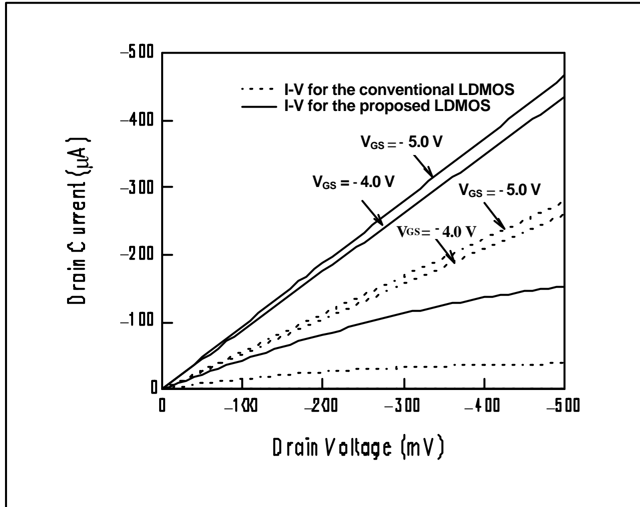

Fig. 11. Forward on-resistance characteristics of LDMOS devices with the conventional field oxide (dot line) and the tapered TEOS field oxide (solid line). The proposed LDMOSFET has twice drain current compared to the conventional LDMOSFET.

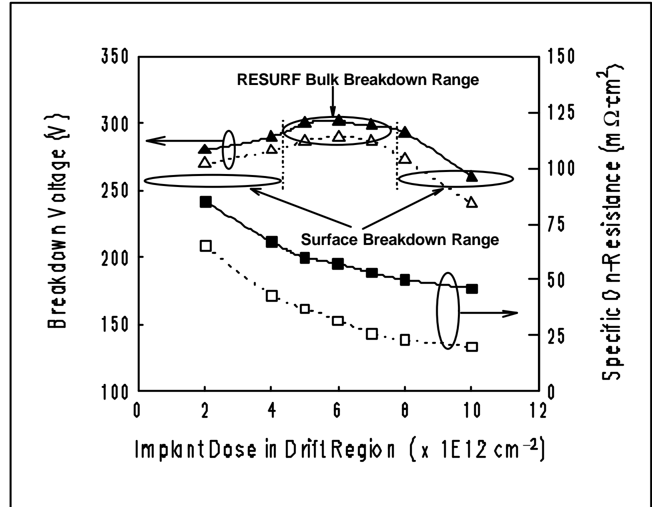

Fig. 12. The distribution of specific on resistance and breakdown voltage as a function of boron dose in drift region. The filled symbols represent the values obtained from the devices with conventional field oxide, while the empty symbols indicate the values obtained from the devices with tapered field oxide.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The on state characteristics for the LDMOS devices with the conventional field oxide and the tapered field oxide are shown in Fig. 10. At $V_{gs} = -5.0\ V$, based on the current-voltage characteristics in Fig. 10, calculated specific on-resistance for the device with the conventional field oxide is given by

$$R_{sp} = 110\ mV / 59.1\ \mu A \cdot 3.0 \times 10^{-5}\ cm^2 = 57\ m\Omega \cdot cm^2 .$$

The calculated specific on-resistance for the device with the tapered field oxide is as follows.

$$R_{sp} = 270\ mV / 257.6\ \mu A \cdot 3.0 \times 10^{-5}\ cm^2 = 31.5\ m\Omega \cdot cm^2$$

when the gate voltage of – 5 V is applied. From the experimental results, the specific on-resistance for the proposed structure is improved by 40 % compared to the conventional structure. The reason is that the TEOS field oxidation at low temperature prevents the out-diffusion at the surface for a given RESURF region and shortens the drift length (B) of the proposed structure. The final difference between A and B in Figs. 1 and 2 is about 1.5 ~ 1.6 μm when the field oxide thickness is 8500 Å.

A similar breakdown characteristic has been reported by our previous paper [13]. The breakdown voltages of the conventional LDMOS and the proposed LDMOS are limited to 305 V and 295 V, corresponding to only 5 % difference between the conventional one and the proposed one.

Experimental results of the R_{sp} and breakdown voltage as a function of boron RESURF implantation into deep n-well are illustrated in Fig. 12. The characteristics show that R_{sp} decreases with increasing boron doping for a given n-type drift region concentration. At low boron doses, the ava- lanche breakdown occurs at silicon surface near the drain and the gate edge because the highest electric field exists on the silicon surface near the drain. As boron dose is increased ($5 \sim 8 \times 10^{12}\ cm^{-2}$) a maximum bulk RESURF breakdown is achieved due to the RESURF principle and the highest electric field located inside the bulk. At high boron dose (> 8× $10^{12}\ cm^{-2}$), the avalanche breakdown also occurs at silicon surface near the drain and the gate edge because the highest electric field exists on the silicon surface near the drain. Therefore, the avalanche breakdown is only dependent on the impurity concentration in the drift region of the structures of Figs. 1 and 2, to both of which RESURF technique was applied. It is also shown in the figure that with the similar breakdown voltage, the on- resistance can be improved by 35 % or more with this proposed structure. This is due to the reducing the current path of 1.5 μm and the preventing the out-diffusion of impurity from the surface of the drift region.

The electrical characteristics of R_{sp} and BVDSS for 100 p-LDMOSFETs supplied by 5 different wafers have been also measured. The uniformity of R_{sp} and VBDSS are less than 5 % and 3 %, respectively. The IDSS leakage current is less than 1 nA in both LOCOS structure and the tapered structure whose value was measured by Tektronix Programmable Curve tracer 370 A at the supplied voltage of –300 V.

V. CONCLUSION

A new tapered TEOS oxide technique has been developed to use field oxide of the power integrated circuits. Reproducible tapered field oxide (~1 μm thickness) has been formed in TEOS oxide by use of a double-layer structure and low temperature annealing process, producing a uniform taper of 20° – 60°. This technology is very simple and provides better uniformity of less than 3 % and reproducibility.

Using process and device simulation, it is shown that the conventional and the proposed structure of p-LDMOS transistors exploit the RESURF principle that results in reduced surface electric fields and thus improve the breakdown voltage. This enables device structure optimization using device simulation, leading to a drastic reduction of on-resistances.

On-resistance of P-channel RESURF LDMOS transistors has been improved by using the novel tapered TEOS field oxide on the drift region of the devices. With the similar breakdown voltage (5 % reduction), the on-resistance can be improved by 35 % or more with the proposed p-LDMOSFET. This is due to the reducing of the current path and preventing out-diffusion of impurity from the lightly doped RESURF region. The uniformities of R_{sp} and VBDSS are less than 5 % and 3 %, respectively. The IDSS leakage current of the LDMOS with the tapered field oxide is less than nA at the supplied voltage of −300 V.

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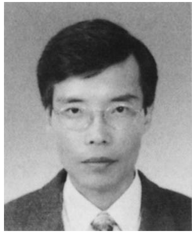

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