Design and Characterization of a 10 Gb/s Clock and Data Recovery Circuit Implemented with Phase-Locked Loop

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A clock and data recovery circuit with a phase-locked loop for 10 Gb/s optical transmission system was realized in a hybrid IC form. The quadri-correlation architecture is used for frequency- and phase-locked loop. A NRZ-to-PRZ converter and a 360 degree analogue phase shifter are included in the circuit. The jitter characteristics satisfy the recommendations of ITU–T. The capture range of 150 MHz and input voltage sensitivity of 100 mVp-p were showed. The temperature compensation characteristics were tested for the operating temperature from –10 to 60 ºC and showed no increase of error. This circuit was adopted for the 10 Gb/s transmission system through a normal single-mode fiber with the length of 400 km and operated successfully.

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I. INTRODUCTION

The transmission rate of optical communication has been drastically increased since it was introduced in the late 1970s. At the present time, 10 Gb/s transmission systems are being deployed for the commercial service. The high speed circuit blocks for the 10 Gb/s signal processing, however, are still remained to be improved for the higher operating margin and the higher reliability. Especially, the clock and data recovery circuit (CDR) should be improved to maintain a sufficient decision phase margin over a wide operating temperature.

The function of CDR is to recover the clock from the transmitted data and retime the data with the recovered clock. The transmitted data include much timing jitter that generated from the chromatic dispersion and the noise of optical transmission channel. The CDR should be designed to be tolerable to this timing jitter and generate a clock with a small timing jitter.

The narrow band-pass filter for 10 GHz-clock extraction in CDR can be realized with either a dielectric resonator filter or a phase-locked loop (PLL) filter [1]–[2]. The CDR with a PLL has several advantages: the possibility of a monolithic integration, low cost and high reliability, and phase locking between the extracted clock and the data signal. Recently there have been reports on 10 Gb/s PLL CDR [3]–[4]. One is a hybrid IC format [3] and the other is a monolithic integrated with an external loop filter [4].

In this paper, we describe design techniques and performance of a PLL CDR in a hybrid format using a commercially available IC. A new non return to zero-to-pseudo return to zero (NRZ-to-PRZ) converter and a 360 degree analog phase shifter are developed for better performance. Section II discusses the

circuit architecture and design details. In Section III, we will show the results of extensive characterization of the circuit and their relevance to the ITU–T standards [5]. Conclusions are presented in Section IV.

II. CIRCUIT CONFIGURATION

Figure 1 shows the block diagram of CDR consisting of an input buffer amplifier, a clock recovery circuit, two sets of phase shifter, and a decision circuit. The 10 Gb/s data amplified by the input buffer are fed both to the decision circuit and to the clock recovery circuit. The clock recovery circuit extracts the clock from the 10 Gb/s NRZ data. The recovered clock is connected to the decision circuit through a phase shifter. The decision circuit retimes the input data by the recovered clock. The phase shifter adjusts the clock phase to an optimum position for the decision of the incoming data.

The performance of CDR largely depends on the clock recovery circuit. Figure 2 shows the block diagram of the clock recovery circuit consisting of an NRZ-to-PRZ converter and a PLL circuit. The NRZ-to-PRZ converter transforms 10 Gb/s NRZ data into pseudo-RZ data that include a discrete clock signal in their spectrum.

Figure 3 shows the NRZ-to-PRZ converter. It obtains both a differentiated signal and a phase-inverted differentiated signal of an incoming data, and rectifies each signal with a half-wave rectifier, respectively, and then combines both signals to generate a pseudo-RZ signal. A Lange coupler is successfully configured to generate two differentiated signals and a bridge diode is used to rectify and combine them. The performance of the new NRZ-to-PRZ converter is comparable with that of a conventional signal converter implemented with EX-OR circuit. The ratio of clock amplitude to the noise spectral density was measured to be 90 dB which was about the same as that of EX-OR type, and it consumes negligible power and

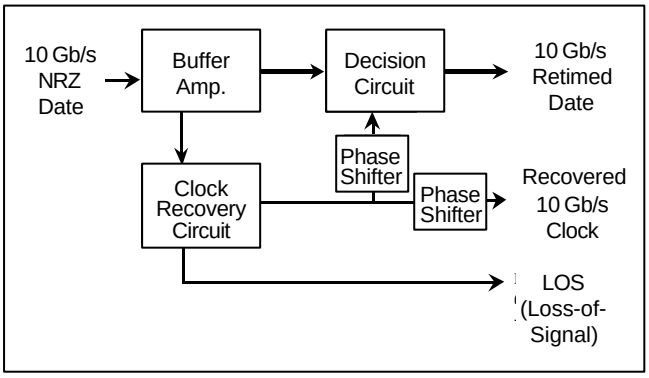

Fig. 1. The block diagram of 10 Gb/s clock recovery and data regeneration circuit.

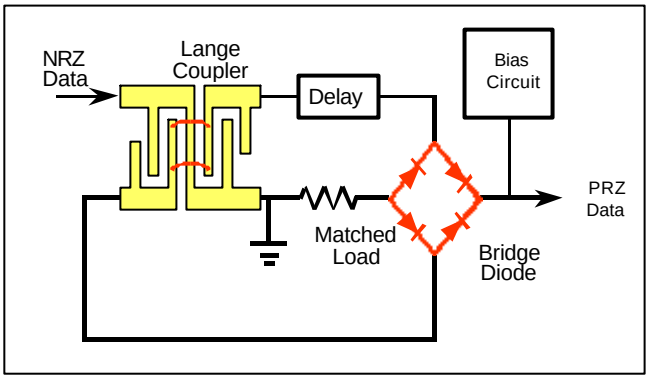

Fig. 3. NRZ-to-PRZ converter.

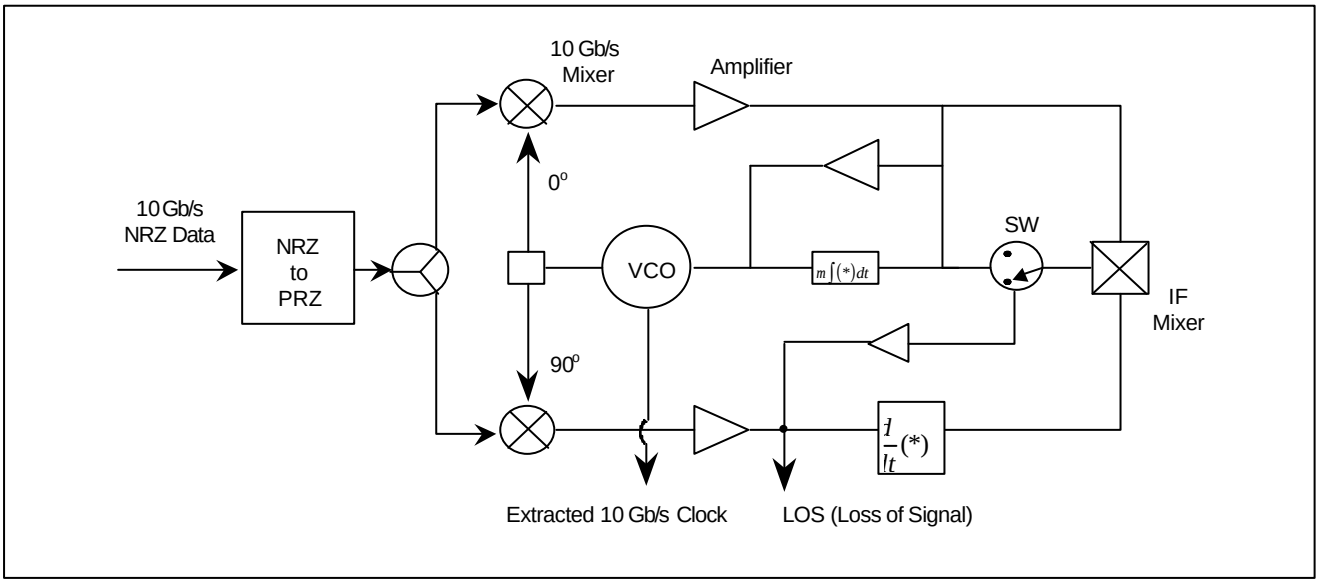

Fig. 2. The block diagram of clock recovery circuit.

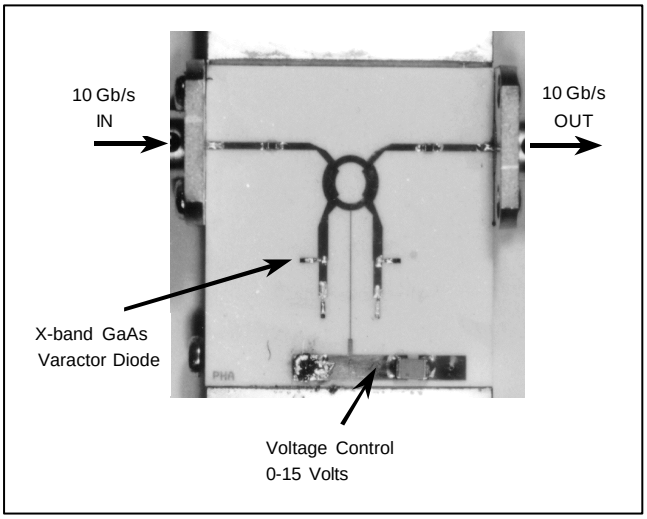

Fig. 4. The photograph of 10 GHz analogue phase shifter.

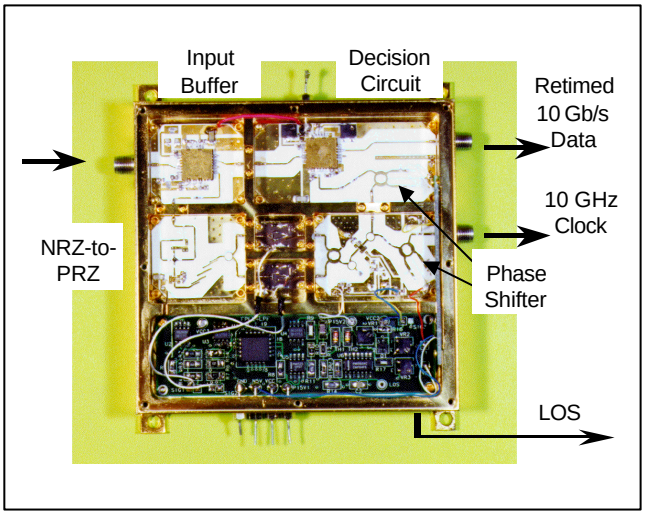

Fig. 5. The photograph of clock and date recovery circuit.

therefore has a good temperature stability. Therefore, the new NRZ-to-PRZ converter will be a favorable choice over the EX-OR type for a high-speed clock recovery circuit. In the PRZ signal, there are noise generated from the randomness of the input data. A band-pass filter with 0.9 GHz 3 dB-bandwidth filters out the noise around the clock signal.

The PLL circuit performing as a narrow band-pass filter is realized in a quadri-correlator frequency- and phase-locked loop (FPLL) [7]–[8]. The dc signal at the output of the IF mixer in Fig. 2 is proportional to the frequency difference between the input clock and the VCO output, and is negatively fed back to the VCO to reduce the frequency difference. This dc signal, however, causes a large voltage offset in PLL after the freuency-locked loop (FLL) completes its function. A switching circuit was built into the conventional FPLL to switch off the FLL signal and avoid the large voltage offset originated from the FLL signal. Besides, the CDR has a loss of signal detection function by using the switch circuit.

Figure 4 shows the photograph of a phase shifter. Two sets of phase shifter were used in CDR. One is for adjusting VCO clock phase to an optimum position for the decision of the incoming data and the other is for adjusting output clock phase. To assemble phase shifters into a CDR module, a size becomes a major design issue. The other issues are to minimize the magnitude and the variation of the insertion loss. In this work, we use a reflection-type analog phase shifter consisting of reflection load [9] and a 90 degree hybrid coupler. The reflection-type analog phase shifter produces the phase shift by reflecting the incident wave with a varactor diode whose capacitance varies according to the bias voltage. We derived the analytic formulas for both the phase shift and the insertion loss [10]. Using the formulas a small size 360 degree phase shifter could be implemented in a single stage hybrid coupler format. The implemented phase shifter shows that the total phase shift range is 380 degree and insertion loss is -4.5 ± 0.8 dB with the control voltage varied from 0 to 15 V.

One of the important issues in CDR is to obtain a stable phase relationship between the incoming data and the extracted clock over the wide operating temperature. In this work this relative phase variation was minimized by adjusting the clock phase with the phase shifter whose control voltage is designed to vary according to the temperature utilizing a simple temperature sensor.

Figure 5 shows the photograph of the CDR. It consists of 4 alumina substrates of 25-mil thickness, two sets of 10 GHz mixer, and a FPLL loop filter built on a printed circuit board. The circuit size is $99 \times 95 \times 15$ mm^3.

III. PERFORMANCES

Figure 6 shows the output waveforms in the time domain in response to a pseudorandom binary sequence of the length $2^{23}-1$ at 10 Gb/s rate from a pulse pattern generator. The top trace is the eye diagram of the output data and the bottom trace is the recovered clock. The input voltage sensitivity—the minimum distinguishable data input voltage amplitude—is about 100 mV. The capture range is over 150 MHz, which is wide enough to cover the deviation of free running frequency of VCO due to changes of ambient temperature. The decision phase margin is measured to be 60 ps (216 degree).

The CDR was evaluated by the jitter characteristics—jitter tolerance, jitter transfer, jitter generation. Jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter causing a 1 dB-power penalty. A sinusoidal jitter is inserted into 10 Gb/s data by modulating the frequency of the reference clock of the pulse pattern generator with a sinusoidal wave. Figure 7

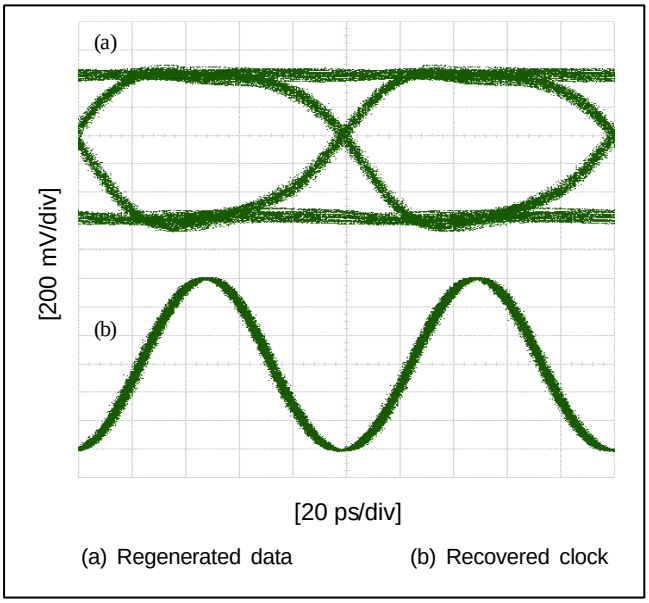

Fig. 6. Output waveform of 10 Gb/s CDR.

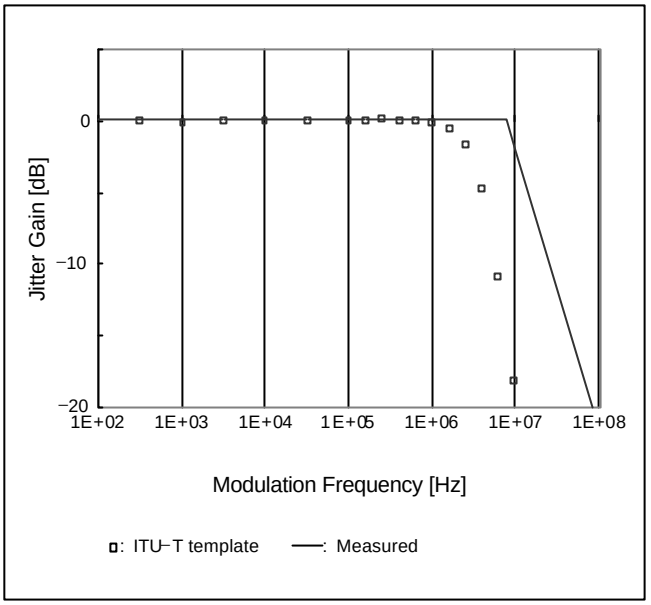

Fig. 8. Jitter transfer function at 10 Gb/s.

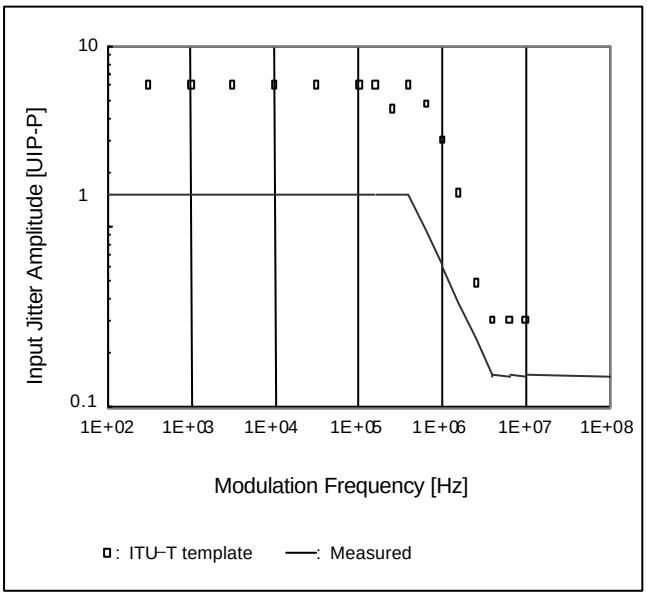

Fig. 7. Jitter tolerance at 10 Gb/s.

shows jitter tolerance measured at jitter frequencies ranged from 100 Hz to 10 MHz. The measured jitter tolerance shown in blocks is larger than the jitter tolerance limit obtained by extending the ITU−T recommendation to 10 Gb/s system.

The jitter transfer function is specified with 3 dB bandwidth and the peak value. The measured transfer function in Fig. 8 shows no peak value and the 3 dB bandwidth of 4.5 MHz. The transfer function also satisfies the ITU−T recommendation.

The rms jitter of the clock was measured by using commercial jitter analyzer. The rms jitter is 0.93 ps and the peak-to-peak jitter is 4.3 ps which is smaller than 0.01 UI (1 ps) rms jitter or 0.1 UI (10 ps) peak-to-peak jitter recommended by the ITU–T.

The CDR compensated against the temperature was tested for the temperature from −10 to 60 degrees in chamber and showed no error in the whole temperature range. This CDR was adopted for the 10 Gb/s transmission system with a normal single-mode fiber of the length of 400 km and the chromatic dispersion of ~17 ps/nm km.

VI. CONCLUSIONS

We developed a 10 Gb/s clock and data recovery module using a new NRZ-to-PRZ converter and two sets of analogue phase shifter in the quadri-correlation architecture. The implemented CDR shows the capture range of 150 MHz, the input voltage sensitivity of 100 mV, and the decision phase margin of 60 ps. An rms jitter generation of < 0.01 UI, good jitter-tolerance, and low jitter-transfer cutoff frequency, all of which meet the jitter requirements in the ITU–T recommendations. The CDR compensated against the operating temperature through the automatic adjustment of the clock phase was tested for the temperature from −10 to +60 degree and showed no error during the whole measurement period.

The NRZ-to-PRZ converter consumes negligible power and therefore has good temperature stability. This will be a favorable choice over the EX-OR type for a high-speed clock recovery circuit. The phase shifters enable input clock of decision circuit and output clock of CDR to have their optimum positions by changing their phase up to 360 degrees.

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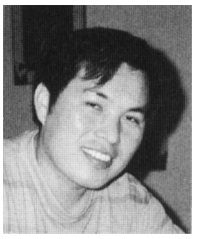

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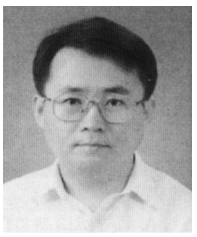

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See *ETRI Journal*, Vol. 20, No. 1, March 1998, p. 36.

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