Thick Metal CMOS Technology on High Resistivity Substrate and Its Application to Monolithic *L*-Band CMOS LNAs

Cheon Soo Kim[a], Min Park, Chung-Hwan Kim, Hyun Kyu Yu, and Hanjin Cho

Thick metal 0.8 μm CMOS technology on high resistivity substrate (RF CMOS technology) is demonstrated for the *L*-band RF IC applications, and we successfully implemented it to the monolithic 900 MHz and 1.9 GHz CMOS LNAs for the first time. To enhance the performance of the RF circuits, MOSFET layout was optimized for high frequency operation and inductor quality was improved by modifying the technology. The fabricated 1.9 GHz LNA shows a gain of 15.2 dB and a NF of 2.8 dB at DC consumption current of 15 mA that is an excellent noise performance compared with the off-chip matched 1.9 GHz CMOS LNAs. The 900 MHz LNA shows a high gain of 19 dB and NF of 3.2 dB despite of the performance degradation due to the integration of a 26 nH inductor for input match. The proposed RF CMOS technology is a compatible process for analog CMOS ICs, and the monolithic LNAs employing the technology show a good and uniform RF performance in a five inch wafer.

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I. INTRODUCTION

The strong demand for portable wireless communication systems motivates the research of radio frequency modules in complementary metal oxide semiconductor (CMOS) technology. To integrate baseband, intermediate frequency (IF) and radio frequency (RF) modules in a single chip for low cost, CMOS or Bipolar and CMOS (BiCMOS) technology is a good candidate for the solution [1]–[5]. Recently, RF transceivers have been implemented by deep sub-micron CMOS technology. But the performance of several RF transceivers fabricated using CMOS technology are very weak to noise performance, and not sufficient enough to meet the specifications of personal communication systems for 1 ~ 2 GHz range. The CMOS technology has many obstacles to overcome for low noise RF circuit applications. To overcome these problems, the quality of passive devices, especially spiral inductor, should be enhanced for RF IC applications. Moreover, the gate geometry and bias condition of device should be optimized to maximize the high frequency performance of MOSFET.

In this paper, we firstly demonstrate a CMOS technology suitable for the fabrication of RF ICs by employing the thick metal process and high resistive substrate, and we successfully implemented it to the monolithic 900 MHz and 1.9 GHz CM OS low noise amplifiers (LNAs). The proposed RF CMOS technology is a compatible process for digital and analog CMOS ICs. And the monolithic LNAs employing the technology show a good and uniform RF performance in a five inch wafer.

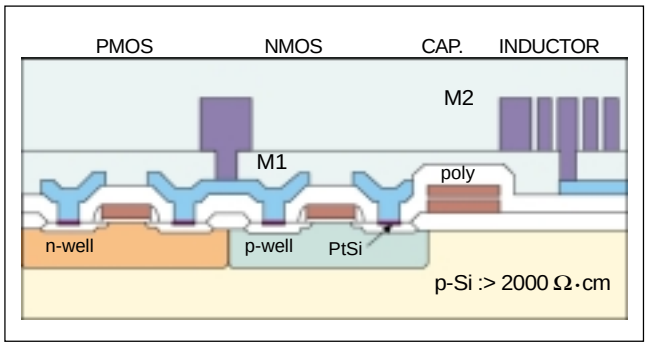

Fig. 1. Cross sectional view of thick metal RF CMOS technology on high resistivity silicon substrate for RF circuits.

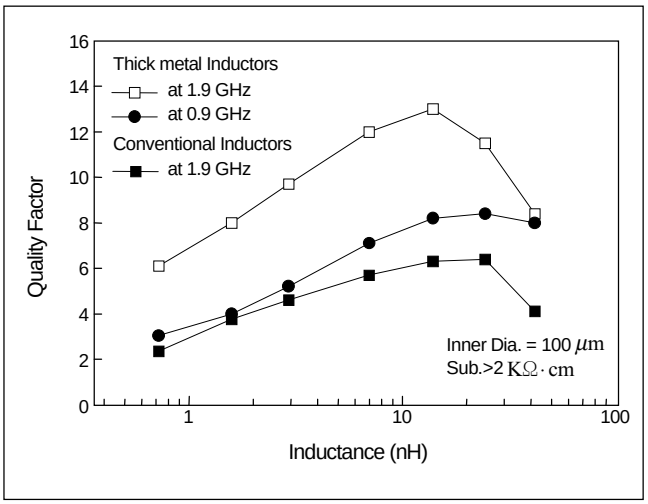

Fig. 2. Quality factor versus inductance of spiral inductors fabricated with thick (3.1 μm) and thin (1.1 μm) metal process.

II. RF CMOS TECHNOLOGY

1. Spiral Inductor Quality

The fabrication procedure of RF CMOS technology is the same as the conventional 0.8 μm twin-well CMOS technology except using the high resistivity silicon wafer. To reduce the substrate loss of spiral inductor due to the conducting substrate, the high resistive silicon substrate was adopted. All of the active devices were designed within well region and passive devices were placed on the high resistive substrate as shown in Fig. 1. Furthermore, thick metal process was employed to reduce the resistance of inductor [6].

Figure 2 shows the quality factor Q of spiral inductor employing the RF CMOS technology. A 13 nH inductor fabricated on substrate with 2 KΩ·cm resistivity shows a Q value of 6.4 at 2 GHz, and this value increases up to 12.9 by employing the thick metal process. The 1~30 nH inductors with the Q of 3~13 range can be easily obtained. The Q of spiral inductors according to the fabrication technologies is summarized in Table 1. The Q of spiral inductors on high resistivity substrate (>2 KΩ·cm) is about 3.6 times larger than that of low resistivity (5 Ω·cm) substrate in the same size inductor. The Q of 6.4 increases up to 12.9 by only increasing the second metal thickness from 1.1 μm to 3.1 μm [7]. However the increase of inter-metal dielectric thickness shows the negligible effects on the inductor Q.

Table 1. The quality factor of spiral inductors depends on the resistivity of substrate and fabrication process technology (Inter Metal Dielectric thickness of standard 0.8 μm CMOS technology was 1.1 μm).

Inductance (nH)	Quality Factor	Q/Q_{ref}	Technology to enhance Q
14.9	Q_{ref} = 1.8	1.0	Substrate res.: 5 Ω · cm
13.8	Q = 4.7	2.6	Substrate res.: 40 Ω · cm
13.1	Q = 6.4	3.6	Substrate res.: >2 KΩ · cm [1)]
13.2	Q = 6.7	3.7	1) + IMD Thickness 4.0 μm
13.2	Q = 9.1	5.1	1) + Metal Thickness 2.1 μm
13.2	Q = 12.9	7.2	1) + Metal Thickness 3.1 μm
Spiral Inductor: Double metal process, Inner diameter = 100 μm, Number of turns = 8, Line/Space =10 μm/2μm, @ f = 2.0 GHz			

These results confirm that employing the high resistivity substrate and thick metal technology is an efficient method for enhancing the Q of inductor, and the Q increases about 7.2 times larger than that of standard double metal CMOS technology.

2. Device Optimization for Maximum RF Performance

The RF and noise performance of MOSFET sensitively depends on the gate layout because the gate resistance affects the high frequency performance severely. So it is essential to analyze the optimal layout and bias condition of MOSFET for RF IC design. The RF performances of 0.8 μm CMOS devices, which have various unit finger width and number, have been analyzed to maximize resonance frequency (f_{max}) and to minimize minimum noise figure (F_{min}) [8].

Figure 3 shows the f_{max} performance of MOSFETs having various gate geometry. The each unit gate was connected with signle contact. The f_{max} increases with reducing unit gate width (W_U), but the increasing rate of the f_{max} decreases for 5 μm of W_U. This results show that the f_{max} is degraded by the narrow width effect of MOSFET below W_U of 10 μm. Therefore, W_U of about 10 μm seems to be the optimal width to obtain the high f_{max} for 0.8 μm polysilicon gate MOSFETs. The f_{max} of nM OSFET with W_U of 10 μm shows 17 GHz at the finger number of 2~6, and starts decreasing with the increase of gate finger numbers due to the increase of parasitic component and input

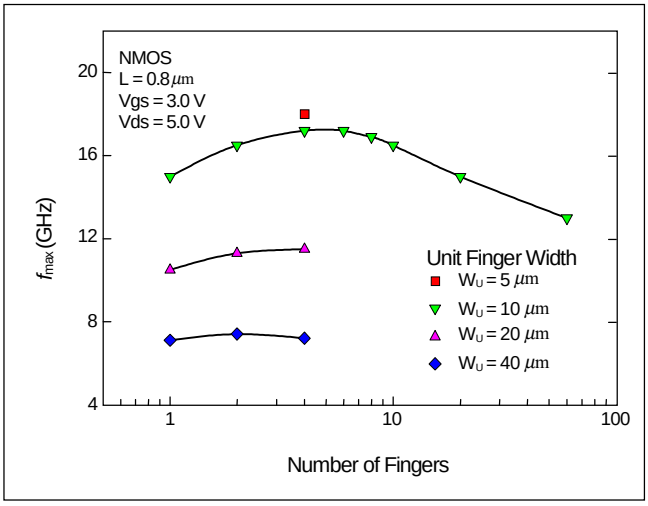

Fig. 3. Measured f_{max} for nMOSFET vs. number of gate finger with several gate width at Vds = 5.0 V and Vgs = 3.0 V. W_U is the unit width of a finger. Pad parasitic components was deembedded by open and short dummy pattern.

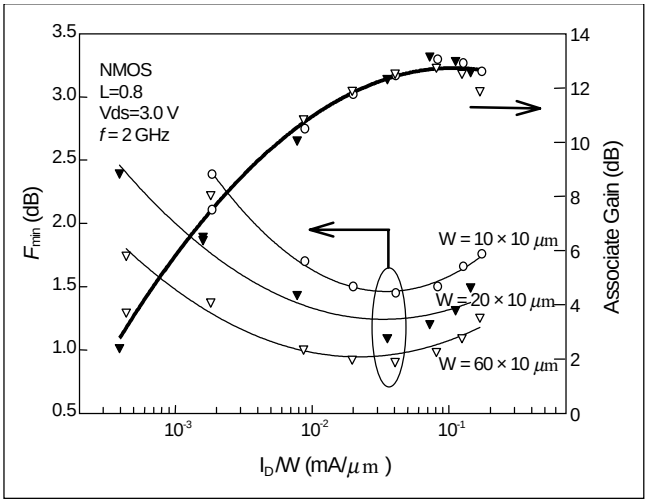

Fig. 4. F_{min} and associate gain vs. I_D/W for large width nMOSFET at Vds = 3.0 V.

signal dispersion of wide MOSFET [9]. So careful considerations should be taken in designing the device layout.

Figure 4 shows the plot of F_{min} and associate gain vs. drain current of large width MOSFET. At the frequency of 2 GHz, the F_{min} of nMOSFET with the channel width of 600 μm was found to be 0.91 dB at Vgs = 1.5 V with the associated gain of 12 dB. If design specifications of gain, noise, and power for RF amplifiers are given, Fig. 4 will be a useful design guide information for circuit designers.

The F_{min} dependency on bias conditions is also very important information to circuit designers. Figure 5 shows the F_{min} dependency of gate and drain bias voltage for channel width of 100 μm device. The gate voltage affects negligibly on F_{min} value at

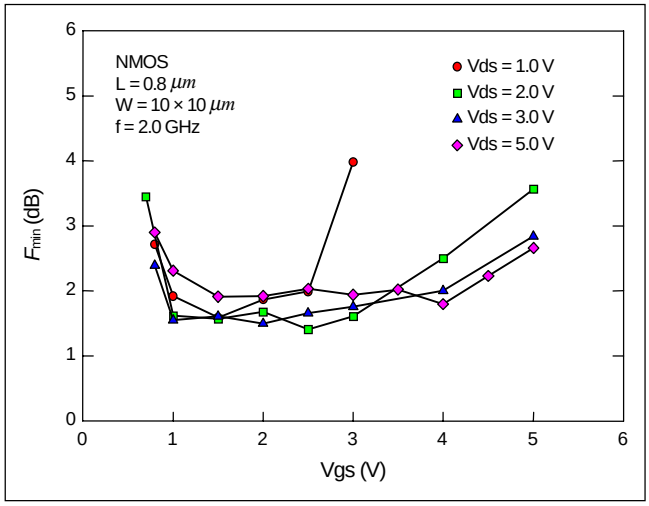

Fig. 5. Measured F_{min} for nMOSFET with the variation of Vgs and Vds at 2.0 GHz.

saturation (Vgs-V_T<Vds) bias conditions except near threshold voltage, which differ from the typical U-shaped F_{min}-I_D characteristics of MESFET or Bipolar devices. The drain bias dependency on F_{min} value was negligible at saturation bias conditions, but the value increases slightly at high drain voltage due to the excess thermal noise in short channel device [10].

From these results, we concluded that the 0.8 μm nMOS FET has the sufficiently high frequency performance and low noise characteristics for LNA and other RF ICs in the frequency range of 1~2 GHz.

III. *L*-BAND CMOS LNA DESIGN AND CHARACTERIZATION

The common source (C-S) with inductive source feedback type, which have been widely used for low noise performance [5], was adopted as input stage. Both the 900 MHz and 1.9 GHz LNA employed the same circuit type except in/out matching circuits as shown in Fig. 6. The layout optimized transistor M_1 with the channel width of 600 μm was adopted for low F_{min} and convenience in matching. The bias condition of the second-stage transistor M_2 was chosen for the high gain and linearity. Transistors M_3 and M_4 with 10 KΩ resistor R_b for ac blocking form the biasing circuitry. The 6.8 nH inductor L_g and 9 nH inductor L_o were used for input and output impedance match at 1.9 GHz, respectively. For a 900 MHz LNA, a 25.5 nH inductor L_g, which is about four times larger inductance compared with that of 1.9 GHz LNA, was used for input match to 50 Ω. The circuit performance was expected using Libra with measured s-parameters and noise parameters.

To analyze the effect of spiral inductors to the LNA noise performance, the *NF* of single stage common source amplifier

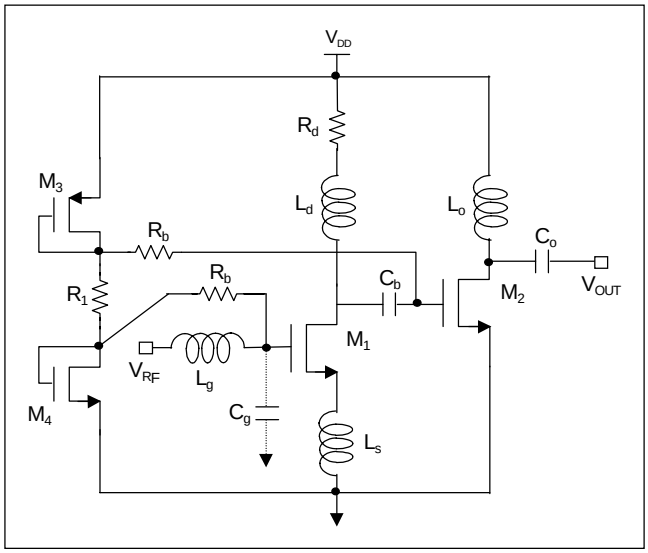

Fig. 6. Simplified schematic of the fully integrated 900 MHz and 1.9 GHz LNA. C_g is used only for 900 MHz circuit.

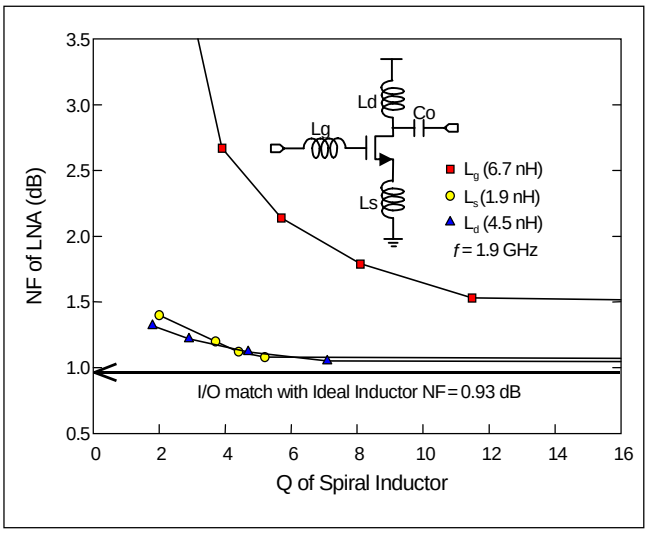

Fig. 7. Simulated noise figure of single stage LNA with the quality factor of spiral inductors.

was analyzed with the variation of inductor quality factor. The *NF* of fully integrated LNA severely depends on the quality factor of spiral inductors as shown in Fig. 7. Especially, the input gate inductor (L_g) affects the LNA noise performance dominantly compared with other inductors. The figure also shows that the Q value of more than 12 is needed for a fully integrated 1.9 GHz LNA with low noise performance. To achieve the high Q more than 12 in spiral inductor on high resistive substrate, the resistance of spiral inductor should be reduced. Therefore, thick metal CMOS technology on high resistive substrate was employed. For thick metal process, the second metal thickness was increased up to 3.1 μm, and the metal was removed by dry etch process with the photo-resistor/oxide multi-layer mask.

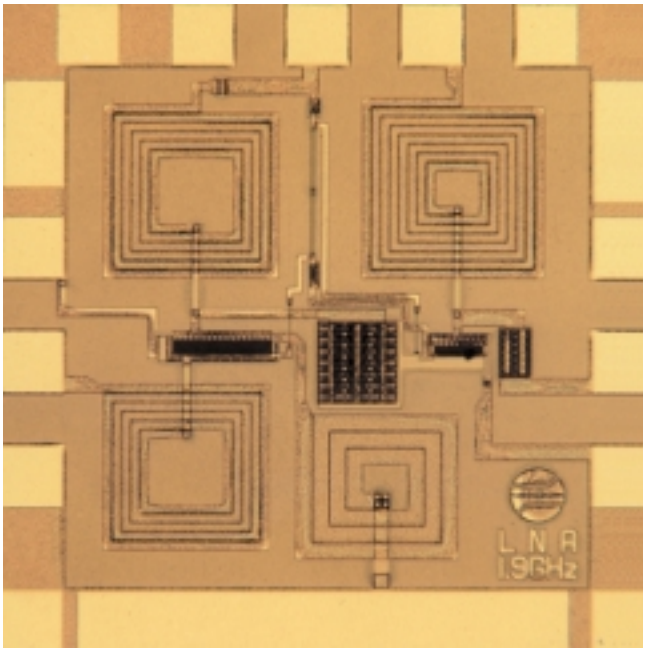

Fig. 8. Microphotograph of 1.9 GHz CMOS LNA fabricated with thick metal process. The chip size of the circuit was 0.93 mm × 0.93 mm

The LNA performance was measured in the frequency range of 0.5 ~ 10.5 GHz using on-wafer RF probes and a HP8510C Network Analyzer. Automated, on-wafer noise figures was also carried out in the 0.3 ~ 3 GHz range using an ATN setup. The performance of linearity was measured using signal source and spectrum analyzer.

1. Performance of the1.9 GHz LNA

Figure 8 shows the microphotograph of fully integrated 1.9 GHz LNA fabricated using the thick metal process with thickness of 3.1 μm. The chip size of the circuit was 0.93 mm × 0.93 mm. The spiral inductor with low inductance value shows a low Q value as shown in Fig. 2. So, a 1.9 nH inductor L_s was designed with wide metal width of 20 μm for high Q.

The measured gain and S_{11} of the 1.9 GHz amplifiers are shown in Fig. 9. The LNA-I and LNA-III represents the amplifier fabricated using standard metal thickness of 1.1μm and metal thickness of 3.1μm, respectively. The measured S_{11} of amplifiers show below –15 dB, and the gain of LNA-I and LNA-III is about 13.6 dB and 15.2 dB at the frequency of 1.85 GHz, respectively. These amplifiers show a good input VSWR at 1.85 GHz, but shows minimum output VSWR of about 1.3 at 1.65 GHz. Therefore maximum gain peak shows at the frequency of 1.7 GHz. The thick metal process enhances the gain of the LNA about 1.6 dB compared with conventional process due to reduction of inductor resistance. The sheet resistance reduced from 35 mΩ/sq to 10 mΩ/sq .

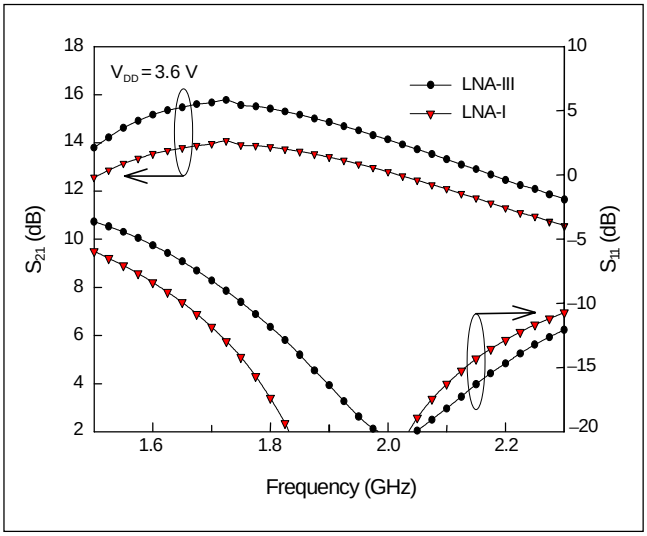

Fig. 9. Measured gain and S_{11} characteristics of 1.9 GHz CMOS amplifiers.

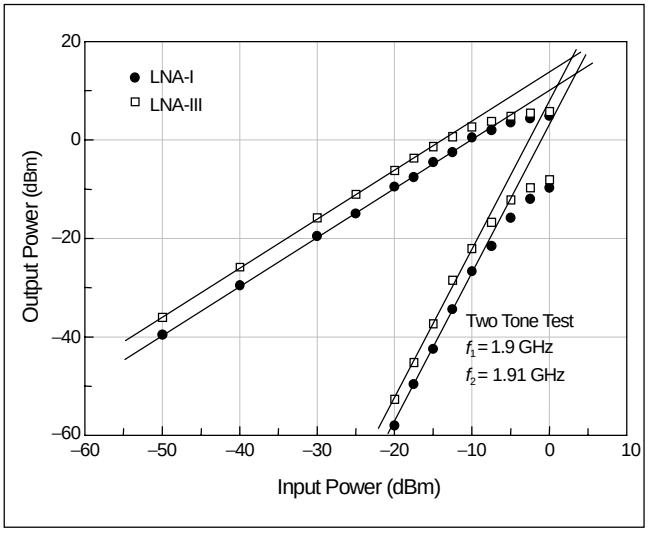

Fig. 11. Measured two-tone transfer characteristics of 1.9 GHz LNA-I and LNA-III.

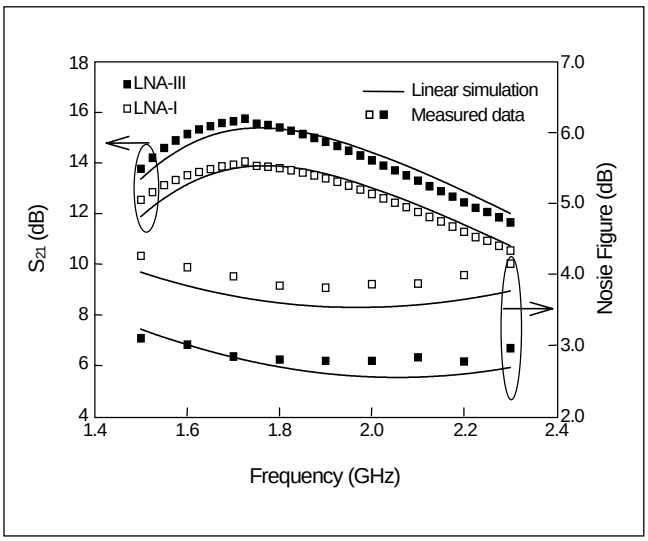

Fig. 10. Measured and simulated performance results of the 1.9 GHz LNA.

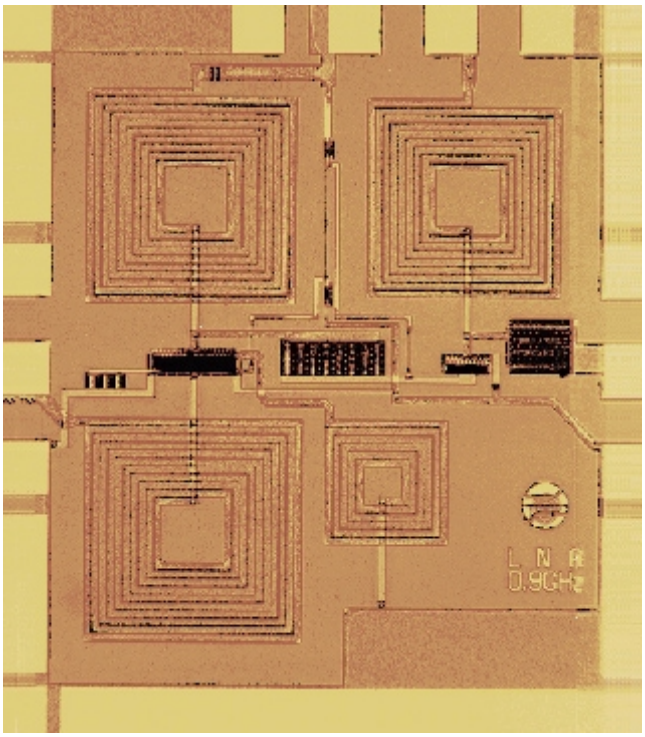

Fig. 12. Microphotograph of 900 MHz CMOS LNA fabricated with thick metal process. The four inductors and bias circuit was integrated in a chip that has the size of 1.1 mm × 1.2 mm

Figure 10 shows the noise figure of LNA-I and LNA-III. The noise figure of LNA-III was 2.8 dB at 1.85 GHz, and 1.04 dB was improved by using the thick metal process. Compared with other LNA that usually use the off-chip [2]–[4], [11], or bonding wire inductor [5], [12], [13], as input matching element, this monolithic 1.9 GHz LNA-III circuit shows the excellent noise figure [14]. Furthermore, Fig. 10 shows that an amplifier employing thick metal inductors can improve the *NF* up to 1.0 dB and gain by 2.0 dB compared with the one fabricated with the standard thin metal CMOS process. The noise performance of the LNAs can be expected accurately by the simulation using small signal parameters of active and passive devices.

Figure 11 shows two-tone transfer characteristics of LNA-III and LNA-I at 1.9 GHz. The LNA-III showed a measured –1dB input compression point of –10 dBm, and the measured third-order inter-modulation intercept point was 4 dBm referred at the input.

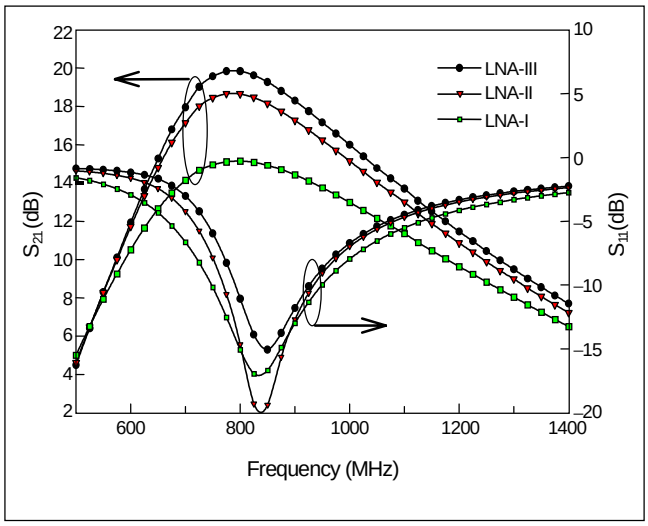

Fig. 13. Measured gain and S_{11} characteristics of 900 MHz CMOS amplifiers. LNA-I, and LNA-II and LNA-III represents the amplifier fabricated using the thick metal thickness of 1.1 μm, 2.1 μm and 3.1 μm, respectively.

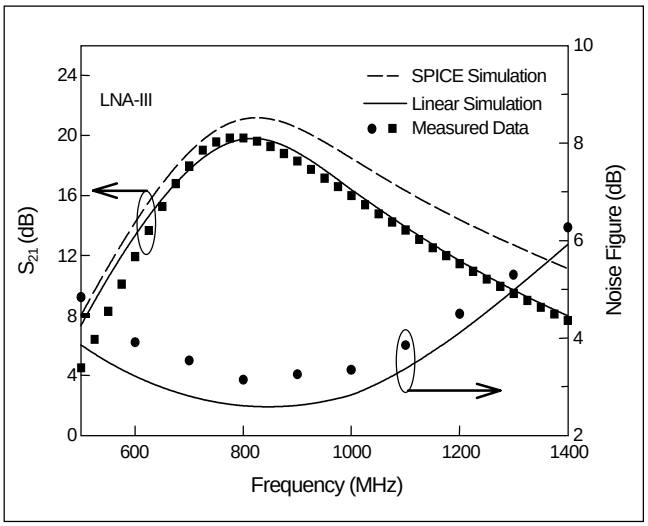

Fig. 15. Measured and simulated performance results of the LNA-III. Sold line and dotted line represent the linear simulation result using the Libra with measured data and the SPICE simulation result with our RF MOSFET model [15], respectively.

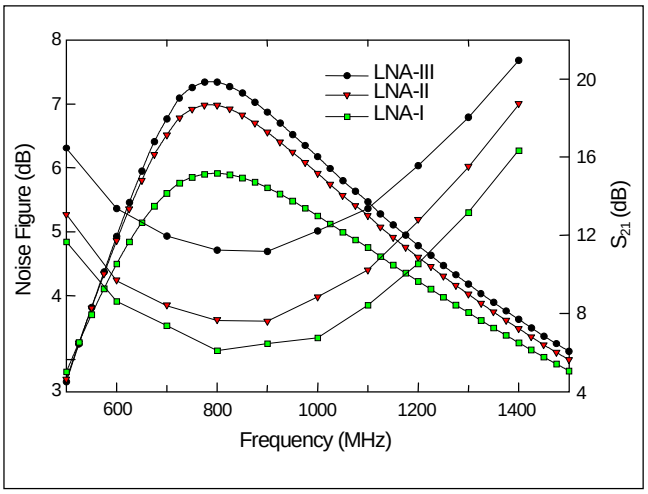

Fig. 14. Noise figure performance of LNA-I, LNA-II and LNA-III.

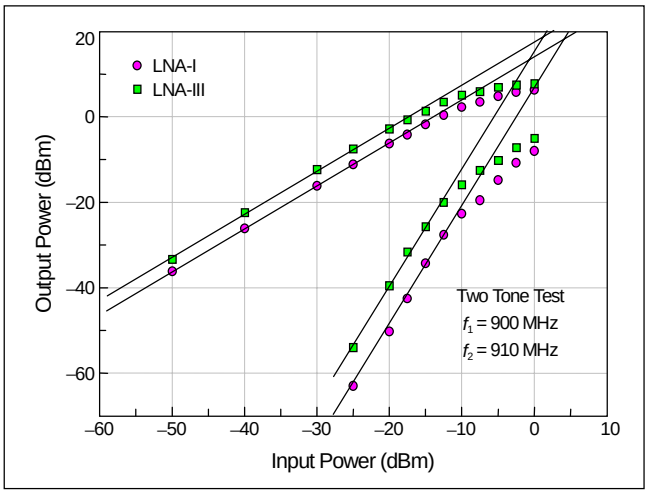

Fig. 16. Measured two-tone transfer characteristics of 900 MHz LNA-I and LNA-III.

2. Performance of the 900 MHz LNA

Figure 12 shows the microphotograph of fully integrated 900 MHz LNA fabricated using the RF CMOS technology. The chip size of the circuit was 1.1 mm × 1.2 mm. The measured gain and S_{11} of the 900 MHz amplifier is shown in Fig. 13. The LNA-I represents the amplifier fabricated using standard metal thickness of 1.1 μm, and LNA-II and LNA-III represents the amplifier fabricated using the thick metal thickness of 2.1μm and 3.1 μm, respectively. The measured S_{11} of all amplifier show a good input VSWR of about –15 dB, and the gain of LNA-I, LNA-II and LNA-III was about 15 dB, 18 dB and 19 dB at the frequency of 875 MHz, respectively. The LNA-III shows about 4 dB higher gain than that of LNA-I. The inductance value of spiral inductor was not the parameter of metal resistance, so the center frequency of matching condition of LNA-II or LNA-III was not moved. But the inductor resistance severely affects the LNA gain compared with 1.9 GHz LNA. These results can be explained by the fact that 2~3.8 times larger inductors were used in the 900 MHz LNA compared with that of 1.9 GHz LNA.

Figure 14 shows the noise figure of LNA-I, LNA-II and LNA-III. The noise figure of LNA-III was 3.25 dB at 875 MHz and about a 1.5 dB was improved by using the thick metal process. Figure 15 shows the measured and simulated

Table 2. Measured performance results of 900 MHz and 1.9 GHz LNA-III.

	V_{DD} (V)	Pwr. (mW)	Gain (dB)	S_{11} (dB)	S_{22} (dB)	*NF* (dB)	IIP_3 (dBm)
900 MHz LNA	3.6	54	19	–14	–5.4	3.3	1.0
1.9 GHz LNA	3.6	55	15	–16	–6.7	2.8	3.0

performance results of the LNA-III. The linear simulation result shows a good agreement with the measured results. The gain and *NF* of the LNA can be expected accurately by the simulation using small signal parameters of active and passive devices. But the simulation results with our model [15], which was developed for RF circuit simulation for SPICE, show that the gain of the circuit was about 2~3 dB higher than that of measured one. Figure 16 shows the two-tone transfer characteristics of LNA-III and LNA-I at 900 MHz. The LNA-III has a measured –1dB input compression point of –13 dBm, and the measured third-order inter-modulation intercept point was 1 dBm referred at the input.

The measured performance results of 900 MHz LNA and 1.9 GHz LNA are summarized in Table 2.

IV. CONCLUSIONS

RF CMOS technology was demonstrated for the *L*-band RF IC applications, and we successfully implemented it to the monolithic 900 MHz and 1.9 GHz CMOS LNAs. By employing the RF CMOS technology, the Q value of 13 nH inductor increases up to 12.9 which was about 7.2 times larger than that of standard double metal CMOS technology. The 1.9 GHz LNA shows a gain of 15.2 dB and a *NF* of 2.8 dB that is an excellent noise performance compared with the off-chip matched CMOS LNAs. The 900 MHz LNA shows a high gain of 19 dB and *NF* of 3.2 dB despite of the performance degradation due to the integation of a 26 nH inductor for input match. These results confirm that the proposed RF CMOS technology is a good candidate for *L*-band RF ICs.

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