Impact of LDD Structure on Single-Poly EEPROM Characteristics

Kee-Yeol Na, Mun-Woo Rho, Kyung-Hoon Kim, Nam-Soo Kim, and Yeong-Seuk Kim

Abstract

The impact of LDD structure on the single-poly EEPROMs is investigated in this paper. The single-poly EEPROMs are fabricated using the 0.8㎛ CMOS ASIC process. The single-poly EEPROMs with LDD structure have slower program and erase speeds, but the drain and gate stresses and the endurance characteristics of these devices are much better than those of the single-poly EEPROMs with single-drain structure. The single-poly EEPROMs with LDD structure do not require the process modifications and need no additional masks, hence can be used for microprocessors and logic circuits with low-density and low-cost embedded EEPROMs.

I. Introduction

There is a great demand for microprocessors and logic circuits with embedded EEPROMs. However, merging these two technologies, i.e., single-polysilicon logic and double-polysilicon EEPROM processes, leads to process complexities and hence yield degradation [1]. These problems can be overcome by utilizing the single-poly EEPROM techniques [2] - [4].

Since typical logic process used for the single-poly EEPROMs includes the lightly-doped drain (LDD) technology to avoid the hot carrier effects, it may not be beneficial for the program and erase of the single-poly EEPROMs. The LDD structure at the drain junction may decrease the lateral electric field and therefore degrades the efficiency of the channel-hot-electron (CHE) program of the single-poly EEPROMs. The LDD structure at the source junction also affects the Fowler-Nordheim Tunneling (FNT) erase characteristics.

In this paper we investigate the impact of LDD structure on the CHE program and FNT erase characteristics of the single-poly EEPROMs. We also discuss the drain and gate stresses and endurance characteristics of the single-poly EEPROMs. In section II, we describe the single-poly EEPROM cell structure and its process. In section III, the fabricated single-poly EEPROMs with different drain structures are characterized and compared.

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II. Cell Structure And Device Fabrication

A cross section of the single-poly EEPROM with LDD structure is shown in Fig. 1. Both source and drain junctions of n-channel MOSFET have lightly doped n^--regions by the LDD process. The p^+- and n^+-doped layers in the n-well are used for the control gate. The polysilicon layer which overlaps between the n-channel MOSFET and the control gate is used for the floating gate. The channel length and width of this cell are 0.8㎛ and 1.4㎛, respectively. The p^+-doped layer in the n-well is implemented by the following reason. Because the floating gate potential is lower than the control gate potential during programming, the n-well under the floating gate is inverted so that the p^+-doped layer in the n-well enhances the coupling ratio. On the other hand the single-poly EEPROM cell with the n^+-doped layer in the n-well has higher coupling ratio during the FNT erase.

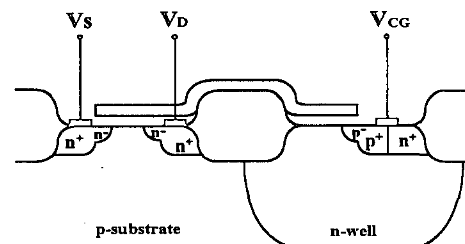

Fig. 1. A Cross section of the single-poly EEPROM with LDD structure.

For the programming of this cell the CHE or FNT method can be used. But in case of typical CMOS logic process the junction breakdown voltage between n^+-doped layer and p-substrate is about 14V. The FNT programming voltage limited by this junction breakdown is too low to be used for programming the cell. Therefore the CHE method is used for the programming of this cell. For the erasing of this cell the source side FNT method is used.

The single-poly EEPROMs are fabricated by using a 0.8μm CMOS ASIC process. This process includes self-aligned twin-well structure, LOCOS isolation, 155 Å gate oxide, WSi_2 single-polysilicon gate, LDD structure, and double layers of metal. The starting wafer is p-type substrate with (100) -orientation and 9-12 ohm-cm resistivity. First the n-well used for the control gate of the single-poly EEPROMs is formed. Following the LOCOS isolation the gate oxide and control gate oxide are simultaneously grown. After that, the polysilicon is deposited, doped by $POCl_3$ gas, and defined for the formation of the floating gate

To investigate the impact of LDD structure on the program and erase characteristics of the single-poly EEPROMs, the source and drain formation steps are splitted into two groups. One group is processed without any process modifications for the LDD devices. For the other group, LDD TEOS deposition, LDD spacer etch, and LDD annealing steps are skipped to make the single-drain (SD) devices.

III. Results and Discussions

The single-poly EEPROMs fabricated by the technique described in section II are characterized by using an HP4155A semiconductor parameter analyzer, an HP8160A pulse generator, and a switching matrix. Especially the single-poly EEPROMs with different drain structures are analyzed and compared. The measured data in Fig. 3 - 7 show some variations depending on die location in the wafer. The one-shot programming characteristics of the single-poly EEPROMs with LDD and SD structures are shown in Fig. 2.

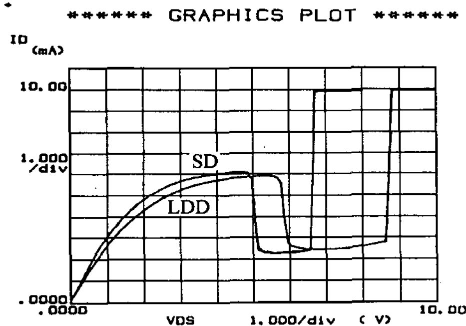

Fig. 2. One-shot programming characteristics of the single-poly EEPROMs with LDD and SD structures (V_{CG}=12V, V_S=0V).

In the triode and saturation regions before the program of the cell, the SD devices have more channel current than the LDD devices. The reason is that the SD devices have shorter effective channel length. due to elimination of lightly doped region. The LDD devices are programmed at the drain voltage of about 5.8V and break down at the drain voltage of about 8.7V. However, the SD devices are programmed at the drain voltage of about 5.0V and break down at the drain voltage of about 6.7V. The SD devices show CHE program at lower drain voltage but at the expense of lower drain breakdown voltage. The reasons for this are two folds: (1) the SD devices have higher lateral electric field near the drain junction due to absence of lightly doped n^--doped layer, and (2) the SD devices have higher channel current as mentioned above.

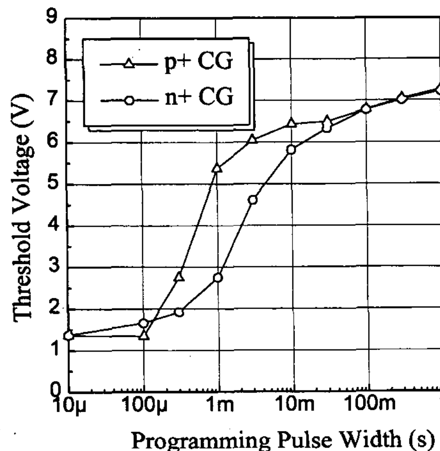

Fig. 3 (a). CHE programming characteristics with different control gate structures (VCG=12V, VS=0V, LDD).

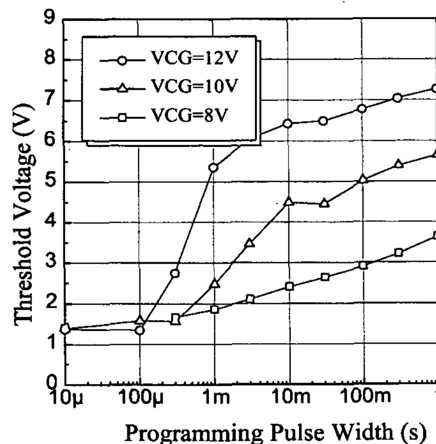

Fig. 3 (b). CHE programming characteristics with different control gate voltages (VD=7V, VS=0V, LDD).

In Fig. 3(a), we show the CHE programming characteristics of the single-poly EEPROMs with different control gate structures. The cells with the p^+-doped control gate (no n^+-doped layer in the n-well) show about 3 times faster CHE programming characteristics than the cells with the n^+-doped control gate (no p^+-doped layer in the n-well). This is due to the following reason: the floating gate potential is lower than the control gate potential during programming, thus the n-well under the floating gate is inverted so that the cell with the p^+-doped control gate have higher coupling ratio. Fig. 3(b) shows the CHE programming characteristics of the single-poly EEPROMs with different control gate voltages. The cells with V_{CG}=12V have faster CHE programming characteristics as well as higher V_T shift than the cells with V_{CG}=8V, 10V. Higher control gate voltages result in higher floating gate voltage, which enhances the CHE injection efficiency.

The CHE programming characteristics of the single-poly EEPROMs are compared between two different drain structures as shown in Fig. 4. The SD devices show over 100 times faster CHE programming speed than the LDD devices. The threshold voltage of 5V can be achieved with 1ms and 300ms programming pulse for the SD devices and the LDD devices, respectively. But as we increase the drain voltage we obtain about same programming speed as shown in Fig. 4. To get V_T of more than 5V with programming pulse of 10ms, V_{DS}=6V for the SD devices and V_{DS}=8V for the LDD devices are required as shown in this figure. The LDD devices require more drain voltage due to lower horizontal electric field near the drain junction. But the fabrication of the LDD devices is simpler than that of the SD devices. Typical CMOS logic process usually includes LDD formation step to avoid the hot carrier effects, so that eliminating this step to make the SD devices is cumbersome. Note that the SD devices can be done by eliminating n^-/p^- photolithography, ion implantation, TEOS oxide deposition, and LDD spacer etching steps.

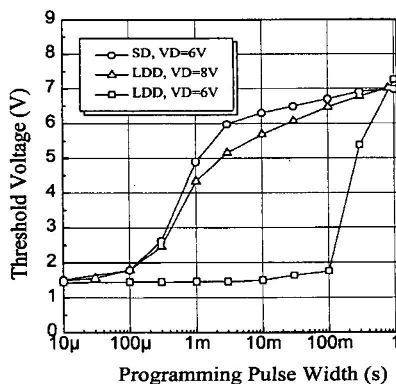

Fig. 4. CHE programming characteristics of the single-poly EEPROMs with LDD and SD structures.

The FNT erase characteristics of the single-poly EEPROMs with both SD and LDD structures are shown in Fig. 5. The source voltage is lower than the junction breakdown voltage, 14V, so that the erase speed is slower than that of typical double-poly EEPROMs. The initial threshold voltages are adjusted to 7V before the erase of the cell. The LDD devices show slower erase time compared to the SD devices because the LDD devices have less Fowler-Nordheim tunneling current due to the lightly doped source region and smaller overlap area beneath the floating gate.

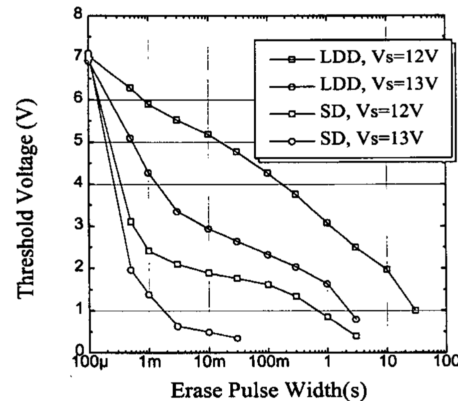

Fig. 5. Erase characteristics of the single-poly EEPROMs with LDD and SD structures.

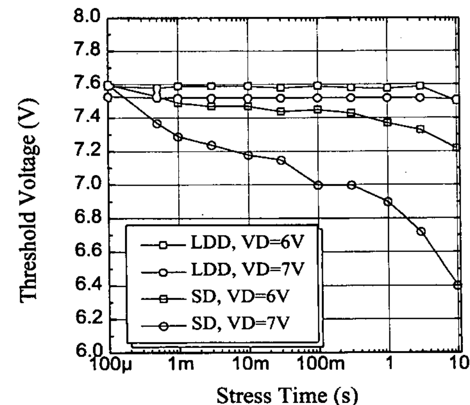

Fig. 6 (a). Drain disturb characteristics of the single-poly EEPROMs with LDD and SD structures.

Fig. 6(a) and (b) show the drain and gate disturb characteristics, respectively. For the drain disturb measurements, the control gate is grounded while the drain is biased normally as the programming mode. The LDD devices show less drain disturb characteristics even though the drain voltage is increased to 7V to speed up the program time. For the gate disturb measurements, the drain is biased to ground while the control gate is biased positively. Both drain and gate disturb characteristics show that the SD devices have more severe

disturb characteristics than the LDD devices. The reason is as follows: in case of the SD devices the electric field near the drain is large, so resulting in more stresses. The LDD devices are less immune from the drain and gate disturbs.

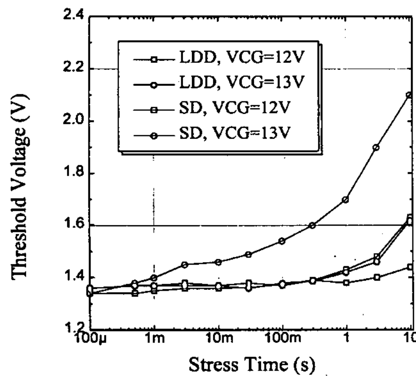

Fig. 6 (b). Gate disturb characteristics of the single-poly EEPROMs with LDD and SD structures.

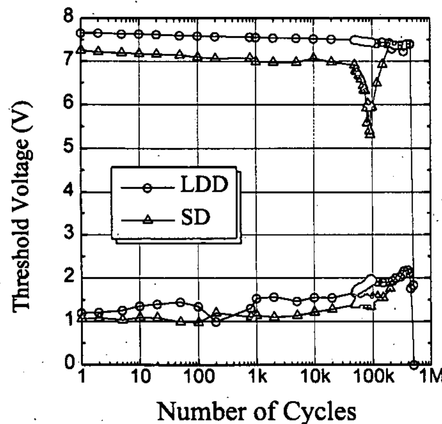

Fig. 7. Single cell endurance characteristics of the LDD and SD devices.

Finally the endurance characteristics of the single-poly EEPROMs with LDD and SD structures are compared as shown in Fig. 7. Both devices show little threshold voltage window opening (no hole traps) initially. As program and erase cycling goes on, the SD devices have a window closing due to electron traps at about 5×10^4 cycles, but the LDD devices show no window closing up to 5×10^5 cycles. The endurance characteristics of the LDD devices are about 10 times better than those of the SD devices. We believe that the LDD devices have better endurance characteristics due to smaller lateral electric field near the drain by the LDD technique. As shown in Fig. 4 - 7, the LDD devices have slow program and erase speeds, but show better reliabilities than the SD devices. These intrinsic characteristics of the single-poly EEPROMs with LDD structure are useful for low-density and low-cost applications which do not require fast speeds but good reliabilities.

IV. Summary

The single-poly EEPROMs with SD and LDD structures were fabricated using the 0.8㎛ CMOS ASIC process. We investigated the impact of LDD structure on the CHE program and FNT erase of the single-poly EEPROMs. The CHE program and FNT erase speeds of the LDD devices are slower than those of the SD devices. The smaller electric field near the drain for the LDD devices may cause this slower speeds, but its speed can be compensated by applying higher drain voltage. The drain and gate stresses as well as the endurance characteristics for the LDD devices show much better reliabilities than those for the SD devices. Therefore the LDD structure is more beneficial to the single-poly EEPROMs. This shows that the single-poly EEPROMs with LDD structure without changing any mask steps or processes can be used for microprocessors and many kinds of logic circuits which require low density embedded EEPROMs.

Acknowledgment

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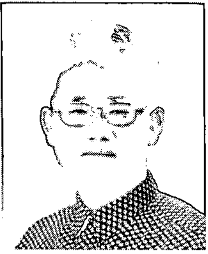

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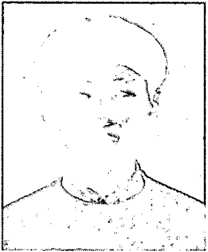

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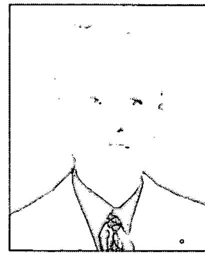

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