Design of Compact and Efficient Interleaved Active Clamp ZVS Forward Converter for Modular Power Processor in Distributed Power System

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Abstract

A high efficiency interleaved active clamp forward converter with self driven synchronous rectifiers for a modular power processor is presented. To simplify the gate drive circuits, N-P MOSFETs coupled active clamp method is used. An efficiency about 90% for the load range of 50-100% is achieved. The details of design for the power stage and current mode control circuit are provided, and also some experimental results are given.

I. Introduction

The modular power processor in a distributed power system such as computer and telecommunication will require a tighter supply voltage, high power, and lower voltage. To meet these demands, a distributed power system, in which an input power converter provides a regulated 48VDC bus with the final low voltage power processing performed directly on each of the logic cards, is the most logical alternative. Thus, design requirements call for a 5VDC, 200W module with a low profile, high power density, and high efficiency greater than 90% [1-3].

The efficiencies for 200W, 5VDC output converters with power density of 50W/in^3 (3.05W/cm^3) are reported in the range of 82%-85% [1-2]. The major factor limiting the efficiency is the power loss in the Schottky rectifier. Thus, to improve the efficiency above 85%, the power MOSFETs could be used as synchronous rectifiers[2-5]. However, the control complexity and driving losses are usually the main constraints in this scheme. Most of these problems are solved by using the self-driven synchronous rectification in a very efficient way in the active clamp forward topology [5].

The paralleling of power stage is well known technique often used in high power applications to achieve the desired output power with smaller size power transformers and inductors. In addition to physically distributing the magnetics, paralleling also distributes the power losses and thermal stresses of the semiconductors. Therefore, lower power and fast semiconductor switches can be used besides low-profile transformers. For an interleaved configuration, the input and output current ripples are greatly reduced because the paralleled power stages are operated with 180° out of phase. Consequently, an interleaved configuration offers an opportunity to reduce the size of input and output filters.

This paper presents a design of interleaved active clamp ZVS forward converter for a modular power processor in a distributed power system aimed at achieving high efficiency with compact size. It utilizes the pulse width modulation (PWM) at a constant frequency of 500kHz(1MHz input/output ripple frequency) and zero voltage switching (ZVS). To simplify the MOSFETs gate drive circuits, N-P MOSFETs coupled active clamp method is used. Thus the relatively complexity and power losses of gate driver circuits are reduced. The design details of power stages, controller, low-profile transformer, and self-driven synchronous rectifier are described. A breadboarded interleaved active clamp ZVS forward converter has been built, and some experimental results have been measured.

II. Overview of an Interleaved N-P MOSFETs Coupled Active Clamp ZVS Forward Converter

The forward converter has been widely used for a low-to-medium power conversion. To reset the power transformer, the active clamp method has been chosen, which provides the higher efficiency than other methods [6]. By making the magnetizing inductance resonate with MOSFET's output capacitance, the active clamp forward converter can be designed to operate with ZVS for the active devices. Fig. 1 shows the circuit diagram of an interleaved ZVS active clamp forward converter. As can be seen in Fig. 1, the interleaved forward circuit consist of two identical section. For convenience, one-half of the circuit and key waveforms are shown in Fig. 2. The clamp switch, Q_2, is used to provide a path for recycling the transformer magnetizing energy in a lossless manner. This provides optimal reset of the transformer as well as reduced switching loss. Under steady-state operation, seven stages are identified within each switching cycle, as shown in Fig. 3. During the transient intervals T_2-T_3 and T_5-T_6, the MOSFET output capacitor, Cs, is respectively charged and discharged by the magnetizing current, due to the resonance between Cs and the magnetizing inductance, Lm.
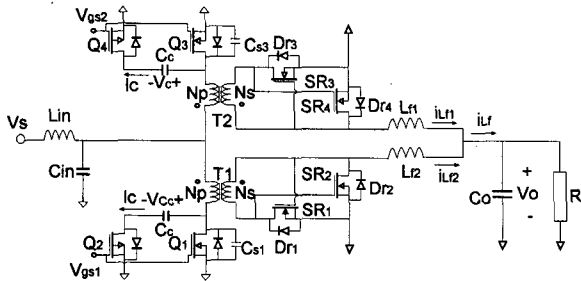

Fig. 1. Circuit diagram of an interleaved active clamp forward converter with synchronous rectifier configuration

The output voltage of the forward converter is given by:

$$V_o = \frac{V_s \cdot D}{N},$$ (1)

where N=Np/Ns is the transformer turns ratio, and D is the duty cycle. According to the volt-second balance on the transformer:

$$V_s \cdot D = (V_c - V_s) \cdot (1 - D),$$ (2)

the voltage across the clamp capacitor is

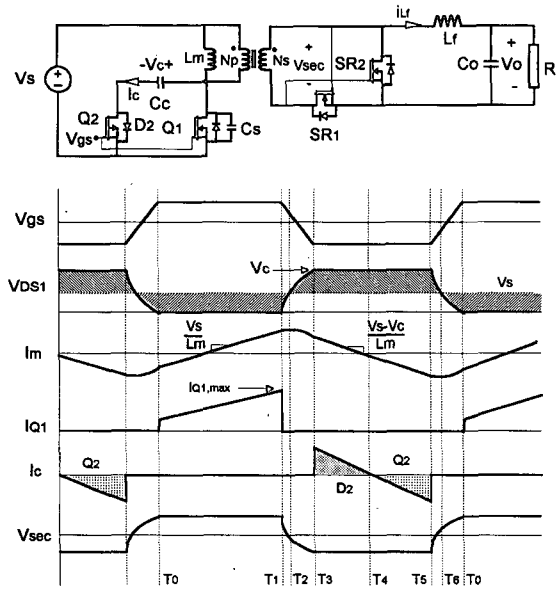$$V_c = \frac{V_o \cdot N}{D(1 - D)}.$$ (3)

Fig. 2. Circuit diagram and key waveforms of active clamp ZVS forward converter
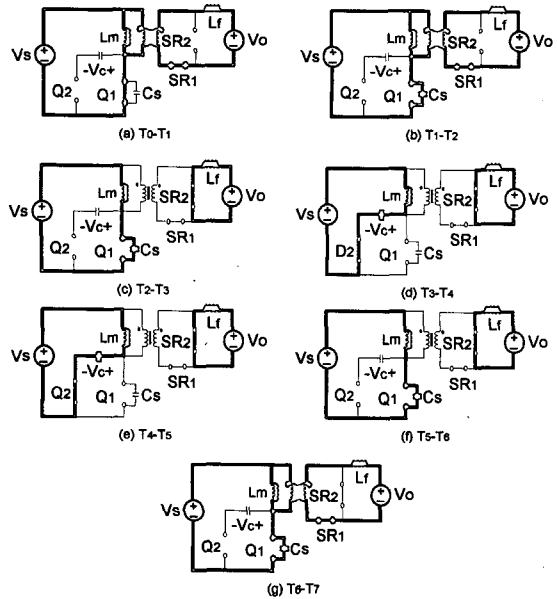

Fig. 3. Equivalent circuit for different operating stages of active clamp ZVS forward converter

The clamp voltage increases as the input voltage increases and the duty cycle increases, and vice versa. Thus, the maximum switch voltage stress, which is equal to the voltage across the clamp capacitor, tend to remain approximately constant over the whole range of the input voltage. In addition, due to the charge balance of the clamp capacitor, the flux of the transformer is symmetrical operated in the first

and the third quadrant. Therefore, this topology features the most efficient utilization of the magnetics [6].

The peak voltage stress of Q_1, Q_2, SR_1, and SR_2 is respectively given by

$$V_{DS1}\max = V_{DS2}\max = V_C = \frac{V_o \cdot N}{D(1-D)}, \qquad (4)$$

$$V_{SR1}\max = \frac{(V_C - V_S)_{max}}{N}, \text{ and } V_{SR2}\max = \frac{V_{Smax}}{N}. \qquad (5)$$

The peak current stress of Q_1 is

$$I_{Q1}\max = \frac{I_{Lf1, max}}{N} \qquad (6)$$

With a current mode control, the active clamp forward topology features the lowest voltage stress on the main switch, constant frequency operation, and current sharing capability. There is one more important advantage that the voltage in the transformer secondary winding is very useful for a self-driven synchronous rectification. Furthermore, its design is as simple as any PWM converter. The interleaved configuration shown in Fig. 1 allows the circuit to maintain the regulation with an overlap(low line) or underlap(high line) in the conduction of Q_1 and Q_2. The turns ratios of T_1 and T_2 are chosen such that at nominal line voltage and full load operation the duty cycle of Q_1 and Q_3 will be about 50%. The AC component of the current flowing through L_{Lf1} will be equal in amplitude and opposite in phase to that in L_{f2}, and the idealized output current $i_{Lf1} + i_{Lf2}$ will be pure DC. As the duty cycle moves away from the ideal 50% point, a double frequency AC component is going to build up. Therefore, the weight and size of the output filter can be significantly reduced. Moreover, this AC cancellation also occurs at the input section. As a result, this configuration makes the input and output filters more compact.

At high switching frequencies, the most suitable device to substitute a diode in the output rectification stage is a power MOSFET. In this way, the almost constant diode voltage drop can be substituted by a resistance type voltage drop. As a result, more improved overall efficiency can be obtained by using the self-driven synchronous rectifier.

In a conventional active clamp forward converter, the pulse transformers and high current IC driver chips are required to drive the clamp switches. These increase the circuit complexity and result in power losses. Furthermore, the leakage inductance of the pulse transformer and the gate-to-source input capacitance of a MOSFET can create an oscillation. Unfortunately, this results in an undesirable gate-to-source voltage. In this paper, to prevent a set of these circumstances, a P-channel MOSFET is used for the clamp switch. The gate terminals of main and clamp switches can be connected as shown in Fig. 2. Thus, the direct drive from

a PWM control chip is attained, which results in simplified MOSFETs gate drive circuits without adverse parasitic ringings.

III. Power Stage Design Considerations

The basic design requirements for interleaved active clamp ZVS forward converter are summarized as follows:

     Input voltage range: 44-52VDC (Nominal voltage: 48VDC)

     Output voltage: 5VDC

     Maximum output current: 40A

     Efficiency: about 90%

     Power density: $40W/in^3$ ($2.44W/cm^3$)

     Height: 1.3cm

     The design of the power stage and steady-state analysis are carried out in detail in the followings.

1. Switching frequency

The effect of switching frequency on the power converter operation is severe. A higher frequency will reduce the size of the capacitor, inductor, and transformer but increase the core loss and switching loss. The switching frequency of f_s=500kHz for the experimental breadboard circuit has been chosen, which yields both an input and an output ripple frequency of f_{ripple}=1MHz.

2. Duty cycle range

Since the active clamp method is employed to reset the power transformer and two PWM control chips are used to control each power stage without load unbalance, the duty cycle can be increased beyond 50%. This high duty cycle tends to reduce the current stress on the main switch while increasing the voltage stress. With a turns ratio of 5 to 1, the maximum duty cycle is 70%. Since the maximum input voltage is 52V, the minimum duty cycle is about 50%.

3. Selection of switches and synchronous rectifier

From equations (3)-(4), the calculated peak voltage stress on the main switches is about 120V. For Q_1 and Q_3 MOSFETs with a drain-source breakdown voltage of $BV_{DSS} = 200V$, a minimal drain-source on-state resistance R_{DSon} should be selected. A good choice is the *IRFP640* from International Rectifier (IR), which has $BV_{DSS} = 200V$, $R_{DSon} = 0.18 \Omega$, and $I_{Dmax} = 18A$.

The use of a P-channel MOSFET as a clamp switch makes a gate drive circuit simple with enhanced circuit performances. Therefore, the choice of clamp switches Q_2 and Q_4 becomes less critical, as the clamp switch carries only a

small magnetizing current. The IRF9640($BV_{DSS} = 200V$, $R_{DSon} = 0.5\Omega$, $I_{Dmax} = 11A$) is selected for Q_2 and Q_4. In order to improve the efficiency of the converter, the synchronous rectifiers are added in parallel with the Schottky diodes. For synchronous rectifiers, SMP60N03($R_{DSon} = 10m\Omega$) is used and the efficiency improvement is about 4%.

4. Transformer design

Transformer turns ratio can be determined by transformer voltage and duty ratio as

$$N = \frac{[V_{s,min} - V_{x,max}]}{[V_{o,max} + V_{SR,max} + V_{Lf}]} \cdot D_{max}, \qquad (7)$$

where $V_{x,max}$ and $V_{SR,max}$ are maximum voltage across the transformer and maximum voltage across the synchronous rectifier, respectively. Using equation (7), N=5 is obtained. The secondary is designed for excellent coupling using copper foil, and the primary has been rounded to nearest lower turns. One half of PQ2620 from TDK core PC50 is selected for the transformer core to easily terminate the high current output winding.

The most difficult task in high frequency magnetic design is to minimize the eddy current losses, or skin effect while optimizing wire size. Thus, an interleaved winding approach is employed to minimize the proximity effect. The optimal diameter of the primary wire is determined by the skin depth, d_{pen}, for copper at $100°C$ as [7]:

$$d_{pen} = 7.5/frequency^{0.5} \ [cm] \qquad (8)$$

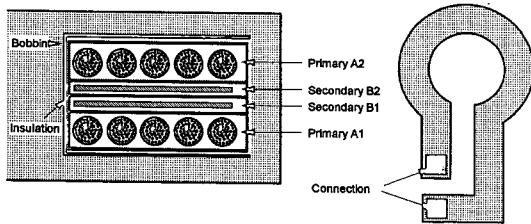At 500kHz, this corresponds to $10.6 \cdot 10^{-3}$ cm, or about thickness AWG #38 wire.

Fig. 4. Exploded view of transformer and configuration of secondary winding

Standard practice to increase coupling between primary and secondary is position both as closely as possible to each other inside the transformer. In order to fill the whole length of the bobbin with the interleaved primary and secondary layers, 2 layers with 5 turns, 75 strands of AWG38 wire are used for the primary winding. The secondary winding is implemented with a copper foil. The primary A1 is wound closest to the bobbin. After insulation, secondary B1 is wound and insulated. Secondary B2 is wound and insulated. primary A2

is wound last, then terminated so that primaries A1 and A2 are wired, likewise for secondary B1 and B2. This interleave winding method and configuration of secondary winding are shown in Fig. 4.

Given the core material type, geometry, frequency, operating Gauss level, ferrite losses can be calculated. From the manufactures information, the typical loss coefficient for PC50 material operating at a flux density swing of 500 [Gauss] at 500kHz is $0.08W/cm^3$. Therefore, the total power loss is summation of the copper and ferrite losses as

$$P_{x,loss} = P_{cop,loss} + P_{core,loss} = 1.51W.$$

5. Clamp capacitor

The resonant frequency formed by the clamp capacitor and the resonant inductor should be sufficiently low so that there is not excessive resonant ringing across the power switch when the switch is turned off. However, using too large a value of clamp capacitance yields no improvement in clamping performance at the expense of a larger capacitor. A good compromise for design purposes is to select the capacitor value so that one-half of the resonant inductance exceeds the maximum off time of main switch. Therefore, the clamp capacitance is designed as

$$C_c \gg \frac{(1-D)^2}{\pi^2 \cdot L_m \cdot f_s^2}. \qquad (9)$$

The clamp capacitor is implemented by a 500nF, 400V metalized polyester capacitor.

6. Output inductor

Since the interleaved technique is used, the ripple of the output current $i_{Lf1} + i_{Lf2}$ can be significantly reduced. The peak-to-peak ripple currents become:

$$\Delta i_{Lf1} = \Delta i_{Lf2} = \frac{(1-D)V_o}{L_{f1} \cdot f_s} \qquad (10)$$

where Δi_{Lf1} and Δi_{Lf2} are output current ripples, and

$$\Delta(i_{Lf1} + i_{Lf2}) = \Delta i_{Lf1} + \Delta i_{Lf2} = \frac{(D-0.5)V_o}{L_{f1} \cdot f_s} = \frac{D-0.5}{1-D} \cdot \Delta i_{Lf1} \qquad (11)$$

From(11), $\Delta(i_{Lf1} + i_{Lf2})_{max} = 0.667 \cdot \Delta i_{Lf1}.max$. The output inductor is implemented with the modified EI core, which yields $L = 0.5\mu H$ at 20A current level.

IV. Design of Controller and Gate Driver Circuit

The schematic of the controller is shown in Fig. 5. The controller is based on the integrated high speed PWM controller chip UC3823 from Unitrode [7]. This controller

consists of PWM circuit, external oscillator, and out of phase clock generator.
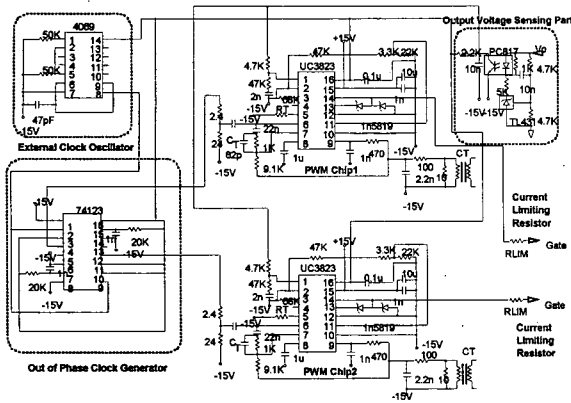

Fig. 5. Controller schematic ᵥ

With two power stages operating out of phase, the internal oscillator is not used. An external oscillator is formed by two NAND gates of 7400. A multivibrator of 74123 is used to limit the maximum duty cycle at low line and full load operating conditions to prevent the core from saturation. The output of each one-shot circuit is used as a clock signal of the individual PWM controller.
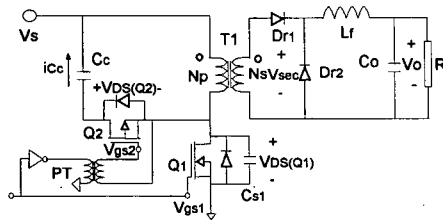

Fig. 6. Gate drive circuit of conventional active clamp forward converter
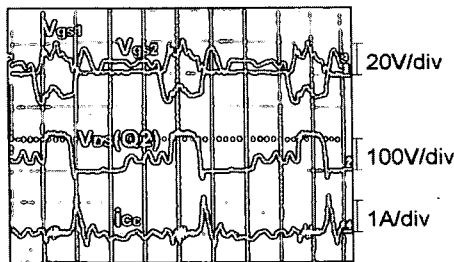
Fig. 7. Undesirable waveforms of clamp switch of conventional active clamp forward converter when duty cycle is 0.3

As can be seen in Fig. 6, the conventional active clamp

forward converter has to use the pulse transformer(PT) and high-current IC driver chips to drive the clamp switches. These increase the circuit complexity and result in power losses. Furthermore, the leakage inductance of the pulse transformer and the gate-to-source input capacitance of a MOSFET can create an oscillation. Unfortunately, this results in an undesirable gate-to-source voltage especially in case of lower duty cycle. These problems are shown in Fig. 7.

The high current totem-pole outputs of PWM controller chip UC3823 have greatly enhanced and simplified the MOSFET gate drive circuit. Since the N-P MOSFETs coupled active clamp technique is used, the gates of the main and clamp switches are connected. Thus, the fast switching time can be attained with a direct drive from UC3823. Also, frequently overlooked, two external components, i.e., the series gate current limiting resistor and Schottky diodes are required to insure a proper operation of PWM while delivering the high current drive pulses. The delay time between the control pulses of main and clamp switches is adjusted with the delay circuit which consists of the series gate current limiting resistor and input capacitances of MOSFETs switch. The operation of the delay circuit is shown in Fig. 8. During Δt_1 and Δt_2, the main and clamp switches are turned off because the applied gate-source voltages are smaller than their threshold turn-on voltages. Thus, the delay time can be adjusted with the gate current limiting resistor to insure proper ZVS operations. Thus the undesirable problems of conventional active clamp forward converter are eliminated as shown in Fig. 9.
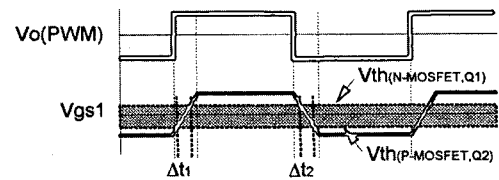

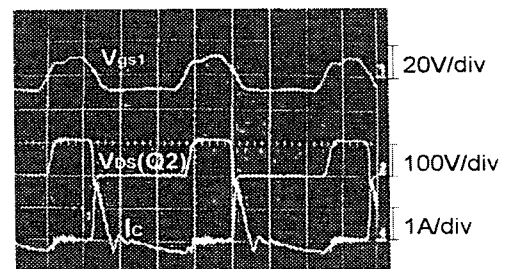**Fig. 8.** Operation of delay circuit

Fig. 9. Experimental waveforms of clamp switch of N-P MOSFETs coupled active clamp forward converter when duty cycle is 0.3

V. Experimental Results

Fig. 10 shows the peak voltages of main switch and clamp capacitor, the peak and rms currents in a main switch, and output voltage ripples of an interleaved ZVS active clamp forward converter as a function of source voltage and load.
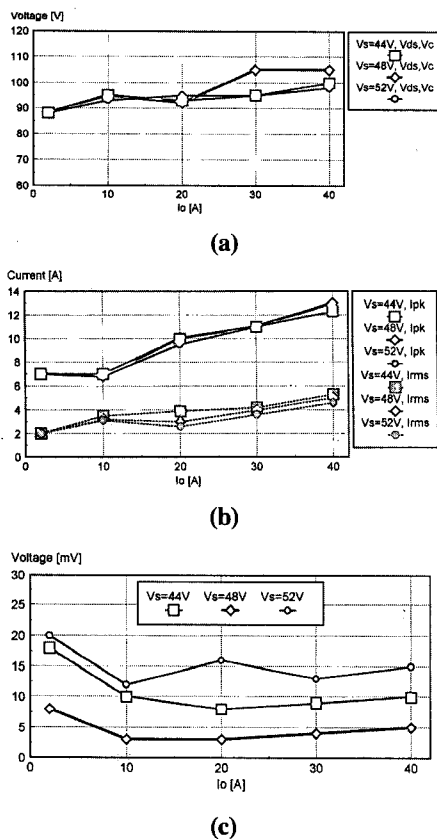

(a)

(b)

(c)

Fig. 10. Peak voltage in a main switch and clamp capacitor (a), peak and rms currents in a main switch (b), and output voltage ripples (c), of an interleaved active clamp ZVS forward converter as function of source voltage and load
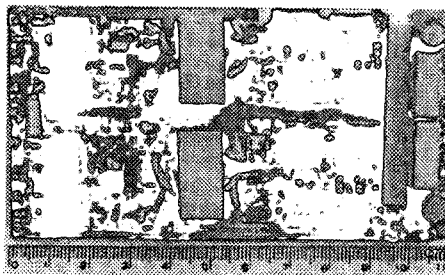

Fig. 11. Photograph of the power stage

Fig. 11 shows a photograph of the power stage. It satisfies the required power density with size of (W: 11.3cm x L: 7.6cm x H: 1.3cm). The experimental waveforms of the gate-source voltage, drain-source voltage, transformer secondary voltage as well as the drain current of the main switch are presented in Fig. 12. This figure also shows the clamp capacitor current and output current.
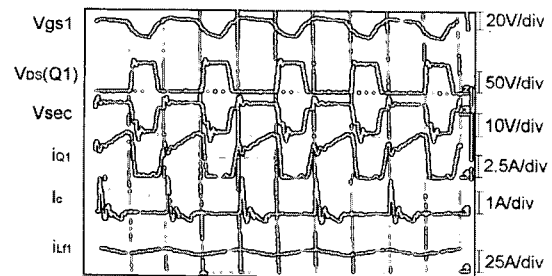
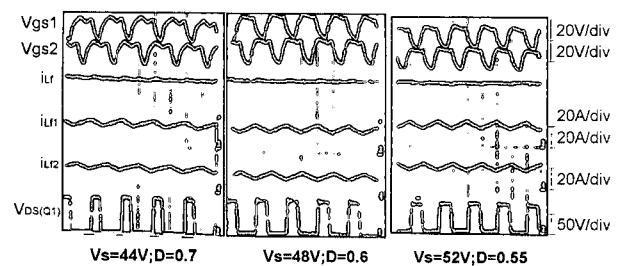

Fig. 12. Key experimental waveforms

| Vs=44V;D=0.7 | Vs=48V;D=0.6 | Vs=52V;D=0.55 |

Fig. 13. Measured key waveforms for different source voltage at full load condition
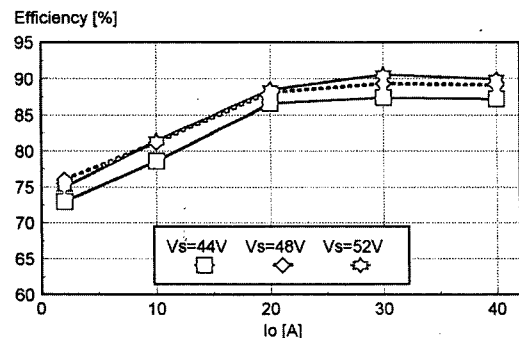

Fig. 14. Efficiency of an interleaved active clamp ZVS forward converter as function of source voltage and load

Fig. 13 shows the measured key waveforms for the different source voltages at full load condition. Fig. 14. shows the overall efficiency of the converter for the several loads

and several input voltages. It can be seen that the efficiency for the lowest input voltage (44V) is the lowest one along the load range because of much conduction losses. The maximum efficiency is 90.6% and it occurs when the input voltage is 52V and the output current is 30A. Losses distribution is shown in Fig. 15. It can be seen that losses in rectifiers is reduced and the switching and conduction losses in main switches are dominant of the overall losses. Other alternative which arises from Fig. 15, is that it could be possible to parallel one more MOSFET in every switch of the main switch. This way, the efficiency at full load could be higher, but the size and the switching losses would be higher.
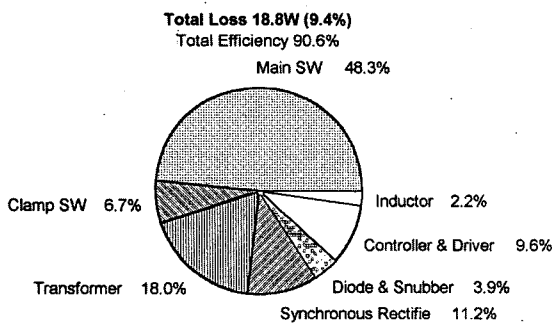

Fig. 15. Losses distribution in case of Vs=52V, Po=150W

VI. Conclusions

The design of a high efficiency power converter for a modular power processor in distributed power systems has been presented. An interleaved N-P MOSFETs coupled active clamp ZVS forward converter with MOSFET synchronous rectifiers is employed to achieve over 90% efficiency at nominal conditions. Power density is $40W/in^3$ ($2.44W/cm^3$) which is good for such a low output voltage in a converter with galvanic isolation. In order to optimize the efficiency and power density, high switching frequency and an interleaved N-P MOSFETs coupled active clamp ZVS forward converter with the MOSFET synchronous rectifiers are used. The N-P MOSFETs coupled active clamp method is employed to simplify the gate drive circuits and the magnetizing inductance of transformer is used to achieve the ZVS condition. The current mode controlled PWM chips are used with a constant switching frequency. It is expected that the design procedure of an interleaved N-P MOSFETs coupled active clamp ZVS forward converter with MOSFET synchronous rectifiers can be applied to other low-power DC/DC converter.

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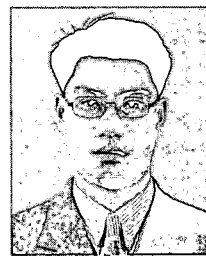
Gun-Woo Moon was born in Korea on October 3, 1966. He received B.S. degree from Han-Yang University, Seoul. Korea, in 1990, and M.S. and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology(KAIST), Taejeon, Korea in 1992 and 1996, respectively. Since 1996, he has been with Korea Electric Power Research Institute(KEPRI), where he is a senior researcher on FACTS devices. His research interests are include modeling, design and control of PWM converters, soft-switching power converters, resonant inverters, distributed power system, power factor correction converters, electric drive system, and static condenser and dynamic voltage regulator for Flexible AC Transmission System(FACTS). Dr. Moon is a member of KIEE and IEEE.