Improving Performance and Routability Estimation in Deep-submicron Placement

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Abstract

Placement of multiple dies on an MCM or high-performance VLSI substrate is a non-trivial task in which multiple criteria need to be considered simultaneously to obtain a true multi-objective optimization. Unfortunately, the exact physical attributes of a design are not known in the placement step until the entire design process is carried out. When the performance issues are considered, crosstalk noise constraints in the form of net separation and via constraint become important. In this paper, for better performance and wirability estimation during placement for MCMs, several performance constraints are taken into account simultaneously. A graph-based wirability estimation along with the Genetic placement optimization technique is proposed to minimize crosstalk, crossings, wirelength and the number of layers. Our work is significant since it is the first attempt at bringing the crosstalk and other performance issues into the placement domain.

I. Introduction

Rapid growth of multimedia and communication systems demands the use of both analog/digital mixed signal ICs and deep sub-micron (below 0.6 μm) CMOS technologies. The higher density and improved electrical performance of MCM technology is needed in these systems. In a typical ceramic multichip module, all the chips are bonded to the top layer (chip layer) of a multilayer substrate. Below the chip layer, there is a stack of wiring layers in which all the chip-to-chip nets must be interconnected and connections to module I/O pins (located on the bottom layer) must be established. The first step of the physical design process is *chip placement.* Over the years, a wide variety of placement algorithms have been developed. For an comprehensive overview of placement and routing algorithms, see [13]. In the mixed analog-digital layout design and deep sub-micron CMOS technologies, automated synthesis of interconnections during the early placement stage of the design cycle is emerging as a most promising approach. Current placement level design models do not capture important physical design effects such as crosstalk, power, and timing, simultaneously, which is the first order of factors in chip performance. Crosstalk noise should be considered because crosstalk between long wires increases delay (because of larger effective line capacitance) and also degrades signal integrity and causes logic faults. Crosstalk contributes as much as 50-75% to interconnection delay [1] as the width of the wire and the space between wires is reduced. In MCMs (resp. deep-submicron layouts), some of the netlengths for connection between bare dies (or modules) can be so long that they have a resistance which is comparable to the resistance of the driver. Performance-driven placement is very important since the interconnect delays form a major part of the system cycle time. A resistance-driven placement algorithm has been proposed in [16]. However when the more performance issues are considered, e.g., in deep-submicron technologies, additional constraints in the form of net separation and via constraint become important. This is because the fabrication of densely routed designs may result in low fabrication yield or a excessive crosstalk design. Excessive local congestion gives rise to future routing difficulty and also increases the potential crosstalk noise in high-speed signal lines. Futhermore, it increases power dissipation due to coupling capacitance. Crosstalk is minimized by ensuring that wires carrying high activity signals are placed sufficiently far from the other wires. Moreover, for high-performance MCM routing, intersections of wires cause the use of more vias which, in turn, require more routing resources (because of the large via pitch), low manufacturing yield, and cause noise problems (because of the mismatched characteristic impedance between wires and vias) [18]. The problem of crosstalk is addressed

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typically after the placement step. The next step in physical design is to assign every global route in the layout environment to a plane pair, called *layer assignment*, so that the capacity constraints are satisfied on all plane pairs, and the number of plane pairs is minimized. A layer assignment algorithm to reduce crosstalk presented in [3,4] maximizes the layer separation between interfering nets, so as to reduce both intralayer and interlayer crosstalk. There are several works related to crosstalk-minimum routings [5,6,11,19]. The main goal of the MCM router developed in [6] is to route all the nets with a minimum number of layers and reduce the crosstalk by separating high frequency wires with a bound over the number of vias used in routing. The placement model targets MCMs, but can also be applied to module placement in a chip layout. A given input is a set of rectangular chips of the same size with pins fixed within each block and a specification of n nets, including timing constraints on nets. Each output solution specifies an absolute position of each chip. The problem is stated as follows:
Given a set of chips C and a set of chip sites S, find a mapping Φ: C $\rightarrow$ S, so as to minimize the crosstalk, crossings and total wirelength needed for routing and to ensure routability of the design in a minimum number of routing layers. Early estimation of wirability during placement is important, but net topology is difficult to estimate at the placement stage. One way to get over the problem is to consider placement and layer assignment simultaneously. However, the high problem complexity may not lead to an effective solution. Motivated by the facts, to take the several performance constraints into account simultaneously, the problem is formulated as a graph-based optimization problem. There is no known reports on crosstalk minimization simultaneously during placement for high performance circuits. Thus, our work is significant and innovative since it is the first attempt at bringing the crosstalk and crossing minimization problem into the placement domain. In Section 2, we formulate the problem. In Section 3, a new heuristic to find a global routing estimation using one-bend routes is presented. An efficient solution to the problem using a Genetic algorithm is then proposed in Section 4. Experimental results and conclusion are presented in Sections 5 and 6, respectively.

II. Problem Formulation: the New Estimation

Conventionally, a cost metric based on wirelength plus congestion increases the wirability. However, in our formulation, we do not consider the congestion measure, explicitly. We observed by experiments that congestion minimization is done automatically while we perform crosstalk and crossing minimization simultaneously, because it distributes wires evenly over the MCM substrate. Note that minimizing the number of crossings reduces the wirelength, whereas minimizing the crosstalk does not always do so. Next, we introduce a new interference measure based on crosstalk and crossings.

1. Net Topology and Graph Generation

Multi-terminal nets have many possible routing topologies such as daisy chain, Steiner tree, star and A-tree [2,21]. However, it is impractical to consider all configurations of a large fan-out net because the number of net topologies as a function of the number of a large fan-out receivers increases rapidly. In [12], Raghavan, Cohoon, and Sahni demonstrated a polynomial time solution $O(n^2)$ time for a one-layer routing problem called *single bend wirability problem*, for two-terminal nets, which is the problem of determining whether there exists a planar routing with at most one bend per net. The problem can be reduced to the 2-satisfiability problem. However, allowing multiple terminals renders the single bend wirability problem NP-complete [22]. The formulation cannot be directly applied to solve our problem that considers multiple constraints on wires. The bounding box measure (of wiring interference) for placement without taking net topologies into account completely is not sufficien t.[1] Thus, we consider, for two-terminal net i, two possible one-bend global routes, denoted i_{τ_1} and i_{τ_2}. It is desirable that the multi-terminal nets are routed within the smallest bounding box enclosing the terminals belonging to the nets, and
with their favorite topologies as mentioned previously. For example, one restricts one to a specific routing pattern for a multi-terminal net with a mincost Steiner tree[2] having minimum wirelength, minimum bends, and minimum stubs. A stub or branch in a tree introduces extra delay and/or ringing in the received signal waveform [15]. Evidently, the topology estimate from a placement in this way is poorer than the estimate from global routing, but it is necessary compromise for a strong coupling between the placement and global routing. Based on these facts, given a placement, we create an interference graph $G = (V, E)$ (refer to Figure 2), where $|V| = 2n$ and $|E| \leq 2n(n-1)$ (in case of two terminal nets), to formulate the interference relation between n nets. In G, there are n nets of two types i_{τ_1} and i_{τ_2}, thus $|V| = 2n$. Edges are formed by connecting every node i_{τ_1} to $2(n-1)$ other nodes except for i_{τ_2}. Each node in V represents a net

1) For example, a simple measure which satisfies this property adds an edge between two vertices iff the bounding boxes of corresponding nets intersect. If the bounding boxes of two nets intersect in a highly congested region, the routability is more severely affected than if they intersect in a region with very few nets.

2) For nets with large terminals, a mincost Steiner heuristic is used

and a weight on an edge in E represents a net-pair crosstalk and crossings measured as below. If there is no crosstalk effect between two nets, then there is no corresponding edge in the graph G, thus $|E|$ can be less than or equal to $2n(n-1)$. In general, a graph $G(V,E)$ is a comparability graph if it satisfies the transitive orientation property, i.e., if it has an orientation such that in the resulting directed graph $G(V,F)$, $(v_i,v_j)\in F$ *AND* $(v_j,v_k)\in F \rightarrow (v_i,v_k)\in F$ [9]. Note that the interference graph G is a comparability graph because it satisfies the transitive orientation property by directing edges from left to right as shown in Figure 2.

2. Crosstalk Measure

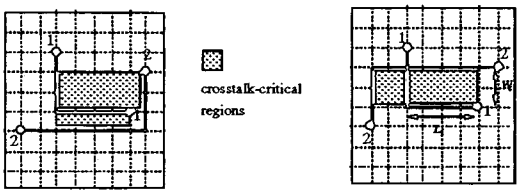

Fig. 1. Crosstalk and Crossing. Minimizing crosstalk may introduce more crossings.

A popular approach used in the past to model the dependency of performance functions on parasitics is net classification. Nets are classified according to the type of signal they carry(stable, large swing, sensitive to noise, etc.). A bus of several sensitive nets running parallel to each other with correlated signals might inject considerable noise into a single net. The *crosstalk-critical region* is defined as a region enclosed by two wire segments of net i and net j so that their coupling distance $d(i,j)$ is less than or equal to a small constant. The value depends on device technology. For example, using AC device technology on an MCM-L layer, δ = 1cm [4]. The shaded regions in Figure 1 corresponds to the set of crosstalk-critical regions induced by the given global routes of the two nets. The crosstalk between two nets i_{τ_p} and j_{τ_q}, denoted as $\mu(i_{\tau_p}, j_{\tau_q})$, is estimated as proportional to the maximum length for which two nets run in parallel and is inversely proportional to the minimum separation between the parallel wires:

$$\mu(i(\tau_p), j(\tau_q)) = \sum_{k\in K(i(\tau_p), j(\tau_q))} (\ell_k / d_k)$$

where $K(i(\tau_p), j(\tau_q))$ is the set of crosstalk-critical regions between two nets i with topology τ_p and j with topology τ_q. An interference graph is established for net-pairwise crosstalk value being an edge-weight of the graph in $O(n^2)$ time. Then, noise tolerance T_i for net i with topology τ with respect to the crosstalk measure μ is approximated as $T_{i(\tau)} = M_{i(\tau)} - \sum_{\forall j} \mu(i(\tau), j)$, where $M_{i(\tau)}$ is the maximum allowable coupled noise for net i with topology τ and j is the crosstalk-critically adjacent net with respect to net i.

We aim to identify the placement which either maximizes the sum of noise tolerance or maximizes the minimum noise tolerance for all nets. Thus, our goal is to remove all noise tolerance violations.

3. Crossing Measure

To minimize the number of signal line crossings and to minimize both congestion and wirelength, we also incorporate the wire crossings into our cost function. Especially for analog nets, crossings are one of the dominant crosstalk noises. The crossing effects of net-pair $\chi(i(\tau_p), j(\tau_q))$ can be computed by the number of intersection points between the net i with its topology τ_p and the other net j with its topology τ_q.

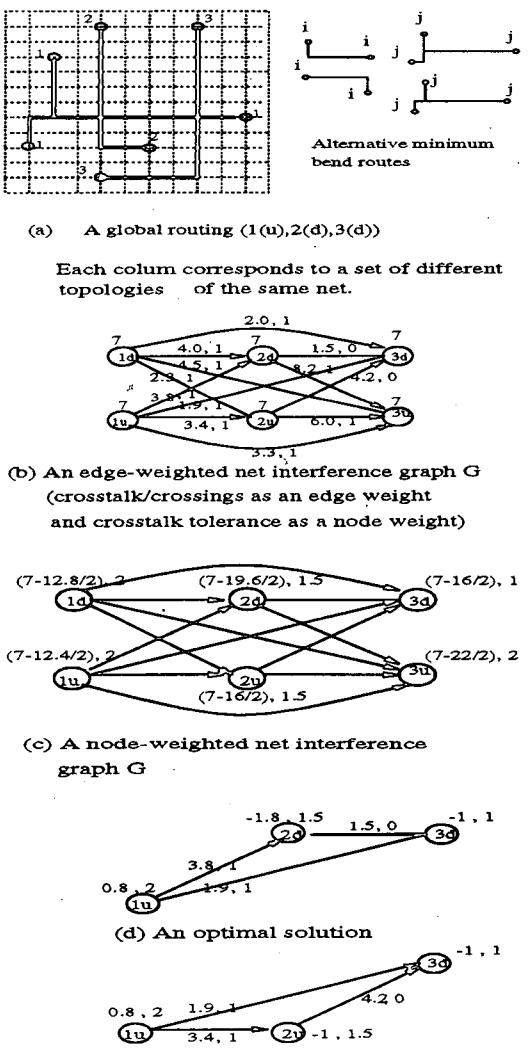

Fig. 2. Graph Formulation

4. Timing Constraints

We need to consider net topologies and size that cause delays larger than the performance requirements or longer than the maximum allowable driver-to-receiver path length. A method of generating bounds on both net length and width of lossy transmission line interconnects to satisfy timing and overshoot constraints of the MCM and PCB designs is described in [8]. Then, timing tolerance $S_{i(\tau)}$ for net i with topology τ with respect to the maximum driver-to-receiver path length $L_{i(\tau)}$ is approximated as $S_{i(\tau)} = M_{i(\tau)} - L_{i(\tau)}$, where $M_{i(\tau)}$ is the maximum allowable driver-to-receiver path length for net i with topology τ and $L_{i(\tau)}$ is the maximum driver-to-receiver path length of net i with topology τ.

5. Object (Fitness) Function

The first approach to our placement algorithm is to find a placement ϕ in Φ (a set of placements) with its global routing ω among a set of global routing solutions $\Omega(\phi)$ that finds

$$\min_{\forall \phi \in \Phi} f(\phi)$$

where the objective function $f(\phi)$ is

$$\min_{\forall \omega \in \Omega(\phi)} \{ \alpha \cdot norm(\max_{i(\tau) \in N} - T_{i(\tau)}) + \beta \cdot norm(\sum_{(i(\tau_p), j(\tau_q)) \in E} \chi(i(\tau_p), j(\tau_q))) \}$$

Here, the user-defined parameters α and β reflect the relative importance of minimizing the crosstalk and crossing, respectively, and *norm()* is a function to normalize the values of crosstalk and crossings. We are to find a Pareto point set by determining for appropriate weights for α and β to meet the various design constraints. The Pareto point set corresponds to an optimum solution to a placement problem minimizing either the number of layers, or the total wirelength, or crosstalk, by varying α and β.

III. Finding A Min-Bend Global Routing with Less Crosstalk and Crossings

We first select a placement ϕ which minimizes the wirelength, satisfying the given timing constraints. Given the initial placement, crosstalk and crossings are the next objectives to be minimized.

The problem of identifying the global routing which minimizes the total crosstalk noise and the number of crossings can be formulated as finding a minimum-edge weighted clique K_n of size n in G. Note that in G the maximum mode clique is of size n. In general graphs, both the maximum node-and edge-weighted k-clique problem is NP-complete, but when restricted to a comparability graph, the exact algorithm on a node-weighted maximum clique problem can be implemented to run in linear time in the size of the graph [9]. However, the exact polynomial-time algorithm on finding a minimum edge-weighted k-clique problem is not known even in comparability graphs. In general, given a complete undirected graph G(V,E) with edge weights $w(i,j)$, and an integer k, the minimum edge-weighted k-clique problem finds a minimum edge-weight clique with k nodes. The problem can be formulated as the following 0-1 integer programming problem which can be solved by any ILP package.

$$\min [\sum_i x_i + \sum_{(i,j) \in E} w(i,j) y(i,j)]$$

$$s.t.$$

$$x_i \in 0,1, y(i,j) \in 0,1$$

$$\sum_{i \in V} x_i = k$$

$$y(i,j) - x_i \le 0, y(i,j) - x_j \le 0, \forall (i,j) \in E$$

$$x_i + x_j - y(i,j) \le 1, \forall (i,j) \in E$$

We conjecture that the problem can be shown as NP-complete. Evidently, ILP is not our choice for fast wirability estimation even though it can be used for global routing. Our experimental results on some heuristics to solve the problem showed that the edge-weighted formulation does not work well in practice due to high complexity of finding a minimum-edge weighted clique. Motivated by the fact, for fast and reasonable estimation, we transform the problem into a version of finding minimum node-weighted clique of a comparability graph G.

Each node $i(\tau)$ is assigned by their corresponding average noise tolerance

$$T_{i(\tau)} = M_{i(\tau)} - \sum_{\forall j} \frac{\mu(i(\tau), j(\tau_q))}{|Q|},$$

where |Q| is the number of different topologies for net j. Refer to Figure 2. The crossing measure on node i can be similarly computed. The problem can be solved optimally in linear time by modifying the dynamic programming of [9] which is a non-trivial linear time algorithm to compute a maximum weighted clique. The difference is that we compute a maximum weighted clique with node size n instead of finding a maximum weighted clique with unlimited node size.

ALGORITHM: MINWEIGHT-CLIQUE

Instance: a comparability graph $G = (V, F)$ with a transitive orientation of E, and with a weight $w(v)$ to each node v.

Question: Find a Minimum Node-Weighted Clique K_n for which the sum of the weights of its vertices is largest possible.

(1) for all v in V do

(2) $w(v) = -1 \times w(v)$

(3) if v is unexplored then
(4) EXPLORE(v);
(5) end for all;
(6) select $y \in V$ *such that* $W(y) = \max W(v) | v \in V$;
(7) $K_n \leftarrow y$;
(8) $y \leftarrow POINTER(y)$;
(9) while $y \notin \Lambda$ do
(10) $K_n \leftarrow K_n \cup y$; $y \leftarrow POINTER(y)$;
(11) return K_n
END Procedure

Procedure EXPLORE(v)
(1) if $Adj(v) = \emptyset$ then
(2) $W(v) = w(v)$; $POINTER(v) \leftarrow \Lambda$; return;
(3) for all $x \in Adj(v)$ do
(4) if x is unexplored then
(5) EXPLORE(x);
(6) end for all;
(7) select $y \in Adj(v)$ *such that* $W(y) = \max W(x) | x \in Adj(v)$;
(8) $W(v) \leftarrow w(v) + W(y)$;
(9) $POINTER(v) \leftarrow y$;
(10) return;
END Procedure

Let source nodes to be the nodes that has no incident directed edge entering the nodes. Let sink nodes to be the nodes that has no incident directed edge escaping the nodes. Thus, if the interference graph consists of two terminal nets only, then the number of source nodes and sink nodes are equal to 2, respectively.

Lemma
After performing step **(5)** of ALGORITHM: MINWEIGHT-CLIQUE, at step **(6)**, y corresponds to one of source nodes in G.

proof> Steps 1~6 in Procedure EXPLORE identifies one of sink nodes. To each vertex v we associate its cumulative weight $W(v)$ after step **(5)**of Procedure EXPLORE. Thus, we preceed from sink nodes toward source nodes at step **(6)** of Procedure EXPLORE. Therefore, at step **(6)** of ALGORITHM: MINWEIGHT-CLIQUE, the node with a minimum accumulated weight coincides with one of source nodes in G.

Theorem
Algorithm MINWEIGHT computes minimum node-weighted clique K_n of a comparability graph G. Furthermore, the time complexity is linear in the size of the graph, i.e., $O(e+n)$, where n is the number of nodes and e is the number of edges in G.
proof> Procedure EXPLORE is similar to the recursive depth-first search. To each vertex v we associate its cumulative weight $W(v)$, which equals the weight of the least-weighted path
from v to some sink. A pointer is assigned to v designating its successor on that least-weighted path. Lines 7-10 calculate K_n once the cumulative weights are assigned.

IV. Placement with Genetic Algorithm

Over the years, a wide variety of placement algorithms have been developed. Sharookar and Mazumder [17] have provided a survey of various placement techniques. For solving simultaneous multi-objective optimization problems, iterative probabilistic search optimization algorithms like the simulated annealing [14] or genetic algorithms are used and the process is iterated until some stopping criteria is satisfied. There have been presented several genetic placement algorithms [10,17,20]. The problem of crosstalk is typically addressed after the placement step. There is no know report on crossing and crosstalk minimization simultaneously during placement, thus our work is significant and innovative since it is the first attempt at bringing the crosstalk and crossings into the placement domain.

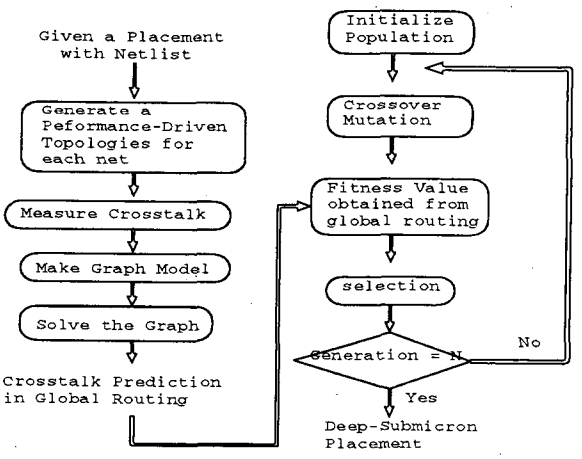

Fig. 3. (a)Crosstalk Estimation in Global Routing, (b) Placement based on Genetic Algorithm with the global routing prediction

The usual string representation in a genetic placement algorithm is as follows. The i-th element within a string corresponds to the placement of the i-th cell in row major among all possible placement locations in all the rows the MCM layout. Finding a appropriate set of parameters for GAs is crucial to its performance. A genetic algorithm is characterized by the number of offsprings to be generated ($0 < C < 1$) and the fraction of populations to be mutated

($0<M<1$). Optimal values for these parameters, C and M, are obtained automatically by running another meta-genetic algorithm for optimization of those parameters. Esbensen and Mazumder [7] have combined the genetic algorithm and simulated annealing algorithm to speed up the optimization search and obtain better placements compared to either algorithm alone. A typical genetic algorithm for placement would as follows;

Procedure GENETIC_PLACE()
initialize population;
for generation = 1 to 6
  crossover();
  mutation();
  for each population
    create $G(\phi)$ w.r.t the placement ϕ;
    estimation by running a minimum-crosstalk, crossing and minimum bend global router on $G(\phi)$ (as described in Section 3);
  end
  selection();
end
END Procedure

In summary, our approach is depicted in Figure 3.

V. Experimental Results

To evaluate the effectiveness of the algorithm, the placer was implemented in 'C', and was tested on MCC1, Ami49, and apte from MCNC benchmarks. Table 1 gives the description of the designs on which the placer was tested. All the experiments were tested using a SUN SPARCclassic. To see the impact of the crosstalk and crossings, we compared the proposed method with the placement of not considering crosstalk and crossovers, and with different values of α and β. We select a minimum one with respect to crosstalk among 9 different α's and β's. Figure 4 shows the result of using MCC1. After performing our placement algorithm, the wirability (i.e., the number of layers required), wirelength, and crosstalk were compared by running a crosstalk Driven MCM router [6]. As in Table {tab:1}, crosstalk is significantly reduced to 26% on the average. Furthermore, wirelength and the number of layers were decreased by 8.9% and 8.3% respectively on the average. For example, in the case of MCC1, the wirelength and crosstalk was improved by 14% and 17% respectively without increase in the number of layers. The execution time of running our algorithm took about 2 hours clock time (not CPU time) for MCC1, 30 minutes for Ami49 and 10 minutes for *apte*; the computing time was mainly due to wirability estimation step described in Section 3.

Table 1. Benchmarks

design	blocks	nets	I/O's
MCC1	9	799	765
Ami49	49	408	22
apte	9	97	73

Table 2. A comparison between placement without ours and with ours

	wirelength(10^5)			xtalk(10^4)			#. layers		
	w/o our alg.	w/ our alg.	% improve	w/o our alg.	w/ our alg.	% improve	w/o our alg.	w/ our alg.	% improve
MCC1	274	235	14	425	352	17	4	3	25
Ami49	40	37	7.4	48.8	33	32	5	5	0
apte	4.1	3.9	5.3	2.8	2	29.3	4	4	0
avg			8.9			26.1			8.33

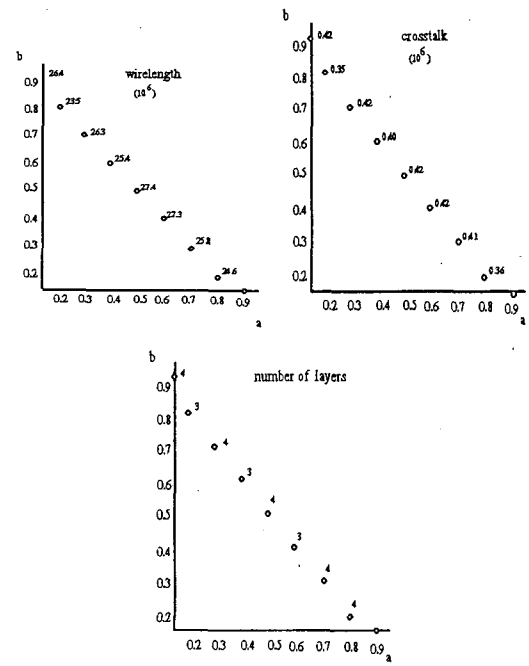

Fig. 4. Test results of MCC1 with varying α and β

Finally, we investigated the wirelength effect of minimizing crosstalk. Remind that crosstalk is proportional to the maximum length for which two nets run in parallel. Figure 5 represents the relationship between wirelength and crosstalk from Figure 4. It was interesting to observe that our placement algorithm automatically minimized the wirelength metric implicitly without including wirelength measure in our objective function. Thus, it can be a "universal" metric for optimizing deep-submicron physical designs.

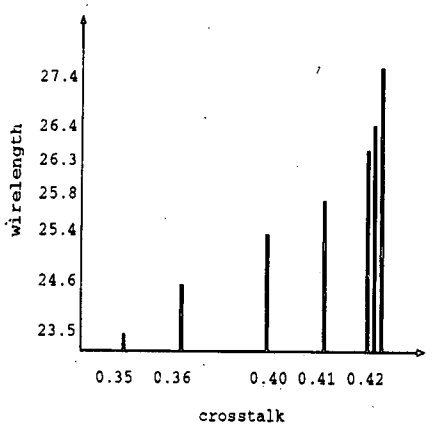

Fig. 5. Crosstalk vs. Wirelength

VI. Conclusion and Future Works

We have presented an effective crosstalk-minimum placement algorithm that considers minimum bend global routing simultaneously. A Genetic approach to solve the placement problem is presented. A novel graph formulation to find a minimum node-weighted *k*-clique on an comparability graph is presented for fast wirability and performance enhancement. Finding an optimal minimum edge-weighted *k*-clique problem in interval graphs is not known to be NP-complete, thus it is a open problem. Thus, one of future directions would be to develop a more efficient heuristic to find the near-optimal or optimal minimum edge-weighted k-clique in an interference graph.

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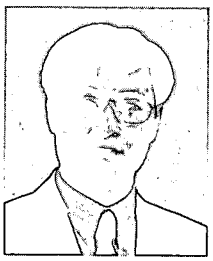

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