Dual-Gate Surface Channel 0.1 μm CMOSFETs

Hyouk Man Kwon, Yeong-Taek Lee, Jong Duk Lee, and Byung-Gook Park

Abstract

This paper describes the fabrication and characterization of dual-polysilicon gated surface channel 0.1μm CMOSFETs using BF_2 and arsenic as channel dopants. We have used an LDD structure and 40 Å gate oxide as an insulator. To suppress short channel effects down to 0.1μm channel length, shallow source/drain extensions implemented by low energy implantation and SSR(Super Steep Retrograde) channel structure were used. The threshold voltages of fabricated CMOSFETs are 0.6V. The maximum transconductance of nMOSFET is 315 μS/μm, and that of pMOSFET is 156 μS/μm. The drain saturation current of 418 μA/μm, 187 μA/μm are obtained. Subthreshold swing is 85mV/dec and 88mV/dec, respectively. DIBL(Drain Induced Barrier Lowering) is below 100mV. In the device with 2000Å thick gate polysilicon, depletion in polysilicon near the gate oxide results in an increase of equivalent gate oxide thickness and degradation of device characteristics. The gate delay time is measured to be 336psec at operation voltage of 2V.

I. Introduction

In CMOS technology, $POCl_3$ doped n^+ polysilicon has been used as a gate material for both nMOSFET and pMOSFET devices due to its simplicity in process. But in deep sub-micron regime, surface channel pMOSFETs with p^+ doped gate have advantages in terms of short channel effect and are preferable to buried channel pMOSFETs with n^+ gate[1].

In surface channel technology, both p^+ gate and n^+ gate must be integrated in the same wafer. But due to the difference of etch rate between n^+ polysilicon and p^+ polysilicon, the method of fabricating dual-polysilicon gate by doping the gate using source/drain implantation after patterning undoped polysilicon has been suggested[2]. This not only minimizes the number of photolithography steps but also avoids the problem of etch rate difference between n^+ and p^+ polysilicon.

However, there is considerable process optimization involved in an ion-implanted dual-gate technology. The thermal budget that can be tolerated in a deep sub-micron CMOS technology is limited by the necessity of having ultra-shallow source/drain junction. At the same time, it is necessary to degenerately dope the polysilicon gate up to the polysilicon/oxide interface in order to avoid problems with depletion effects in the gate. The depletion effect tends to increase the effective oxide thickness and thereby degrade the device characteristics[3,4,5].

This paper presents the fabrication of dual-gate surface channel 0.1μm CMOSFETs by doping gate after patterning, their DC and AC characteristics and device degradation due to gate depletion.

II. Fabrication

CMOSFETs with dual polysilicon gate (n^+ polysilicon for nMOSFETs and p^+ polysilicon for pMOSFETs) have been fabricated. Figure 1 shows the main process sequence. N-well was formed on the p-type substrate and n-well substrate concentration is 8×10^{16} cm^{-3}. Devices were isolated by the conventional LOCOS process. In order to control threshold voltage, BF_2 for nMOSFET and As for pMOSFET were implanted. Implantation energy and dose were split to investigate the device characteristics for various threshold voltages and channel profiles. Split conditions are shown in table 1. In order to suppress the bulk punch-through, $5 \times 10^{12}/cm^2$, 45keV boron was implanted in n-channel and $4 \times 10^{12}/cm^2$, 150keV As was implanted in p-channel. The gate oxide with thickness of 40 Å was grown by furnace at 800 ℃. The gate poly silicon was deposited with various thickness (1000 Å, 1500 Å and 2000 Å) to investigate the gate depletion as the variation of the gate polysilicon thickness. The gate pattern was defined by the direct e-beam lithography and RIE (reactive ion etching). Figure 2 shows a

Manuscript received October 29, 1997; accepted January 13, 1998.
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Table 1. Key process conditions

	nMOSFET	pMOSFET
substrate doping	B, 1×10^{15} cm^{-3}	As, 8×10^{16} cm^{-3}
V_{TH} control	BF_2, 1×10^{13}/cm^2, 90keV or BF_2, 1×10^{13}/cm^2, 70keV	As, 4×10^{12}/cm^2, 90keV or As, 1×10^{13}/cm^2, 120keV
Gate polysilicon thickness	1000 Å or 1500 Å or 2000 Å	
Punch-through stopper	B, 5×10^{12}/cm^2, 45keV	As, 4×10^{12}/cm^2, 150keV
Shallow source/drain	As, 5×10^{14}/cm^2, 10keV	BF_2, 5×10^{13}/cm^2, 10keV
Deep source/drain and gate doping	As, 5×10^{15}/cm^2, 35keV	BF_2, 3×10^{15}/cm^2, 10keV
Anealing	800 ℃ for 60 min. by furnace, and 1050 ℃ for 10sec by RTA	

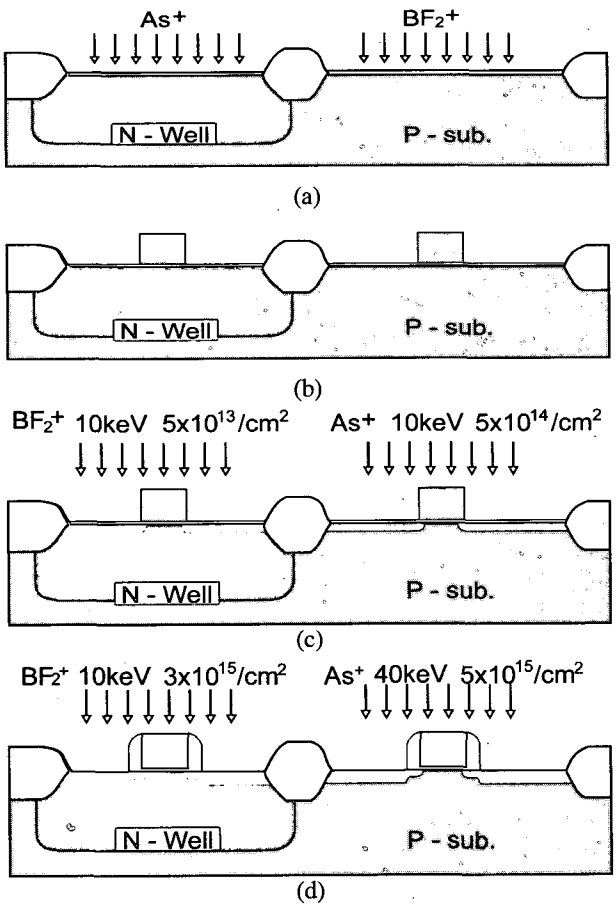


Fig. 1. The main process sequence. (a) n-well formation, active n-well, region, definition, implantation for the threshold voltage control, (b) gate oxidation and gate patterning (c) implantation for LDD, (d) sidewall formation and implantation for the deep S/D

SEM cross-section of a 0.19㎛ gate pattern after etching by RIE and deposition of TEOS with the thickness of 1000 Å. The shallow source/drain extensions were formed by low energy implantation with 5×10^{14}/cm^2, 10keV As for nMOSFETs and 5×10^{13}/cm^2, 10keV BF_2 for pMOSFETs. 1000 Å TEOS was deposited and etched by RIE for sidewall formation. Then, the deep source/drain doping and the gate polysilicon doping were performed simultaneously by implantation with 5×10^{15}/cm^2, 40keV As for nMOSFETs and 3×10^{15}/cm^2, 10keV BF_2 for pMOSFETs. Annealing was done at 800 ℃ for 60min by furnace, and 1050 ℃ for 10sec by RTA in nitrogen. Table 1 shows the key process conditions and the main split conditions.

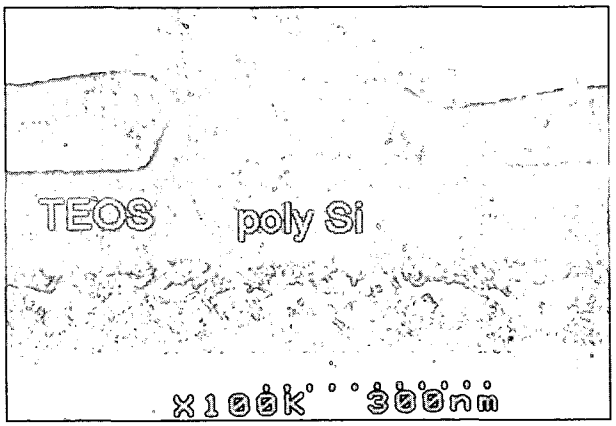
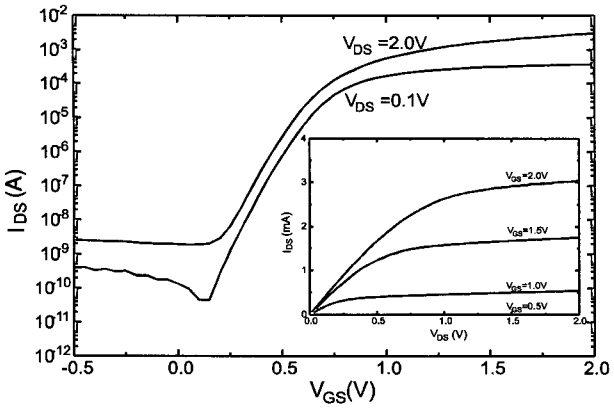


Fig. 2. SEM image showing the cross-section of etched polysilicon gate

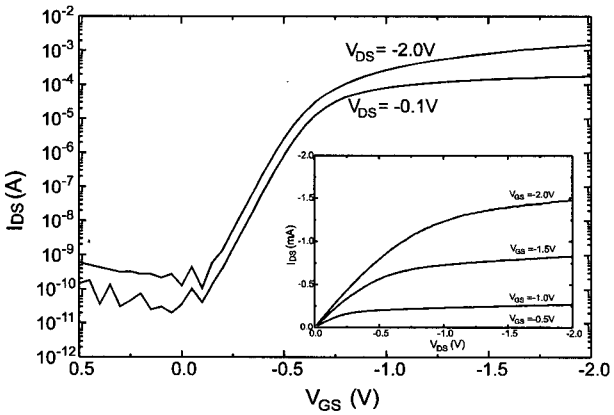
III. Device Characteristics

Figure 3 shows the I-V characteristics of the devices fabricated with the channel implantation condition of 1×10^{13}/cm^2, 90keV BF_2 for nMOSFET and 4×10^{12}/cm^2, 90keV As for pMOSFET. The patterned channel lengths were 0.19㎛ (Fig 2.) and the extracted effective channel lengths are 0.10 ㎛ for nMOSFET and 0.12㎛ for pMOSFET. The effective channel length was extracted by the variation of source/drain resistance at several substrate bias. Drain saturation current of 418㎂/㎛ and 187㎂/㎛ is obtained at $V_{GS}=V_{DS}=2V$. Maximum transconductances are 315 ㎲/㎛ for nMOSFETs and 156 ㎲/㎛ for pMOSFETs. Subthreshold swings are 85mV/dec for nMOSFETs and 88mV/dec for pMOSFETs, and no punchthrough is observed.

Figure 4 shows the threshold voltage roll-off characteristics as a function of the effective channel length. In the regime of 0.1㎛ channel length, the threshold voltage is 0.6V. Maximum threshold voltage shifts (ΔV_T) of nMOSFET and pMOSFET are 60mV and 30mV, respectively. For nMOSFETs, channel implantation condition of 90keV has better V_T roll-off characteristics and lower threshold voltage by 0.1~0.2V. For pMOSFETs, the two channel implantation conditions show very similar characteristics. This threshold voltage is high for 0.1㎛ CMOSFET characteristics and low power devices. This high threshold voltage is probably due to



(a)



(b)

Fig. 3. I-V characteristics (a) nMOSFET(Leff=0.10μm) (b) pMOSFET(Leff=0.12μm)

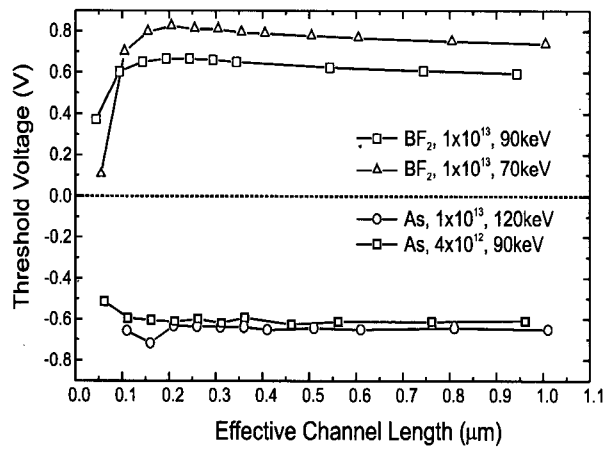
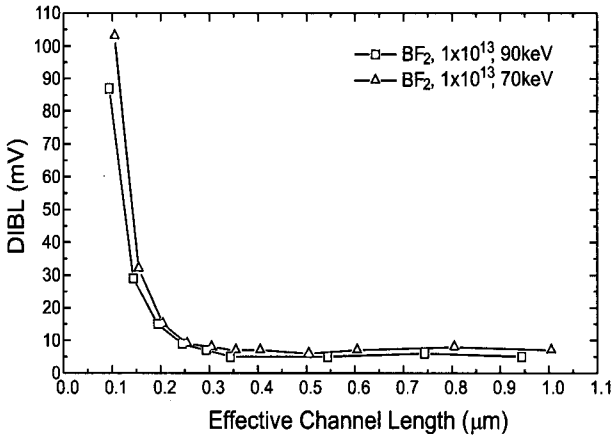
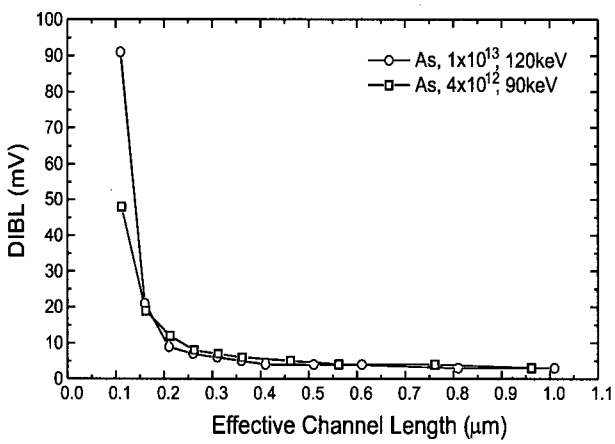


Fig. 4. Threshold voltage roll-off characteristics

high channel doping. The channel implantation dose(BF_2, $1\times 10^{13}/cm^2$) should be reduced by 20~40% in order to lower the threshold voltage to 0.3~0.4V for nMOSFETs. For pMOSFETs, high threshold voltage is due to high surface doping by less thermal budget in well drive-in process. Figure 5 shows that DIBL(Drain Induced Barrier Lowering) is less than 100mV, confirming that short channel effect is suppressed well in the regime of 0.1μm channel length.



(a)



(b)

Fig. 5. DIBL characteristics (a) nMOSFET (b) pMOSFET

Figure 6, 7, and 8 show the drain saturation current, maximum transconductance and subthreshold swing with the gate polysilicon thickness as a parameter. If polysilicon is not doped sufficiently due to low temperature annealing, the depletion effect tends to increase the effective oxide thickness and thereby degrade the device characteristics. Thus, the drain saturation current and the transconductance decrease, and the subthreshold swing increases. As the polysilicon thickness decreases, polysilicon grain size decreases. So dopants can not only reach the bottom of polysilicon, but also can easily diffuse into the polysilicon grain. These figures show that device characteristics are more degraded as the gate polysilicon thickness increases. The saturation current and the maximum transconductance decrease by 20~40%, and the subthreshold swing increases by 10%. Especially, the

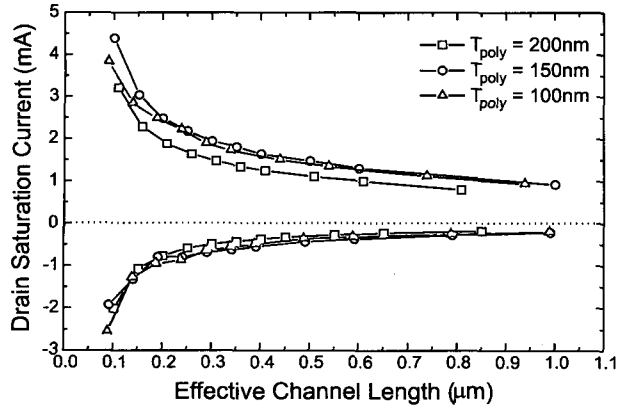
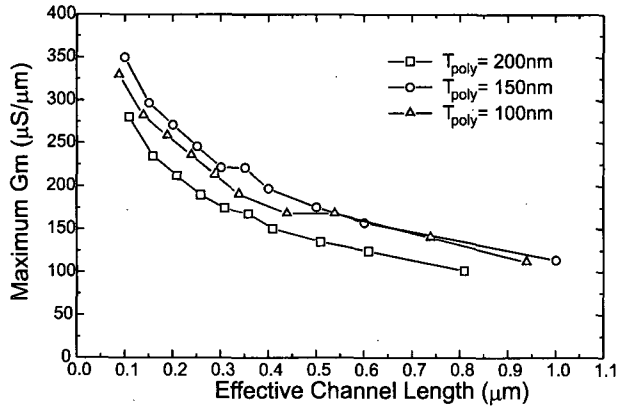
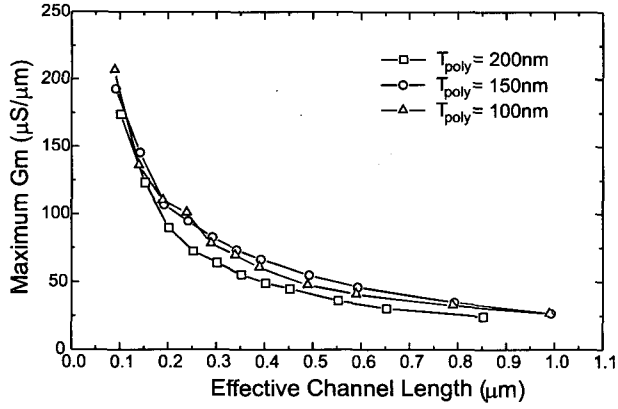


Fig. 6. Drain saturation current as the variation of gate polysilicon thickness.



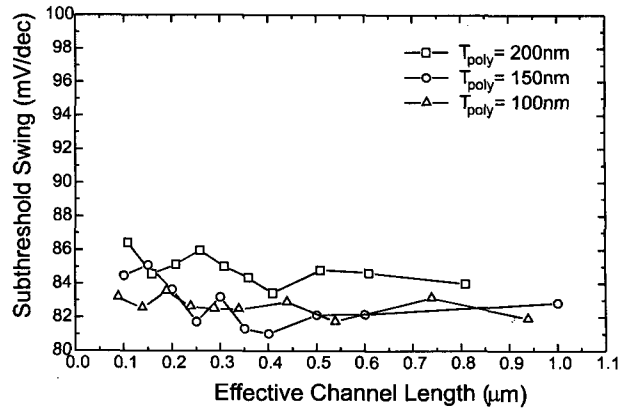
(a)



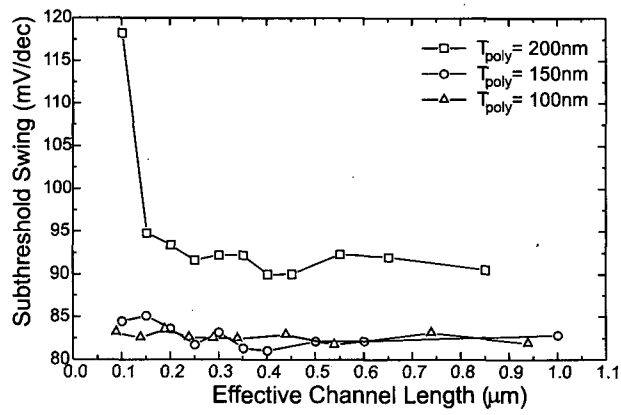
(b)

Fig. 7. Maximum transconductance as the variation of the gate polysilicon thickness (a) nMOSFET (b) pMOSFET.

characteristics of pMOSFETs are more degraded than those of nMOSFETs in terms of subthreshold swing. This seems to be due to low energy(10keV) source/drain implantation in order to get the ultra-shallow source/drain junction for



(a)



(b)

Fig. 8. Subthreshold swing as the variation of gate polysilicon thickness (a) nMOSFET (b) pMOSFET.

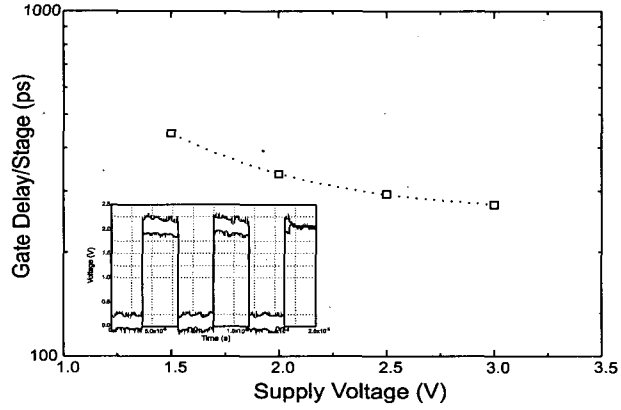


Fig. 9. Gate delay as a function of the supply voltage. The inset shows the ring oscillator waveform.

pMOSFETs.

Figure 9 shows the gate delay of CMOS inverters and the waveform of circuit. The circuit is composed of a 101-stage ring oscillator followed by a 7-stage frequency divider. The

gate delay is calculated to be 336psec at the operation voltage of 2V. The relatively large delay resulted mainly from large parasitics: (1) high resistance of S/D and gate due to the lack of silicide, and (2) large capacitance due to unscaled S/D area and relatively high channel doping. So silicide process is necessary to improve the AC characteristics, and channel doping should be lowered[6,7].

Ⅳ. Conclusion

We fabricated dual-poly gate surface channel 0.1㎛ CMOSFETs by doping the gate with source/drain ion implantation after gate patterning. The gate depletion effect on device characteristics was investigated for various thickness of the gate polysilicon. By performing the gate doping at the source/drain doping simultaneously, we could reduce the thermal budget for boron diffusion in p^+ gate polysilicon. As a result, the boron penetration from p^+ polysilicon into channel surface in pMOSFET could be suppressed effectively. However, the performance of CMOSFET with gate polysilicon thicker than 2000 Å was considerably degraded by the gate depletion problem. In order to avoid the gate depletion, the thickness of gate poly silicon should be reduced to less than 1500 Å. But, the AC performance of CMOSFET was degraded by the large resistance of gate polysilicon. To improve the AC characteristics, The gate resistance should be reduced, by incorporating the silicide process.

Acknowledgment

This research was supported by the Electronics and Telecommunication Research Institute(ETRI) under contract No. ISRC96-N-5512.

References

[1] Genda J. Hu and Richard H. Bruce, "Design Tradeoffs Between Surface and Buried-Channel FET's," IEEE Trans. Electron Dev., vol.32, no.3, pp.584-588, 1985.

[2] C.Y. Wong , J.Y.-C. Sun, Y. Taur, C.S. Oh, R. Angelucci, and B. Davari, "Doping of N+ and P+ Polysilicon in a Dual-gate CMOS Process," IEDM Tech. Dig., pp.238-241, 1988.

[3] S. Batra, K. Park, J. Lin, S. Yoganathan, J.C. Lee, S.K. Banerjee, S.W. Sun, and G. Lux, "Effect of Dopant Redestribution, Segregation, and Carrier Trapping in As-Implanted MOS Gates," IEEE Trans. Electron Devices, vol.37, no.11, pp.2322-2330, 1990.

[4] J.J. Sung and C.-Y. Lu, "A Comprehensive Study on p^+ Polysilicon-Gate MOSFET's Instability with Fluorine Incorporation," IEEE Trans. Electron Devices, vol.37, no.11, pp.2312-2321, 1990.

[5] L.K. Han, D. Wristers, J. Yan, M. Bhat, and D.L. Kwong, "Highly Suppressed Boron Penetration in NO-Nitrided SiO_2 for p^+-Polysilicon Gated MOS Device Applications," IEEE EDL-16, no.7, pp.319-321, 1995.

[6] Y.Taur, S.Wind, Y.J. Mii, Y. Lii, D.Moy, K.A. Jenkins, C.L. Chen, P.J. Coane, D. Klaus, J. Bucchignano, M. Rosenfield, M.G.R. Thomson, and M.Polcari, "High Performance 0.1㎛ CMOS Devices with 1.5V Power Supply," IEDM Tech. Dig., pp.127-130, 1993.

[7] Tetsuo Izawa, Koh Watanabe, and Seiichiro Kawamura, "21-ps 0.1㎛ CMOS Devices Operating at Room Temperature," IEEE EDL-14, no.11, pp.533-535, 1993.

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