A Study on Switching Shunt Regulator for Satellite Power System

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Abstract

The resistive shunting for the fine control of a Direct Energy Transfer(DET) systems is fully developed, but the non-resistive shunting using variable size solar array segments is in progress. This paper presents the spacecraft power control through switching of solar array segments, which uses a fully regulated DET power regulation. This method eliminates a dissipative element and removes the associated design limitations which arise from the dissipative elements for radiating cooling in deep space.

The switching shunt regulator comprises the switched Solar Array Shunt(SAS) modules that regulate the solar array power. These SAS modules connect/disconnect the solar array segments to/from the bus according to the loading in the main bus without significant variations in the dissipation level. In this paper, twelve segments are used in the shunting. In order to verify the basis of analysis, the computational result of an analytic loop gain is performed.

I. Introduction

The spacecraft power system is composed of solar panel, a solar array drive unit, a power control unit which includes solar array regulator and battery charger/discharger. The power control unit of a spacecraft must provide adequate power to each subsystem and payload during mission life, and it also needs high reliability and performance in space environment. The power control unit can be classified into Maximum Power Point Tracking(MPPT) system and Direct Energy Transfer(DET) system. The maximum power available from solar array is processed by peak power tracker and its output is used to charge batteries through the dc/dc converter, DET system, which is used in GEO satellites, is directly transferred to the load without any use of a series-connected regulator and it regulates the bus voltage by shorting out unnecessary sections of a solar array if excess power is available.

This paper presents the improvement of conventional Koreasat1 power system with partial shunt regulator which has switch heat problem during switching, and weight increase problem as power level goes up. Partial shunt regulator control method is to place a tap on the array string. On the other hand a non-dissipative switching shunt regulator regulates bus voltage through solar array sections switching on or off. Thus this control method maintains the bus voltage at a fixed level from a light to a full load. The non-dissipative switching shunt regulator can decrease switch heat problem because it regulates the bus voltage by shorting out unnecessary sections of the solar array when excess power is available. The advantage of this configuration is to eliminate any additional wiring on switches, which cause complexity to a existing design using a simple digital control[1-3].

In this paper, small-signal dynamics of the main bus of a spacecraft power system in various modes are analyzed. The bus impedance is fully analyzed, and the system loop gain and digital gain are discussed.

For the verification of analysis, dynamic characteristics of main bus are simulated using Pspice and Matlab software for each mode of the systems operation.

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II. Solar Array Regulator

1. Solar array regulator circuit

The non-dissipative switching shunt regulator regulates the bus voltage by shorting out the unnecessary sections of the solar array when excess power is available. Considering the solar array switching concept can be classified into four basic

configurations. In the four configurations, a series-switching parallel array and a shunt switching parallel array have been used as the prime candidates for controlling solar array because of a low stress on the solar array during shadowing, the lowest wiring complexity, and the simplest switch drive electronics[4].

In this paper, the shunt switching parallel array is selected as shown Fig.1. The configuration of solar array with non-dissipative shunt switch is connected parallel to the shunt switching parallel array. It can be designed in small size and built lightweight because of less heat problem than other configuration.

Each array section under sunlit and normal orientation behaves as a current source I_{SH} and is assigned to a shunt switch. The individual shunt switches are in turn determined by the corresponding output logic state of a microprocessor.

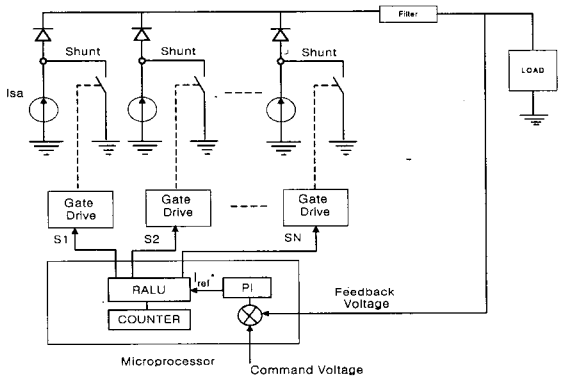


Fig. 1. Block diagram of non-dissipate shunt regulator.

2. Switching regulator control principle

The switch control technique of the solar array regulator with switching method can be implemented by several methods. In this paper, the proposed control principle is shown in Fig. 2.

The output bus regulation is achieved by sensing the bus voltage via an error amplifier. The regulator control circuit monitors the power bus voltage, V_{bus}, and compares it with the reference voltage, V_{ref}, to generate an error signal. When the error output exceeds the high reference voltage, V_H, then the on window enables the digital logic so that more bits in the register of microprocessor are in a state corresponding to switch-on state. On the contrary , if the error output drops below the low reference, the off logic turns off more bits. As a result, a section of the array is disconnected

Fig. 3 shows a crossing point between I-V characteristics for the output of the switching solar array segments and constant power load. The operating point is maintained on the constant current portion of the solar array characteristics, as illustrated in Fig. 3 by point A. This operating point is unstable due to the negative resistive characteristic of the load. To understand the dynamics of this system, we assume an initial operating point A. A slight deviation(move a point B) from this reference, e.g., an increase in voltage, results in decrease of the input current required by the load. When the load current decreases, the solar array regulator will be shunt array sections. If the load current exists between array sections, a switch in that point is controlled by Pulse Width Modulate(PWM) method as shown by Q3 in Fig. 2. In real operation, either a load decrease or source increase tends to increase the bus voltage. Under this condition, more shunts will be turned on to absorb the excessive source currents.

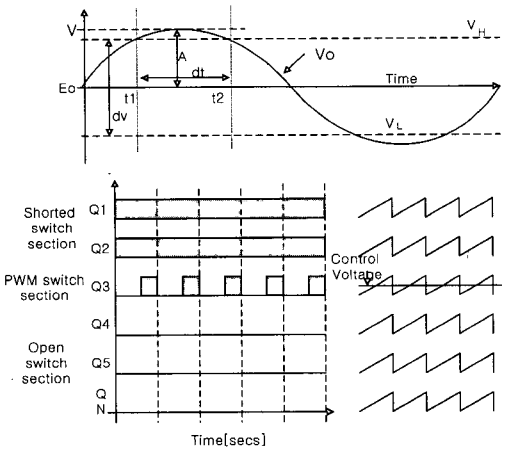


Fig. 2. Voltage detection definition of sequential shunt regulator.

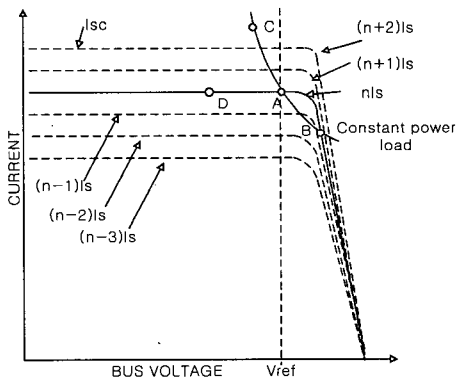


Fig. 3. Parallel switching solar array segments.

III. Bus impedance analysis

In shunt mode, system stability of the shunt regulator depends on the shape of the system loop gain. Control loop of the solar array shunt regulator is characterized by the input impedance of solar array, bus filter capacitor, load and control circuit of the solar array regulator. One solar array

section consists of a number of cells in series to get a string with the required voltage. Many of these strings are connected in parallel to get the total section current, I_p. Individual solar cell parameters are described in [5].

Fig. 4 shows the small-signal equivalent model for the system. The shunt regulator feedback controller gain is represented by the admittance Y. The equivalent solar array and bus capacitor output impedance, Z_{eq}, is the open loop bus impedance of the system without the regulator gain, Y. In general, the lumped parameters, C_{11} and R_s are small, and the bus open loop impedance Z_{eq} can be approximated by:

$$Z_{eq}=\frac{R_{11}(1+s/\omega_0)}{1+s\omega_1} \tag{1}$$

where, $\omega_0=\frac{1}{CR_C}$, $\omega_1=\frac{1}{CR_{11}}$

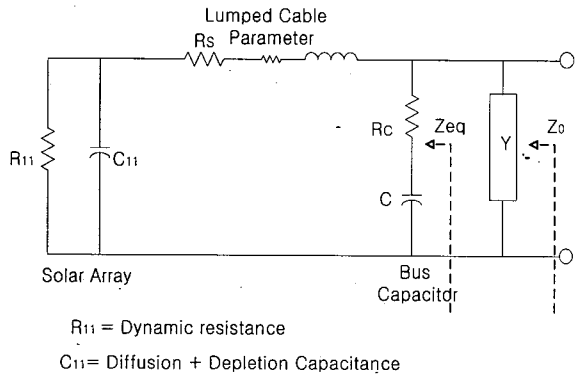


Fig. 4. Small-signal equivalent model.

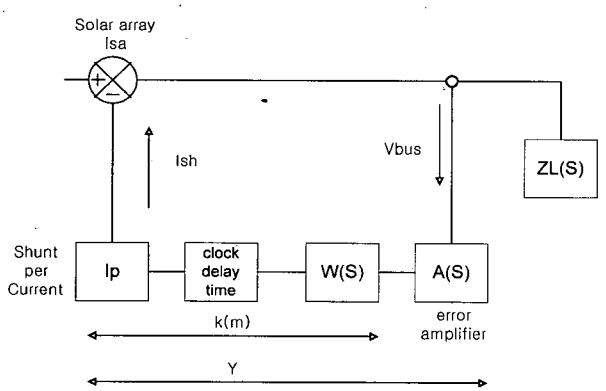


Fig. 5. Small-signal block diagram for solar array regulator.

As given by the computer simulated plots, using the actual circuit model, shown in Fig. 6, the low frequency value of Z_{eq} is $R_{11}+R_c \cong R_{11}$, the pole is at $\omega_p = 1/(CR_{11})$; and the zero is at $\omega_z = 1/(CR_c)$. The high frequency value is R_c which will be the peak value of the bus impedence if the loop gain T is properly a adjust.

1. Loop gain and stability analysis

The shunt regulator forms a simple feedback system, with the regulator gain Y as the system feedback gain

$$T=Y\cdot Z_{eq} \tag{2}$$

while the closed loop bus impedance is

$$Z_0=\frac{Z_{eq}}{1+T} \tag{3}$$

The shunt controller gain function in Fig. 5 is

$$Y=\frac{i_{sh}}{v_{bus}}=k_m\cdot A(s) \tag{4}$$

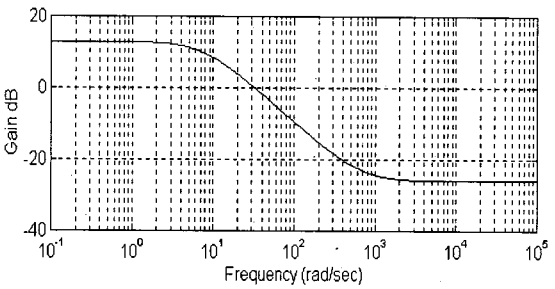


Fig. 6. Source impedance, Z_{eq}(0dB=1Ω) R_1=4.4, C=3000 μF, R_C=0.05, f_p =12Hz, f_z=1.1KHz.

Where i_{sh} is the small signal switched current, v_{bus} is the small signal bus voltage, A(s) represents the error amplifier gain, and k_m is the digital controller gain. Note that km including a digital gain function, the digital clock delay, and digital gain function, w(s) , can be obtained from Fig 2. The first-crossing time t_1 is obtained between the reference voltage and bus voltage.

$$t_1=1/\omega\cdot\sin^{-1}[\frac{V_h-E_0}{A}] \tag{5}$$

And the time interval dt is given by

$$dt=\frac{\pi}{\omega}-2\cdot t_1 \tag{6}$$

$$dt=\frac{\pi-2\cdot\sin^{-1}[\frac{V_h-E_0}{A}]}{\omega} \tag{7}$$

During this time interval, more shunts are actively turned on. In the above equation, E_0 is equal to $[(V_h-V_l)/2]$. Voltage-to-time duration conversion process is completed and yields a time-window function prescribed as

$$f(TW)=\frac{\pi\cdot 2\sin^{-1}[\frac{V_h-V_l}{2A}]}{\omega\cdot T_c} \tag{8}$$

The window function indicates that, for constant V_h, V_l, the window width explicitly depends on

$$f(TW)\geq 1,\qquad A\geq\frac{V_h-V_l}{2\cdot\cos[\omega\cdot\frac{T_c}{2}]} \tag{9}$$

the sinusoidal amplitude A. In other words, the gain function being sought for is

$$f(TW) = \frac{d}{dA} f(TW) \tag{10}$$

that is

$$\frac{d}{dA} f(TW) = \frac{2[V_h - V_l]}{A \cdot \omega \cdot T_c \cdot \sqrt{A^2 - (V_h - V_l)^2}} \tag{11}$$

By adopting the Laplace operator. And the digital gain function which includes the comparator, the digital logic can be rewritten as

$$W(S) = \frac{2[\frac{V_h - V_l}{A}]}{A \cdot T_c \cdot s \cdot \sqrt{1 - [\frac{V_h - V_l}{A}]^2}} \tag{12}$$

The digital gain is $k_m = W(s) \cdot e^{-s(T_c/2)} \cdot I_P$ which include each array module current, Ip, digital gain function, W(s), and digital clock delay time, $e^{-s(T_c/2)}$.
The error amplifier transfer function is as follows

$$A(s) = \frac{A_m}{1 + s/\omega_c} \tag{13}$$

where A_m is the dc gain of error amplifier. The overall loop gain, T, is given by

$$T = Z_{eq} \cdot k_m \cdot A(s) \tag{14}$$

$$T(s) = - Z_{eq} \cdot W(s) \cdot e^{-s(T_c/2)} \cdot I_P \cdot A(s) \tag{15}$$

2. Design example

The primary consideration in the loop gain design is that T must drop below unity at a designed frequency with a reasonable stability margin. At the same time T should be high at dc to provide good bus regulation. As shown in Fig 7, the loop gain must be made much larger than 1 in the region ω_0 to ω_c ,if possible.

The closed loop impedance, Z_0 is also shown in Fig 7.

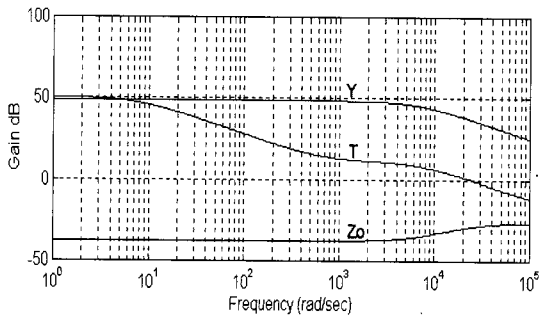


Fig. 7. Transadmittance of shunt, Loop gain and Bus impedance.

The numerical design data are provided as
- Bus voltage : 70V
- Bus voltage variation : 1V for 0 to 48A
- $\omega_c = \omega_0 = 1/CR_C$: 6666[rad/sec]
- ω_m = 25000[rad/sec]
- Y_m = 75 mho
- C = 3000 μF

The switching frequency choice is selected based upon many factors, such as required closed loop bandwidth, bus voltage ripple specification, and bus capacitor ESR at switching frequency. For a given system, the proportional controller bandwidth of 4kHz is chosen as the switching frequency. With a switching frequency of 20kHz, the loop gain crossover ω_m is chosen as one-fifth of the switching frequency, 25000[rad/sec], The controller bandwidth ω_c is chosen at 6666[rad/sec]. The DC value of controller gain will produce bus voltage error of 0.64V for 48A load current variation, which is within the specified 1V variation. This value of Y_m in this system is 75mho. Each array section gives 4A, and fine control of the current is obtained via PWM(Pulse Width Modulation) control in one section of the 12 array sections

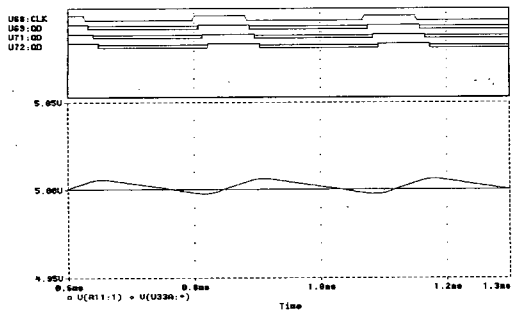
IV. Simulation and Discussion

The switch control principle of solar array regulator with switching technic can be handled by several methods. In this paper, two kinds of control methods are simulated. The first is decided output bit via shift register using the the bus voltage sensed. For the latter case, the switch is controlled by PWM method.

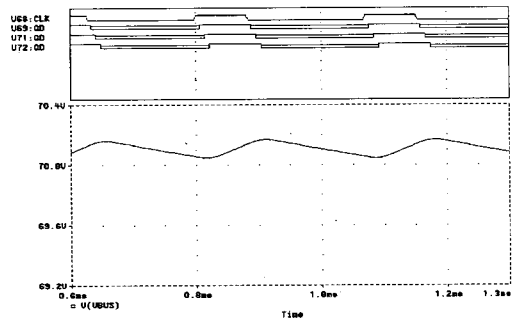
The waveform of digital output in Fig. 8 is obtained by sensing the bus voltage via error amplifier. This becomes the clock input(U68) of the counter, which is compare with counter pulse by the pulse of clock generator. The output pulse of the shift registers(U69, U71, U72) is shown shifting at the every edge of the clock pulse. The bus voltage which increases during the output of shift registers(U69;QD, U71;QD, U72;QD) is on because of the solar array segments, and switch drive circuits are connected in parallel. When the error output exceeds high reference voltage, V_H as shown in Fig. 8.b, the shift register is turned off. The maximum ripple voltage of this circuit is 0.15V , which is within the specified ripple voltage range.

In Fig. 9, the bus voltage is maintained at a fixed level via the control of switch circuit which is connected to solar array in parallel. Fig 9.b is shown for which the bus voltage is subject to varied ripple voltage from maximum $\pm$0.44V to $\pm$ 0.39V for 10A to 30A step variation.

Fig. 10 shows the bus voltage variation and total shunt

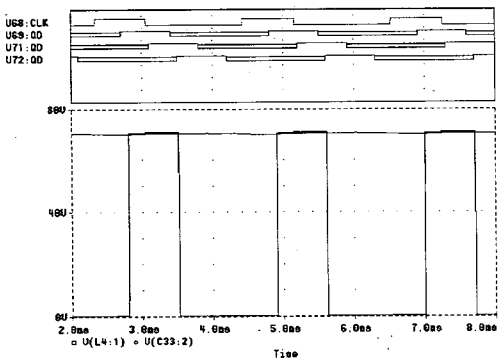


(a) Comparison waveform of error detector

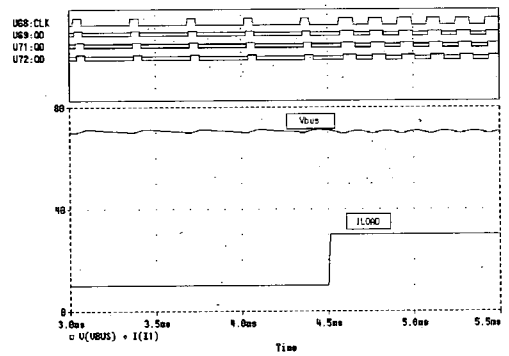


(b) Bus voltage variation for fixed load

Fig. 8. Error detect of shunt switch solar array.



(a) Operation waveform of Shunt switches



(b) Bus voltage variation for transient load

Fig. 9. Shunt switching simulation of solar array Vmax= 70.15V, Vmin=70.05V, C=3000uF.

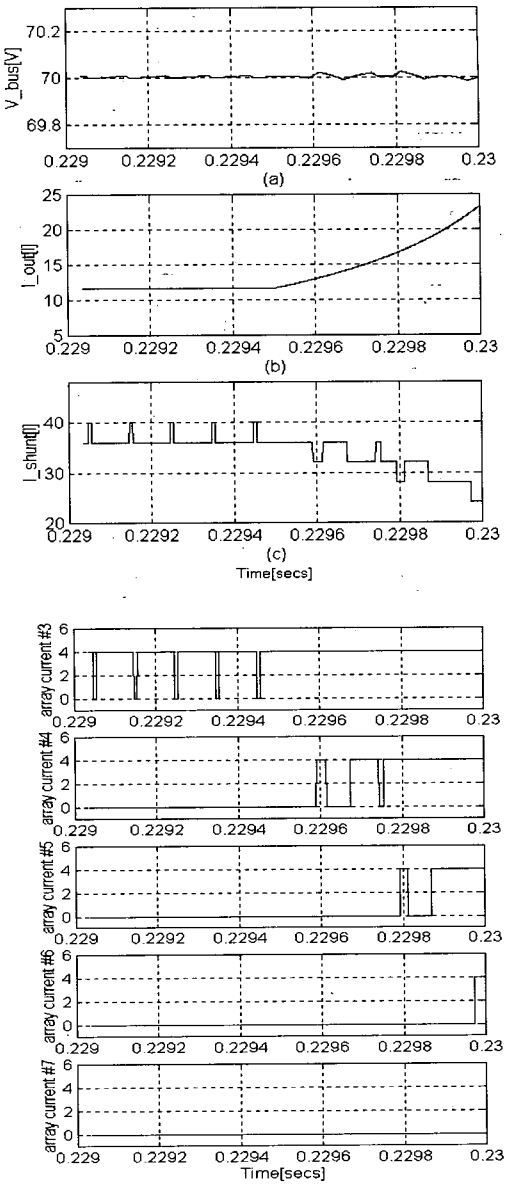


Fig. 10. Shunt switching simulation of solar array (for load variation).

current for load variation. The regulator is in PWM control in number #3, #4, #5, #6 of solar array. Bus voltage variation and total shunt current for fixed load are shown in Fig. 11, and the number #4 of solar array is in PWM control. From the above observation, it turns out at the the PWM control method can be, used to decrease, the heat problem of switch via switching control of solar array

V. Summary

This study presents improvement of solar array regulator

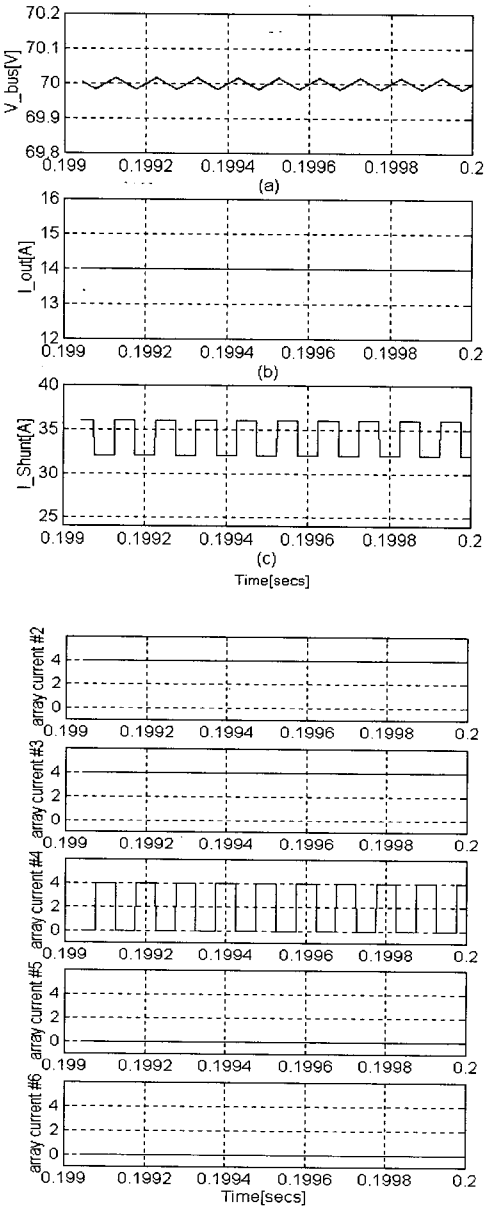


Fig. 11. Shunt switching simulation of solar array (for fixed load).

design using data of Koreasat 1,2. The proposed technique uses a new power control unit with digital control method. In order to overcome the disadvantage of the analog shunt switching method, digital control method with PWM control using microprocessor is tried in this study. In this paper, twelve segments are used in the shunting, and a solar array simulator is utilized as an alternative for the input power.

Small-signal dynamics of the main bus of the proposed spacecraft power system in various modes are also analyzed. The bus impedance is investigated in conjunction with the system loop gain and digital gain.

For the verification of analysis, the behavior of shunt switching regulator is simulated for each mode of the load variation.

References

[1] KENG, W.U., "Loop Gain of a Spacecraft Switched Shunt Power System", IEEE Transactions on Aerospace and Electronic Systems, Vol.30, No.4, 1994, pp.1049-1053.

[2] FLECK. G.W., "Solar Array Switching Unit Stability Analysis", Proceeding of the 19rd Intersociety Energy Conversion Engineering Conference, 1984, pp576-581

[3] Patil. A.R., and Cho B.H., "Design Consideration for a Solar Array Switching Unit", Proceeding of the 25rd Intersociety Energy Conversion Engineering Conference, 1990, pp.373-379.

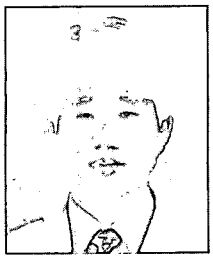
[4] Decker D.K., and Cassinelli. J., "High Power Solar Array Switching Regulation", Proceeding of the 16rd Intersociety Energy Conversion Engineering Conference, 1981, pp.224-231.

[5] Peck S.R., and Devaux R.N., STC/DBS Power Subsystem Control Loop Stability Analysis, Proceeding of the 19rd Intersociety Energy Conversion Engineering Conference, 1984, pp.636-647.

[6] ----------, The Design Center Application Notes Manual, MicroSim Corp.,1993.

[7] ----------, MATLAB Reference Guide, The Math Works Inc.,1993.

[8] Choi J.D., "Design Consideration of Spacecraft Switched Shunt Power System", KIEE Conference, 1996, pp.320-322.



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