Random Pattern Testability of AND/XOR Circuits

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Abstract

Often ESOP(Exclusive Sum of Products) expressions provide more compact representations of logic functions and implemented circuits are known to be highly testable. Motivated by the merits of using XOR(Exclusive-OR) gates in circuit design, ESOP(Exclusive Sum of Products) expressions are considered as the input to the logic synthesis for random pattern testability. The problem of interest in this paper is whether ESOP expressions provide better random testability than corresponding SOP expressions of the given function. Since XOR gates are used to collect product terms of ESOP expressions, fault propagation is not affected by any other product terms in the ESOP expression. Therefore the test set for a fault in ESOP expressions becomes larger than that of SOP expressions, thereby providing better random testability. Experimental results show that in many cases, ESOP expressions require much less random patterns compared to SOP expressions.

I. Introduction

BIST(Built-in self test) is one of the most frequently used DFT(Design for testability) techniques[1], in which parts of a circuit are used to test the circuit itself. Since generation of test patterns and analysis of test responses are necessary to test a circuit, implementing BIST inevitably requires extra hardware. To reduce the penalty of cost and performance caused by BIST, often LFSRs(linear feedback shift registers) are used as pseudo-random test pattern generators. However, to obtain enough fault coverage in a reasonable amount of test time, the circuit should be testable with random patterns.

To achieve this goal, there have been many approaches published which includes techniques of inserting tests so that the faults resistent to random patterns are easily detected[2]. The other methods eliminate random pattern resistent faults during transformations of two-level circuits into multi-level circuits [3, 4]. Also it has been demonstrated [5] that careful assignments of don't cares of functions can improve random pattern testability of the circuit.

In constructing random testable multi-level circuits, SOP (Sum of Products) expressions are used at the start of its logic synthesis procedure and testability preserving transformations are applied to get multi-level logic circuits[3, 4]. However, there have been many researches demonstrating the high testability of AND/XOR circuits. Several advantages of using XOR gates in designing testable circuits were shown in [6, 7, 8, 9]. Moreover, ESOP provides more compact representations than SOP expressions in many cases [10].

Motivated by the conciseness and high testability of AND/XOR circuits, in this paper, ESOP(Exclusive Sum of Products) expressions are considered as the input to the logic synthesis for random pattern testability. We focus on the problem of whether ESOP provides better random testability than SOP expressions. Consider a fault in gate inputs of AND/XOR circuits. Then the fault effect is propagated through a path that includes an XOR gate. The propagation of fault effects through XOR gates is not affected by other inputs to the XOR gate. Therefore generating test patterns in AND/XOR circuits is much easier than AND/OR circuits and the test sets become larger than those of AND/OR circuits. Since the test set of faults in AND/XOR circuits is larger than that of AND/OR circuits, obviously they provide higher random pattern testability.

Random pattern testability of a fault is decided by the detection probability of the fault which is defined as the number of test patterns that detect the fault divided by the total number of input patterns. In other words, if a fault has a larger test set, it has more probability of being detected by random patterns. Specially some faults with detection probability below some threshold are called r.p.r.(random pattern resistent) faults and a circuit is random testable if it has no r.p.r. faults [3].

Throughout this paper, AND/XOR circuits and AND/OR circuits represent two level gate networks which realize the

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given ESOP expressions and SOP expressions respectively and a *cube* refers to the product term realized by an AND gate of the two level circuit. Therefore a literal contained in a cube corresponds to gate input line of the AND gate. Test set for a fault stuck-at-α in line l is denoted by $T(l/\alpha)$. For a cube $C = \{l_1, l_2, ..., l_k\}$ and a literal $l \in C$, C/l denote $C - \{l\}$ and $C_{l=\beta}$ means C with l replaced by the constant β. The size of a cube represents the number of literals contained in it. Therefore small sized cubes actually contain more minterms than large sized cubes.

II. Test Generation of AND/XOR Circuits

The test set for a fault in input/output lines of an AND gate of the given AND/XOR circuits is determined only by the cube realized by the AND gate. Consider a stuck-at-α fault in line l which is an input to the AND gate realizing cube C_i where the ESOP of the given function F contains cubes $C_1, C_2, \cdots, C_n$. Then,

$$
\begin{aligned}
F(l=0) \oplus F(l=1) &= (C_1 \oplus C_2 \oplus \cdots \oplus C_{i,l=0} \oplus \cdots \oplus C_n) \\
&\quad \oplus (C_1 \oplus C_2 \oplus \cdots \oplus C_{i,l=1} \oplus \cdots \oplus C_n) \\
&= C_{i,l=0} \oplus C_{i,l=1} \\
&= C_i/l \qquad (1)
\end{aligned}
$$

$$
\begin{aligned}
T(l/\alpha) &= (l = \alpha') \cdot (F(l=0) \oplus F(l=1)) \\
&= (l = \alpha') \cdot C_i/l \qquad (2)
\end{aligned}
$$

Equation 1 is the condition for the fault propagation and equation 2 shows the test set obtained by combining logic equations corresponding to the fault excitation and the fault propagation. Since C_i/l denotes the cube obtained by eliminating literal $l \in C_i$, the number of tests in equation 2 is decided by the number of minterms contained in C_i, which is $2^{n-|C_i|}$ where n is the number of primary inputs. For example, if a cube $abc'd$ in the AND/XOR circuit contains a stuck-at-1 fault on input a, the test for the fault is $(a') \cdot (bc'd)$ by equation 2 which has one minterm if the function is composed of primary inputs a, b, c and d. Similarly, for a cube abc' with line a stuck-at-1, the test becomes $(a') \cdot (bc')$ by equation 2 which has two minterms $a'bc'd$ and $a'bc'd'$. Note that the test set is obtained independent of the other cubes in the circuits because the fault propagation is not affected by any other cubes of the ESOP except the one that corresponds to the faulty AND gate. This is due to the characteristic of the XOR gate collecting the cubes realized by AND gates. Obviously it provides a larger test set when the cubes are collected by an XOR gate compared to the case where the cubes are collected by an OR gate.

Example 1. *Consider two circuits given in Fig 1 which have same cubes or set of AND gates with same inputs. Figure 1(a) shows a circuit in which AND gate outputs are collected by an OR gate and in Figure 1(b), the same AND gate outputs are collected by an XOR gate. The lines in Figure 1(a) are denoted by* $l_1, l_2, \cdots, l_7$ *and*

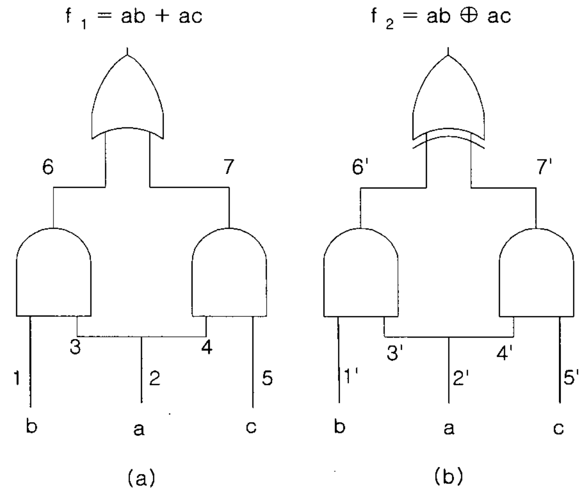

Fig. 1. Comparison of two circuits with same cubes collected (a) by an OR gate and (b) by an XOR gate

the lines in Figure 1(b) are denoted by $l_{1'}, l_{2'}, \cdots, l_{7'}$. *The test sets for faults occurring on gate input lines are as follows.*

$T(l_1/0) = abc' \rightarrow 1$ *minterm*
$T(l_{1'}/0) = ab \rightarrow 2$ *minterms*
$T(l_1/1) = ab'c' \rightarrow 1$ *minterm*
$T(l_{1'}/1) = ab' \rightarrow 2$ *minterms*

...

$T(l_7/0) = ab'c \rightarrow 1$ *minterm*
$T(l_{7'}/0) = ac \rightarrow 2$ *minterms*
$T(l_7/1) = (a' + c')(a' + b') = a' + b'c' \rightarrow 5$ *minterms*
$T(l_{7'}/1) = a' + c' \rightarrow 6$ *minterms*

Here, one can notice that with the same cubes the test sets for faults on gate input lines of AND/XOR circuit in Fig 1(a) are always larger than those for AND/OR circuits in Fig 1(b). In specific, consider a 0-stuck-at fault in line l_1 *and line* $l_{1'}$ *of Figure1.*

While the fault effect of the fault $l_{1'}/0$ *can be propagated to the primary output without considering the value of line* $l_{7'}$ *in Figure 1(b), the value of line* l_7 *in Figure 1(a) should be considered to propagate the fault effect of the fault* $l_1/0$ *to the primary output of Figure 1(a) as shown in the following equations.*

$T(l_1/0)$ = *(fault excitation)* $\cdot$ *(AND gate propagation)* $\cdot$ *(OR gate propagation)*

$$
\begin{aligned}
&= (l_1 = 1) \cdot (l_3 = 1) \cdot (l_7 = 0) \\
&= b \cdot a \cdot (ac)' \\
&= abc'
\end{aligned}
$$

$$
\begin{aligned}
T(l_1/0) &= (\text{fault excitation}) \cdot (\text{AND gate propagation}) \\
&= (l_{1'} = 1) \cdot (l_{3'} = 1) \\
&= b \cdot a \\
&= ab
\end{aligned}
$$

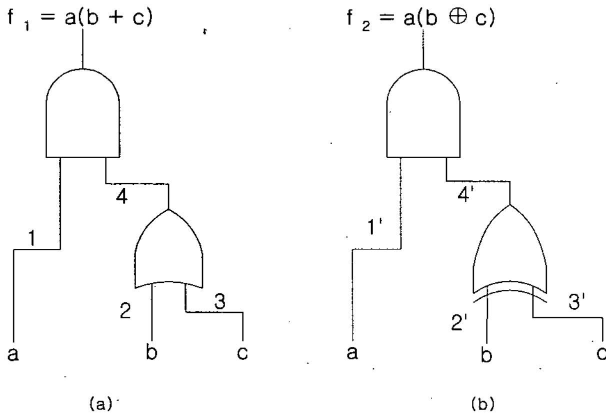

Fig. 2. Two circuits with same cubes after kernels are extracted using (a) an OR gate and (b) an XOR gate

Example 2 *Figure 2 shows circuits changed from those given in Figure 1 by kernel extraction. In this case, ESOP expressions provide larger test sets in most cases. However, there can be an opposite case as shown in the tests for faults in* l_1 *and* $l_{1'}$

$$
\begin{aligned}
T(l_2/0) &= abc' \rightarrow 1 \text{ minterm} \\
T(l_{2'}/0) &= ab \rightarrow 2 \text{ minterms} \\
T(l_2/1) &= ab'c' \rightarrow 1 \text{ minterm} \\
T(l_{2'}/1) &= ab' \rightarrow 2 \text{ minterms}
\end{aligned}
$$

$$
\begin{aligned}
T(l_1/0) &= a(b+c) \rightarrow 3 \text{ minterms} \\
T(l_{1'}/0) &= a(b \oplus c) \rightarrow 2 \text{ minterms}
\end{aligned}
$$

From the equation 1 and equation 2, the followings can be drawn.

Observation 1 *Comparing two circuits, AND/OR and AND/XOR, including same set of cubes, the test sets for faults in gate inputs of AND/XOR circuits are larger than those of AND/OR circuits.*

(Proof) The test of a fault is decided by combining conditions for the fault excitation and the fault propagation. The fault propagates through two gates, the faulty AND gate and the collecting OR(XOR) gate in AND/OR(AND/XOR) circuits. Propagating the fault effect through an XOR gate does not require the other inputs to have certain specific values. On the contrary, when the cubes are collected by an OR gate, the other inputs to the OR gate except the one on the propagation path should be 0 to propagate the fault effect. Obviously the condition of propagating the fault effect through the faulty AND gate is same for both cases and when the AND gate outputs are collected by an XOR gate, the condition for propagating XOR gate is not needed, resulting in a smaller test set. For the input lines of the OR(XOR) gate, the same argument applies.

Observation 2 *The test set size of a fault in AND/XOR circuits is decided by the size of the corresponding cube in its ESOP expression.*

(Proof) The test set size for a fault in a cube C_i *is* $2^{n-|C_i|}$ *by equation 2 where n is the number of primary inputs.*

From these observations, we can conclude that if a function is implemented by its ESOP expression with same sized cubes as its SOP expression, the random testability of the ESOP expression is better than that of the SOP expression, because the r.p.r. faults in two-level circuits are due to the large sized cubes(or equivalently cubes composed of smaller number of minterms) of its SOP or ESOP expressions. However, in some special cases, the opposite occurs.

Example 3 *Consider the circuit in Figure 3. The function f has the minimized ESOP expression with a cube which is larger than any cubes appeared in the SOP expression as shown below.*

$$
\begin{aligned}
f &= ab + cd \\
&= ab \oplus cd \oplus abcd
\end{aligned}
$$

In this case, obviously ESOP has r.p.r. faults and is hard to be tested by random patterns. However this case does not always happen in all Boolean functions. There can be numerous applications where the logic function does not fall into this category, which we can see from benchmark experiments.

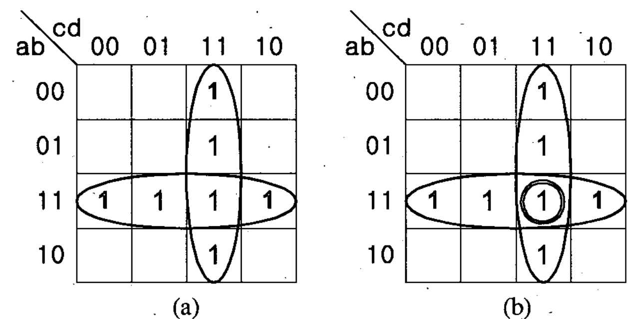

Fig. 3. The case where SOP(in (a)) provides better random testability than ESOP(in (b))

III. Effects of ESOP Representations on Random Testability

There exist many ESOP minimization tools developed and/or currently being developed[10, 11]. However, because

of much broader range of problem space, the results can have various forms. For example, minimized SOP forms contain only prime cubes on the ON-set of the function. In ESOP forms, the cubes need not to be on the ON-set of the function. The cubes of ESOP forms can be any cube in the Boolean space only if an ON-set minterm is covered by the cubes odd number of times and the OFF-set minterm is covered by the cubes even number of times.

Since random testability is affected by the cube size of the ESOP representation, we consider two typical minimization methods: one targeting product term count minimization and another which favors the solution without large sized cubes. The following examples show the differences of the two categories of ESOPs in their random testabilities.

Example 4 *Figure 4 shows an example which have two ESOP expressions with different sizes of the cubes. The given function f can be represented differently as follows.*

$$f = abc'd + ab'c'd \quad (3)$$
$$= abcd' \oplus ab'c'd \quad (4)$$
$$= acd' \oplus ab'c \oplus ab'd \quad (5)$$

One ESOP in 5 contains 3 cubes of size 3 and another in 4 has 2 cubes of size 4. Without computing exact probabilities, one can see that the latter is much harder to test with random patterns in the sense that the random pattern testability is decided by the existence of r.p.r. faults[3].

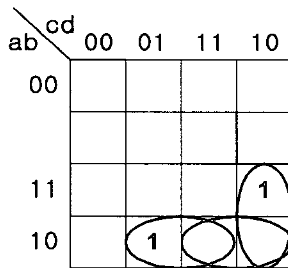

Fig. 4. ESOP with 3 cubes to cover a 2 minterm function.

Example 5 *Figure 5 shows another such example. Here, again, the ESOP with smaller sized cubes are better in random testability.*

$$f = [- - 1\ 0] \oplus [- 0 - 0] \oplus [- 0\ 0 -] \oplus [0 - - 0] \oplus [0\ 0 - -]$$
$$= [1\ 1 - 0] \oplus [- 1\ 0\ 0] \oplus [1\ 0 - 1] \oplus [- 0\ 1\ 1]$$

As shown in the above examples, different ESOPs can have different random testabilities. The ESOP with minimum number of product terms does not always guarantee highest random pattern testability. On the contrary, ESOPs with smaller sized cubes in the cost of increased product terms provide better random testability as demonstrated by the experimental results.

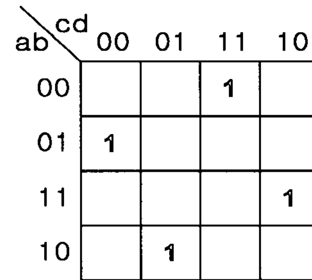

Fig. 5. Another logic function generating ESOPs with different sized cubes, resulting in different random testabilities.

IV. Experimental Results

To lead the experiment, two ESOP expressions are generated. One is with minimal number of product terms(ESOP1 in the tables) and another with the largest cube size minimized(ESOP2 in the tables). Since the r.p.r. faults are due to the large sized cubes(cubes with large number of literals), ESOP2 provides better random testability at the cost of more product terms and/or literals. The ESOP1 files are first generated targeting minimum number of product terms and ESOP2 files are generated by applying

Xlinking[12] operations to the corresponding ESOP1 files. IBM PC Pentium system is used for the experiment and the SOP or ESOP files are converted to ISCAS89 format first and then fault simulation with pseudo-random patterns generated by LFSR is performed. In table 1, #PI, #PO and #prd denote the number of primary inputs, the number of primary outputs and the number of product terms, respectively. The number of patterns given in table 1 and table 2 is the number of test patterns applied to get more than 95% test coverage. Table 2 shows the same results after common cubes are extracted(with gcx command in MisII[13]).

The results show that in most cases ESOP requires much less number of random patterns. However, in some cases, the improvements are little to be noticed. For example, duke21 shows little change in the number of random patterns. But, when common cubes are extracted, it needs much smaller number of patterns.

From table 2, we can see that the random testability of two-level circuits are preserved even when common cubes are extracted and more than that, smaller number of patterns are needed in most cases. Not shown in this paper is the effect of every operation which are used in multi-level logic synthesis, which we are currently exploring. Since cordic contains parity type subfunctions, its SOP representation has a large number of cubes while its ESOP representation is rather simple. Also t481 shows abrupt difference in its

Table 1. Random testability of two-level circuits.

Circuit			SOP			ESOP1			ESOP2		
Name	#PI	#PO	#prd	#lit	#pat	#prd	#lit	#pat	#prd	#lit	#pat
9sym	9	1	87	522	480	52	380	256	140	532	32
t481	16	1	481	4752	65K	40	13	32	40	13	32
cordic	23	2	1206	18369	344K	192	1513	2784	378	2572	736
ttt2	24	21	124	557	15K	61	296	3424	72	348	1728
duke21	22	29	87	759	13K	78	687	12K	198	1581	11K
add8	16	8	1244	10956	36K	257	1722	1280	416	2659	512
comp8	16	3	766	8192	56K	576	6667	1848			
cm162a	14	5	31	99	480	20	94	160	20	94	160
cm163a	16	5	81	27	224	14	52	96	14	52	96

Table 2. Random testability of circuits after common cubes are extracted.

Circuit	SOP		ESPO1		ESOP2	
Name	#lit	#patterns	#lit	#patterns	#lit	#patterns
9sym	358	384	246	320	420	32
cordic	2984	276K	600	1984	892	416
duke21	566	12K	540	2656	731	2304
t481	1140	50K	36	32	36	32
ttt2	427	1728	202	416	227	160
add8	3177	15K	932	640	1376	192
comp8	2052	41K	3344	8256		
cm162a	75	320	54	160	54	160
cm163a	67	192	42	64	42	64

number of product terms between SOP and ESOPs. However, note that random testability is not decided by the number of product terms but by the size of the cubes. ESOPs of t481 have a set of small sized cubes. The experimental results given above can be improved with more efficient ESOP minimization tools which are being developed by many research groups worldwide.

V. Conclusion

In this paper, the random pattern testability of ESOP expressions are compared to that of SOP expressions of the given logic function. It is shown that ESOP provides always better random pattern testability than SOP expressions assuming they have same sized cubes. Experimental results show favorable results to ESOP expressions in most cases. And the experiment shows that when common cubes are extracted the testability is preserved or even improved in most cases, which enlights the possibility of ESOPs being used for multi-level logic synthesis.

Currently, we are developing algorithms to transform two-level AND/XOR circuits into multi-level circuits preserving random pattern testability and random pattern resistant faults are eliminated at the same time. We expect that when multi-level circuits are constructed from AND/XOR circuits, generated circuits will be highly random testable compared to those synthesized by conventional methods.

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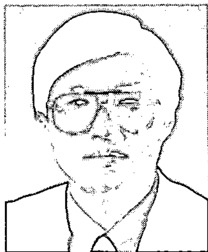

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