# Electrical Stress in High Permittivity TiO2 Gate Dielectric MOSFETs

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## ABSTRACT

Suitable replacement materials for ultrathin $SiO_2$ in deeply scaled MOSFETs such as lattice polarizable films, which have much higher permittivities than $SiO_2$, have bandgaps of only 3.0 to 4.0 eV. Due to these small bandgaps, the reliability of these films as a gate insulator is a serious concern. Ramped voltage, time dependent dielectric breakdown, and hot carrier effect measurements were done on 190 layers of $TiO_2$ which were deposited through the metal-organic chemical vapor deposition of titanium tetrakis-isopropoxide (TTIP). Measurements of the high and low frequency capacitance indicate that virtually no interface states are created during constant current injection stress. The increase in leakage upon electrical stress suggests that uncharged, near-interface states may be created in the $TiO_2$ film near the $SiO_2$ interfacial layer that allow a tunneling current component at low bias.

**Keyword:** Electrical Stressed Effects, MOCVD, High Permittivity, $TiO_2$, MOSFETs

## I. INTRODUCTION

The preparation of high permittivity thin films have received considerable interest for the fabrication of charge storage insulators for the new generation of dynamic random access memories[3],[4]. In another application, the use of high permittivity materials is considered as one of the best alternative to conventional ultra-thin silicon dioxide [5],[11]. For MOSFETs scaling into the deep submicron, there is a strong need to reduce the gate oxide thickness. Tunneling currents however, limit the scaling of $SiO_2$ to approximately 25Å as shown in Fig. 1 and Fig. 2. Suitable replacement materials such as lattice polarizable films which have much higher permittivities than $SiO_2$ have bandgaps of only 3.0 to 4.0 eV. Due to these small bandgaps, the reliability of these films as a gate insulator is a serious concern. Although wearout information is now being obtained on some storage capacitor materials, very little is known regarding charge trapping and breakdown for high permittivity films when used as a gate dielectric and therefore when deposited directly on silicon. In this paper we report on leakage currents and the effects of electrical stress on FETs using one such high permittivity material, $TiO_2$.

## II. EXPERIMENTS

The $TiO_2$ MIS capacitors were fabricated on 9-15 Ω-cm boron doped Si substrates. The backside of the wafers received a $10^{15}$ $cm^{-2}$ boron implant at an energy of 50 KeV to ensure a good ohmic contact of aluminum to the substrate body.

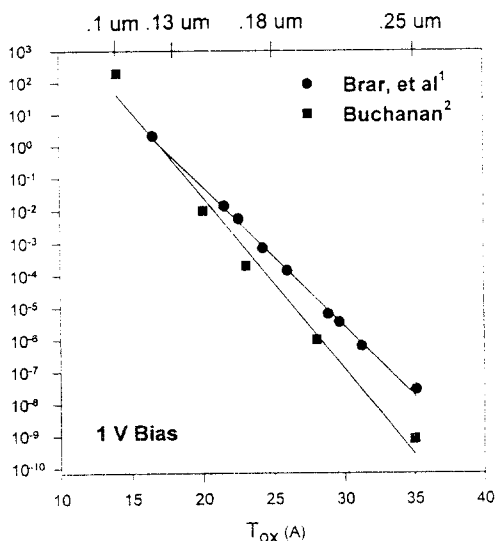


Fig. 1. Measured leakage current density for ultrathin SiO2 from Brar *et al.* [1] and Buchanan *et al.* [2].

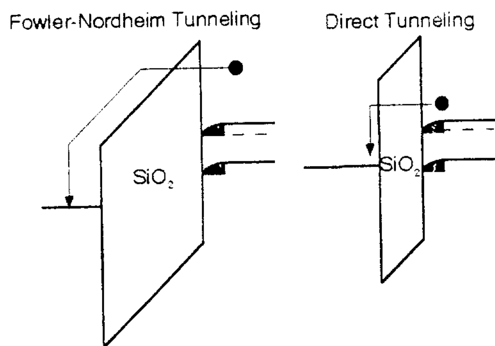


Fig. 2. Thickness dependent transport mechanism. Direct tunneling transport mechanism rather than FN tunneling increases leakage current in very thin SiO2 dramatically.

190Å layers of $TiO_2$ were deposited through the thermal decomposition of titanium tetrakis-isopropoxide on 2" p-type (111) silicon wafers which had undergone a standard LOCOS isolation [5], [6]. After deposition of $TiO_2$ the wafer was annealed for 30 minutes in dry oxygen at 750℃. This annealing was found to reduce leakage currents through the film. Transmission electron microscope (TEM) results indicate that this deposition anneal process produces an interfacial silicon dioxide layer approximately 25Å thick. After $TiO_2$ deposition, 2500Å of platinum was sputter deposited for the gate electrode. Platinum was selected as the gate electrode due to its large work function and refractory nature. It has been used extensively with high permittivity materials. The wafers then received a 30 minute nitrogen anneal at 850℃ after the transistor source/drain implant to activate the implanted impurities and to densify a deposited oxide layer. After the fabrication was complete a 450℃ hydrogen anneal was performed. All electrical measurements were done with an HP4156 semiconductor parameter analyzer and an HP4194 impedance analyzer.

## III. RESULTS AND DISCUSSION

The layers were analyzed for chemical and structural composition by X-ray diffraction (XRD) and Rutherford backscattering spectrometry (RBS). XRD results indicated that the films were polycrystalline anatase with no evidence of any rutile phase[6], and RBS showed a [Ti]/[O] stoichiometric ratio of 1:2 as shown in Fig. 3, within the sensitivity of the analysis. Atomic Force Microscopy (AFM) measurements, which can provide some information regarding the roughness of the platinum/$TiO_2$ interface and a rough indication of grain structure, showed that the $TiO_2$ films had mean roughness values of about 30Å, with lateral feature sizes of 500Å for the surface of approximately 500Å thick $TiO_2$ films after the 750 ℃ anneal.

The leakage current through the device has been measured as a function of temperature for both accumulation and inversion biases. The anneal was found to significantly reduce the leakage current and $J/T^2$ is found to follow standard thermionic emission behavior. Forward Recoil Spectroscopy showed that the concentration of hydrogen in these films is correlated with increased interface state densities and leakage current, and that the hydrogen concentration of films decreases sharply with post annealing at 750

℃. The effective barrier height was approximately 0.5 eV for the as-deposited film, while the $O_2$ annealed film had a barrier height of 1.0 eV. X-ray diffraction measurements of the $TiO_2$ films on (111) substrates show no significant change in crystallization with the 750 ℃ anneal, although atomic force microscopy shows a reduction in surface roughness. We therefore believe that this increase in the barrier height with $O_2$ annealing is due to a change in the band alignment, perhaps due to a change in the charge state or strain at the $TiO_2$/Si interface due to interfacial $SiO_2$ layer. When biased into accumulation, the current initially is temperature independent, suggesting that the current in this regime is dominated by tunneling. Above 100 ℃ however it shows standard thermionic emission behavior up to 160 ℃ where it again becomes temperature independent. It is believed that the current in this temperature independent regime may be limited by tunneling through to $SiO_2$ interfacial layer. The leakage under inversion bias was independent of temperature up to 70 ℃ while it shows standard thermionic emission behavior. The absence of temperature dependence at 25 ℃ to 70 ℃

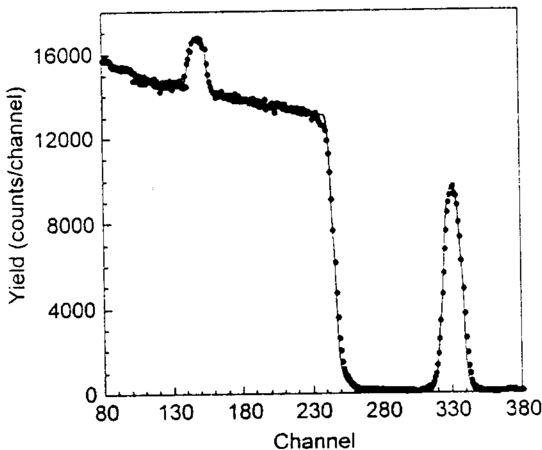


Fig. 3. Rutherford Backsacttering Spectrum for a TiO2 film on (111) Si deposited with TTIP at 457 oC. The RUMP generated theoretical curve ( ) corresponds to stoichiometric TiO2.

suggests that the post-stress current is dominating by tunneling over the temperature range studied. The barrier for emission was between 0.94 and 1.0 eV for all samples measured[7].

The ramped voltage measurements with a 1 V/sec ramp rate showed Fowler-Nordheim current-voltage characteristics of 150x150$\mu m^2$ capacitors. To minimize the voltage drop in the substrate, negative biases were used in order to keep the capacitors in accumulation. A clear irreversible breakdown occurred at an applied field of approximately 3.2 MV/cm, and the charge to breakdown $Q_{BD}$ is ~6 C/cm$^2$. A distribution of breakdown fields is reasonably tight.

No clear breakdown was seen in time dependent dielectric breakdown (TDDB) tests. The leakage current through the $TiO_2$ increased after electrical stressing. This effect was most pronounced at low bias conditions. At a 2 volt accumulation bias the leakage current increased by a factor of 10 after 1.0 Coul/cm$^2$ and another factor of 50 after 100 Coul/cm$^2$, but no clear discontinuity in the voltage-time(constant current) or current-time(constant voltage) curves are seen. Measurements of the high frequency capacitance indicate that little charge trapping occurs during electrical stress as shown in Fig. 4 (a). By using the calculated flat voltage shift, the change in the bulk trap density ($\Delta N_{ot}$) was identified under constant current injection stress. Theoretically the kinetics of trapping and detrapping can be expressed by a first order rate equation[8]:

$$\Delta V_{fb}(t) = \frac{qN_{eff}}{C_{ox}}[1 - \exp(-\frac{\sigma Jt}{q})] \qquad [1]$$

where $C_{ox} = \varepsilon_{ox}/d_{ox}$ is the oxide capacitance per unit area, is the effective trap density per unit area with the centroid of the trapped charge X and with the total trap density within the oxide $N_t$, $\sigma$ is the capture cross section, and $\Delta V_{fb}(t)$ is the flat band voltage shift. Differentiating

$$\frac{d}{dt}\Delta V_{fb}(t) = \frac{\sigma J N_{eff}}{C_{ox}}\exp\left(\frac{-\sigma J t}{q}\right) \qquad [2]$$

By assuming an Neff of order $10^{14}$ $cm^{-2}$, the capture cross section $\sigma$ was estimated to roughly $10^{-23}$ $cm^2$ [9]. This is much smaller than conventional $SiO_2$ trap values[10]. $TiO_2$ insulator may be much less vulnerable to TDDB stress as shown in Fig. 4 (a) as like tunnel anneal oxide ( 40Å in Fig. 4 (b)) $SiO_2$ because carriers in $TiO_2$ film may loose less energy than those in conventional $SiO_2$(Fig. 4(c)) due to its small energy band-gap and small capture cross section.

Both 1 MHz and 100 Hz capacitance voltage curves measured using capacitors made with 190 Å layers of $TiO_2$ displayed a pronounced voltage dependent accumulation capacitance, which contradicts standard MOS theory. It also complicates the calculation of the $TiO_2$ dielectric constant. The usual analysis of the MOS capacitor in accumulation or in inversion assumes a charge sheet of negligible extent the semiconductor /dielectric interface. This is a good approximation when the actual position of charge added to the accumulation layer (<x>) by a change in gate bias is much less than the thickness of the oxide, or more precisely, when $t_{ox}/\varepsilon_{ox} >> \langle x\rangle/\varepsilon_{Si}$. In the deep the accumulation region, the large band bending of silicon induces a high electric field at the $SiO_2$/Si interface. The potential well near the silicon surface is approximately triangular. The electron density in the potential well is proportional to , where is the solution of Schrodinger equation that have the form of Airy functions. The average electron location of the electron in each energy state is

$$\langle x\rangle = \frac{\int x_i|\psi_i(x)|^2\,dx}{\int|\psi_i(x)|} = \frac{2E_i}{3qF_s} \qquad [3]$$

It is important in extracting dielectric constant from MOS capacitor measurements to take into account the finite accumulation layer thickness, particularly when the ratio of dielectric constant to

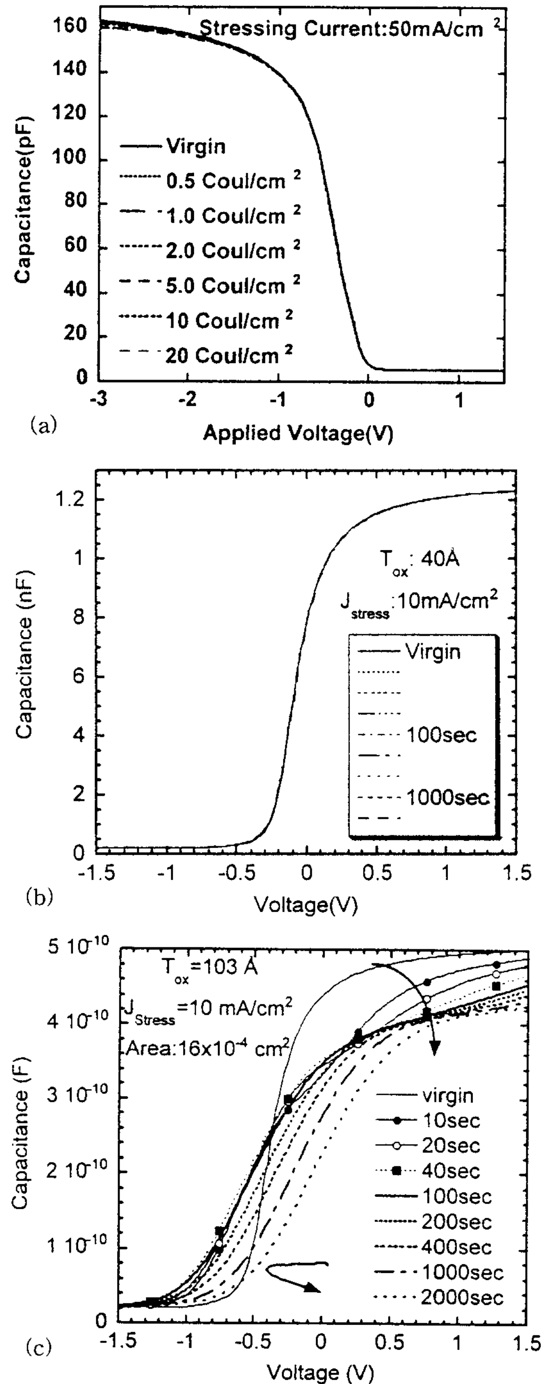


**Fig. 4.** High frequency C-V characteristics of 190 TiO2 films (a), 40 (b) and 103 SiO2 (c) and after TDDB stress. Thinner and lower conduction barrier show less vulnerable to TDDB stress.

insulator thickness is larger than 10Å [1]. In that case

$$\frac{1}{C_{meas}} = \frac{t_{TiO_2}}{\varepsilon_{TiO_2}} + \frac{t_{SiO_2}}{\varepsilon_{SiO_2}} + \frac{\langle x \rangle}{\varepsilon_{Si}} \quad [4]$$

where the mean electron distance from $SiO_2$/Si interface is

$$\langle x \rangle = \frac{\sum n_i \langle x_i \rangle}{\sum n_i} \quad [5]$$

Thus, a pronounced voltage dependent accumulation capacitance might be caused from hole trapping in the $TiO_2$ very near the $SiO_2$ rather than relating to the voltage dependence of the accumulation layer width because we didn't see any pronounced capacitance even for 26 $SiO_2$ MOS system. These trapped holes may be easily detrapped from small capture cross section specially when the interfacial $SiO_2$ thickness is thin enough not to be traced by a hysteresis loop. Taking this into account, the permittivity of the $TiO_2$ films is approximately 30, in good agreement with other published papers. The interface state density extracted from the C-V curves with Castagne and Vapaile's method fell mid $10^{10}$ $cm^{-2}$-$eV^{-1}$ at midgap, but rose sharply on either side, unlike the "U" shaped behavior in thermal oxide capacitors. Measurements of the high and low frequency capacitance with constant current TDDB stress with 0.4, 4.2, 20, and 38 $C/cm^2$ indicate that virtually no interface states were created during stress. Very little bulk charge trapping exists after electrical stress suggesting that these films have few intrinsic traps and are highly resistant to current induced trap creation. The increase in leakage upon electrical stress suggests that uncharged, near-interface states may be created in the $TiO^2$ film near the $SiO^2$ interfacial layer that allow a tunneling current component at low bias. Alternatively, the increase in current may be due to the creation of neutral traps near the platinum gate electrode.

Finally, $TiO_2$ FETs were fabricated from these layers over a standard LOCOS structure. Fig.5 shows the subthreshold characteristics for a drain bias of 100 mV for a 100 x 100 ㎛ transistor as well as a device with a drawn gate length and width of 1 and 5 ㎛, respectively. A subthreshold inverse slope of 83 mV/decade is seen for the large device, while the smaller transistor has an inverse slope of 91 mV/decade for worsecase. However, we notice that most of inverse slopes are about 70 mV/decade which is comparable to that of thermal oxide MOSFETs. The large inverse slope for the smaller device is believed to indicate the onset of short channel behavior as deep source/drain junctions were intentionally used for the process. Fig. 6 shows a family curves for 10 (gate width) x 1.25 (gate length) $㎛^2$ transistor. While generally good current-voltage characteristics are seen for the $TiO_2$ MISFET' s, the low field effective electron mobility inferred from the transconductance is

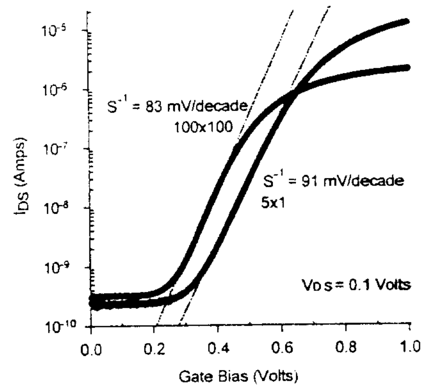


Fig. 5. Subthreshold behavior of 100 x 100 ?m and 5 x 1 ?m transistor. Both curves were obtained at a drain bias of 0.1 V.

approximately 280 $cm^2/Vs$. This is two times lower than the values commonly obtained from $SiO_2$ based MOSFET's. The source of this mobility reduction is consistent with the relatively large values of the interface state density as measured by capacitance-voltage and conductance techniques. The hot carrier effects were also measured at $V_d$= 3.5 V and $V_g$= 2 V, but the threshold voltage shift and transconductance were clearly improved rather than degraded[11]. Conductance performance was improved after hot carrier stress. We even noticed this kind of

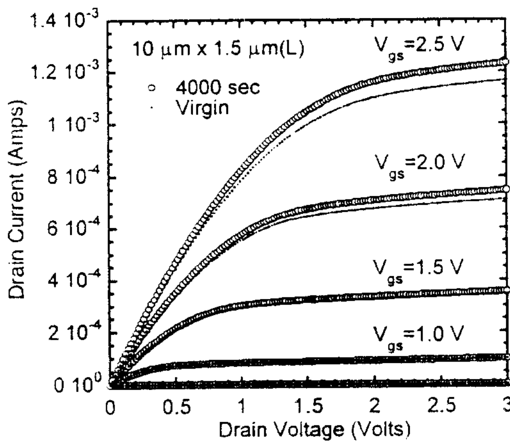


**Fig. 6.** The transistor characteristics improved by hot carrier stress, Id-Vd for mask size (W/L = 10/1.5) at Vd = 3.5 V and Vg = 2 V for 4000 second.

phenomena even for low field TDDB stress. The value of effective mobility can be increased after filling trap sites by carriers.

## IV. CONCLUSION

High permittivity $TiO_2$ dielectric MISFETs were fabricated on boron doped Si (111) substrates with a stand LOCOS structure. Measurements of the high and low frequency capacitance with constant current TDDB stress indicate that virtually no interface states were created during stress. Very little bulk charge trapping exists after electrical stress suggesting that these films have few intrinsic traps and are highly resistant to current induced trap creation. The increase in leakage upon electrical stress suggests that uncharged, near-interface states may be created in the $TiO_2$ film near the $SiO_2$ interfacial layer that allow a tunneling current component at low bias. Alternatively, the increase in current may be due to the creation of neutral traps near the platinum gate electrode. While generally good current-voltage characteristics are seen for the $TiO_2$ MISFET's, the low field effective electron mobility inferred from the transconductance is approximately 280 $cm^2/Vs$. This is two times lower than the values commonly obtained from $SiO_2$ based MISFET's.

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