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NEW DESIGN CONCEPT FOR UNIVERSAL CCD CONTROLLER

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ABSTRACT

Currently, the CCDs are widely used in astronomical observations either in direct imaging use or spectroscopic mode. However according to the recent technical advances, new large format CCDs are rapidly developed which have better performances with higher quantum efficiency and sensitivity. In many cases, some microprocessors have been adopted to deal with necessary digital logic for a CCD imaging system. This could often lack the flexibility of a system for a user to upgrade with new devices, especially if it is a commercial product. A new design concept has been explored which could provide the opportunity to deal with any format of devices from any manufactures effectively for astronomical purposes. Recently available PLD (Programmable Logic Devices) technology makes it possible to develop such digital circuit design, which can be integrated into a single component, instead of using microprocessors. The design concept could dramatically increase the efficiency and flexibility of a CCD imaging system, particularly when new or large format devices are available and to upgrade the performance of a system. Some variable system control parameters can be selected by a user with a wider range of choice. The software can support such functional requirements very conveniently. This approach can be applied not only to astronomical purpose, but also to some related fields, such as remote sensing and industrial applications.

1. INTRODUCTION

In recent years the CCD imaging systems have been actively applied to many areas such as commercial products and industrial systems. Particularly, the scientific purpose imaging systems have been benefited from the properties of high sensitivity and quantum efficiency of the CCDs over conventional sensors. In many cases of

commercial and industrial imaging systems, the CCD controller electronics are often available as an option from the manufacturer for any specific sensors, which have been designed and integrated into a module, or a package. However, for the purpose of scientific applications, the system design should be optimised precisely according to its original specific requirements, especially for low light level detection.

In practical implementation, the system control parameters of a CCD imaging system, such as waveform timing and bias levels, have to be customised and tailored for its best performance. The universal controller is termed here that the system parameters of a CCD imaging system can be selected by the user's request, particularly to support any format of any manufacturer's CCD conveniently. This also makes possible precise tunings of system control parameters in the process of the noise performance experiments in optimum low light level applications. A new design concept for such a universal CCD controller is introduced in this work, particularly aiming at versatile flexibility of the system design.

2. SYSTEM DESIGN APPROACHES

There could be many possible techniques to provide proper drive waveforms for reading out the integrated charge on the CCDs. The characteristics of CCDs and its system design of associated electronics have been extensively described by Mackay (1986). McLean (1989) discussed possible methods to design a system which can be classified into two categories, in general. The first one is based on the hard-wired design meaning that the electronic functions are carried out by circuitry and cannot be altered by typing instructions on a computer keyboard. The design utilises some commercial TTL, or CMOS devices for digital logic circuit. The system parameters can be selected by manual switches from front panel knobs with simple structure and little software effort. However it could have a difficulty to support various operational modes.

Meanwhile the other approach is based on programmable designs such that electronic functions can be controlled by computer commands. In this case, the system design is based on a microprocessor and associated software. Generally the instructions of system parameters, such as clocking information, are stored into memory devices as necessary. This approach can support various operational modes at the cost of considerable software effort in designing stage. In most cases of recent commercial products, the system designs are based on this concept. The users may

experience some difficulties in modifying system control parameters, particularly when low-level language programming is involved in control software.

For the flexibility of a system, it has to allow adjustment of as many system parameters as possible by the software. As an example, the number of pulses together with their timing and phase, the bias voltage levels and clocking sequences, can be arranged by the software with a computer. Considering this, the system design of this approach can be classified as the latter case. This kind of approach normally requires use of memory devices which can store necessary information such as required drive waveform sequences. However, unlike the latter case, it is now possible to design without using microprocessors owing to the recent advances of PLD technology. Rather, the system design itself is a similar process of digital logic design in a hard- wired approach, but in a special CAD software system without employing any discrete digital components. This is unique approach in designing CCD controller. Initially, this approach has been developed by Han (1993) for multiple readout of mosaic CCD focal plane. Applying the concept to this work for a single CCD sensor, the system design can be optimised further and control parameters can be organised more efficiently for its best performance.

The system control parameters have been summarised as following. These are some important factors to control any format of CCDs from any manufacturers particularly for very low-light level applications.

- **Number of pixel and lines :** These numbers should be given as variable inputs to the controller by a user from the software for flexibility to control any format CCD. This implies the controller has to issue any numbers of horizontal and vertical clock waveforms by the commands of a user.

- **Waveform timing :** The flexible timing control of drive waveforms is practically the key feature for universal controller design, since most CCDs require different timing waveforms for its best performance. It is particularly important in low light level applications with slow scan mode such as astronomical purposes. Any timing sequences have to be supplied and modified easily to support any CCD. The transition timing control between the phases of clock waveforms is a very sensitive parameter of charge transfer efficiency.

- **Voltage levels for bias and waveforms :** The analog voltage levels of the bias and waveforms with regard to the ground level directly give effect to

the system performance. The best combinations of the bias and waveform voltage levels can be often obtained by fine tuning in optimisation processes. By using a DAC (Digital to Analog Convertor), digital data control makes it possible to provide any analog voltage combinations for any CCD.

- **Timing resolution :** In most cases of programmable designs, the timing instructions are stored into memory devices. The timing resolution sets the minimum unit of one memory address, and is dependent on the length of a waveform and system clock frequency. This parameter has to be flexible to cope with various operational modes for its best efficiency.

- **Video processing and digitisation timing control :** The image signal from a CCD sensor is amplified in the video processing circuit by well-known CDS (Correlated Double Sampling) technique to eliminate the reset noise. The dual slope integrator timing can be controlled as with waveform timing in this process. The timing of data acquisition with an ADC (Analog Digital Convertor) for digitisation has to be controlled in the same manner as a form of digital bit pattern. These two parameters are important elements in optimising the performance of a system for a low-noise imaging system.

In addition to above parameters, the controller design has to support various control commands, such as start readout, shutter control, rotating filter wheel, exposure times, *etc.* Such functions can be controlled by digital logic circuit so that relevant output signals can trigger indicated accessories according to user's commands.

3. HARDWARE DESIGN CONCEPT

The hardware structure based on their functional arrangement is very similar in any CCD imaging system. The digital controller is the heart of the whole system that provides digital waveforms, all necessary system control logic including interfacing between the system and computer. The design of this unit is directly related to the efficiency of the whole system. The analog driver supplies all bias voltages, analog waveforms to the CCD. Convenient control of this analog electronics can be achieved by using some DAC devices. This is important to adjust levels of bias voltage and analog waveforms without any hardware alteration. Besides these, headboard with cryostat, video processing circuit, digitiser have to be also arranged for a complete

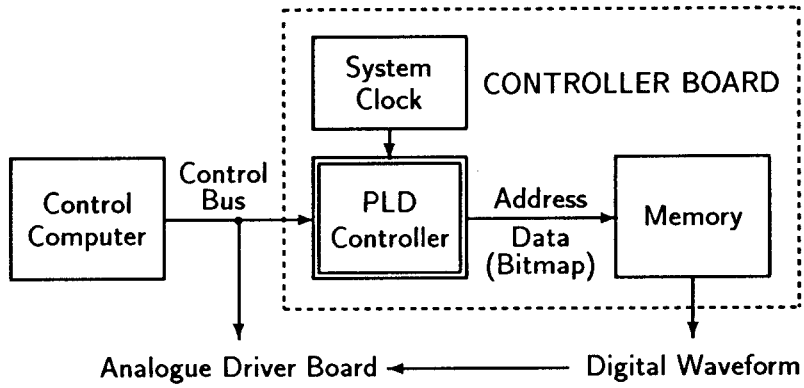

Figure 1. The block diagram of the controller design concept.

system. Among them, the most important units in the whole system are the digital controller and analog driver. The other parts are subject to these two units, thus discussions are mainly concentrated on the design of them, while other parts can be considered as passive units.

The controller design in this work is focused on taking advantages of both hard-wired and programmable designs as previously discussed. Most of other similar works employed microprocessors in dealing with digital logic for required waveforms and other control signals (Leach 1988, Leach and Beal 1990, Luppino and Miller 1992). However, this could often lack the flexibility of a system for a user to upgrade with new devices. Thus it was avoided to use any microprocessors in this design. Recently, due to the advance of EPROM (Erasable Programmable Read Only Memory) technology, it is possible to integrate a complicated digital circuit that consists of more than 20 thousands logic gates by a special CAD system. This means that it enables to concentrate a whole digital controller circuit into a single PLD chip, without using any discrete components. It can work as a special *sequencer* that produces specific digital signals according to the arranged design.

Considering this, there are not many fundamental differences with a microprocessor based design in dealing with a given job for the same purposes. Rather this approach has some advantages such as predictable timing delay and flexibility without any low level language programming. The system control parameters can be easily modulated from the software and are also able to support various operational modes. This greatly improves flexibility and compactness of a system as well as sim-

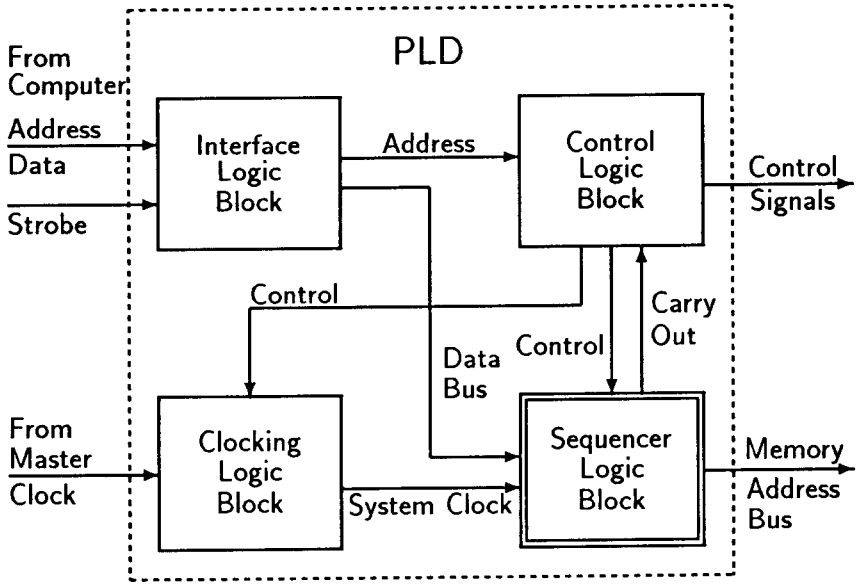

Figure 2. The block diagram of the single chip PLD controller circuit.

plicity. In principle, a total of 2 digital devices (one PLD, one memory chip) plus a system clock and buffers can process all required logic to control a CCD. The design concept developed by Han (1993) for mosaic CCD focal plane can be directly applied to the system design for a single sensor with necessary modification. Advantages in PLD design approach for a CCD imaging system can be highlighted as compactness and flexibility. Simple control software structure and design simulation ability are additional benefit, and further details have been discussed elsewhere (Clayton 1994, Han *et al.* 1994).

In this work, the concept of controller circuitry can be characterised as memory device control. The information stored in the memory devices is written by the software as a form of digital bit pattern (hereafter bitmap), which represents the specific instructions for timing waveforms. A bitmap is defined as a series of logical 0's and 1's in controller memory that specifies the low or high of CCD waveforms. After writing the bitmap into the memory devices, cycling around the memory can generate the digital waveform directly. The heart of the digital circuit is concentrated in a single PLD chip, which contains thousands of logic gates generated by the CAD

software. The design can be thoroughly simulated and tested by the facility of the CAD software. The bitmap can be designed so that various operational modes can be implemented. All system control parameters including data and address information can also be controlled here. The concept of the controller design is shown in Figure 1.

The main task of the PLD controller is to supply memory address information when writing the bitmap by the software into the memory devices and reading out from the memory devices. The bitmap data is supplied together with address information by the software at the same time. This approach allows great flexibility to users for implementation of various drive waveforms by modifying the bitmap, because the bitmap directly reflects the required analog waveforms. It is therefore very important to organise such bitmap efficiently by the software to deal with any waveforms. The whole procedure to generate proper waveforms is entirely dependent on the software. The PLD design also includes some other control signals and buffer control signals. The whole design can be organised into several subdesigns as lower hierarchy level of the top-level design according to their functions. The block diagram of the PLD digital controller circuit design is shown in Figure 2.

The design of analog driver circuitry is another important factor, particularly in low noise application, since it directly provides necessary waveforms to CCD. In many cases, sources of unsatisfactory noise performance are identified as noise susceptible analog waveforms. If only stable voltage sources are considered, there could be many possible methods to provide required analog signals such as simple voltage source circuit. However two important requirements are flexibility and compactness. The analog waveforms and bias levels have to be controllable easily by the software to optimise the system performance. Further, chip count and circuitry area have to be minimised so that they can be accommodated in the cryostat, if necessary, for the lowest system noise.

With recent advance of electronic technology, a design with programmable voltage source by using DAC would be a reasonable approach. Recently available *octal DACs* (eight channels in a single package) are particularly practical for this purpose as they allow great flexibility in a compact package to provide many voltage sources efficiently. Considering the required number of waveforms and bias levels is less than 16 for slow scan operation, only two octal DACs can provide required programmable voltage source. Some more devices of course can be additionally used according to

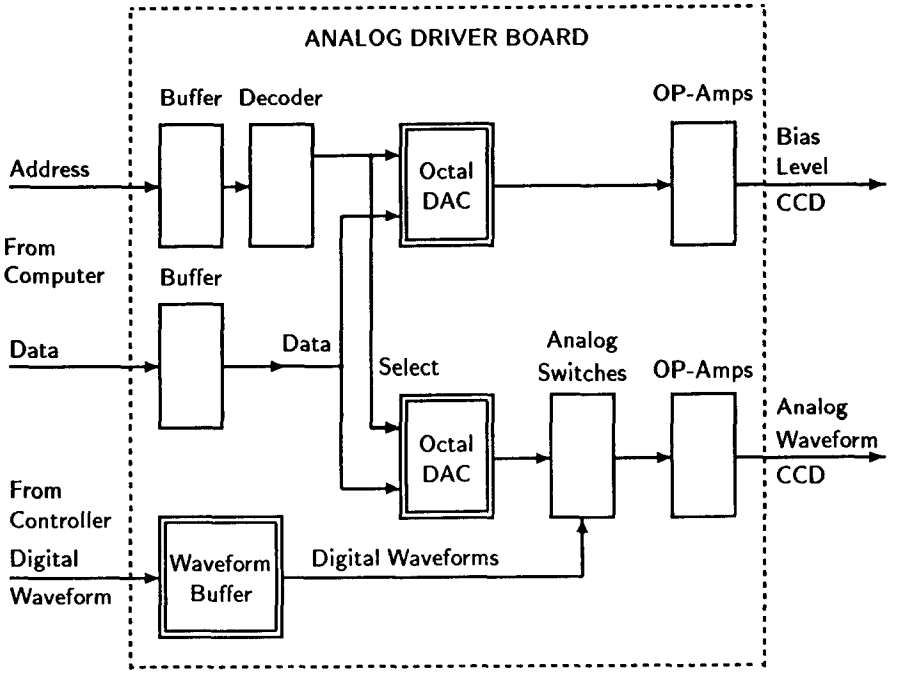

Figure 3. Block diagram of the analog driver board design. Two *octal DACs* are assigned to provide analog voltage levels for CCD.

specific purposes. The block diagram of the design concept using the octal DACs is shown in Figure 3.

4. SOFTWARE DEVELOPMENT

The software or hardware in a programmable system design cannot stand alone independently. Both parts are closely related, thus they have to be considered at the same time in the initial designing stage, otherwise it may be difficult to support fully each other's requirements to perform their assigned functions. The controllability of the software is directly related to hardware structure. A fully software controllable system may require very complicated software and hardware structure, whilst a hardware optimised system could have a difficulty in control flexibility of the system at the expense of simple or no software. Therefore a balanced compromise has

to be made at reasonable stage between the two approaches. In this design, the system control parameters are supplied from the software. These include a unit of repeat pattern for waveforms as a form of the bitmap, DAC control information and controller initialise parameters. Such digital information is given as variable inputs from the keyboard, together with some control commands that supply trigger signals for any operational mode. The control software programming concept for the mosaic CCD system by Han *et al.* (1994) can also be applied to this approach with much simple structure.

To provide analog voltage levels for waveforms and bias levels, the DACs have to be programmed to their proper state. The levels are directly controlled from the software with 8 bit resolution of maximum voltage level. The address information of a DAC for a specific level can be supplied with required digital data, allowing wide range of flexible levels. Once the level has been defined, it is held by digital latch in the DAC until updated data is applied to the same address. The hardware design of the controller requires its initial conditions to be set before any operations. Here the term 'initial conditions' directly refers to the system parameters of one pixel readout time for both horizontal and vertical, and number of pixels and lines of a CCD. Generally these four parameters determine a sequence of repeat pattern to readout the image charge. It can be considered that the first two parameters characterise how to transfer charge inside a pixel or a line, specifically in terms of their timing. The latter two determine how to transfer the charge in terms of their number of transfers for a CCD frame. Internal latches of a PLD can store this information digitally, down-loaded from the software. The sequencing is done by the hardware electronics according to the contents of the bitmap.

The key feature of the software is bitmap coding that defines the details of the drive waveforms, video processing signal and digitisation timing during the charge transfer. The sequence of analog waveform, which is applicable to most kinds of CCDs, can be defined as a form of a bitmap, and generated by a circuitry, for example, a sequence of one vertical waveform followed by a horizontal one. Each of bits of a bitmap instructs particular waveform information or related signals as shown in Table 1. Generally the length of a bitmap depends on the clocking period for one pixel readout time. A bitmap directly reflects waveforms and relevant signals in hardware. It is not a difficult task to code such a bitmap if we know exact waveform specification, preferably in graphical format. The main process is

Table 1. An example of a bitmap structure for a three phase CCD.

Order	Abbr.	Information	Order	Abbr.	Information
1st	ϕH_1	Horz. Clock Phase 1	9th	SR	Sample Reset
2nd	ϕH_2	Horz. Clock Phase 2	10th	DS	Dark Sample
3rd	ϕH_3	Horz. Clock Phase 3	11th	SS	Signal Sample
4th	ϕR	Reset Clock	12th	AD	ADC Trigger
5th	ϕV_1	Vert. Clock Phase 1	13th		Spare
6th	ϕV_2	Vert. Clock Phase 2	14th		Spare
7th	ϕV_3	Vert. Clock Phase 3	15th		Spare
8th		Spare	16th		Spare
First Byte			Second Byte		

programming 0 or 1 according to the waveform specification, using any editors or word processors in ASCII format. The information is generated by the software and stored into memory devices (RAM). The user can easily arrange required waveforms by modifying the bitmap source file. A programming approach with GUI (Graphic User Interface) format in this process has been investigated (Han *et al.* 1994). An example of a bitmap structure is shown in Table 1.

The system control is achieved by sending the command signals from the software to the controller, such as 'start operation' or 'select RAM writing mode'. Each of these commands can be arranged to have specific address information for the decoder in the PLD controller. Once such addresses have been decoded, individual control signals are generated, then each related circuits are triggered by these signals. Some latches have to be prepared in the PLD controller to hold the signals, and cleared immediately after execution of the commands. Because these command signals are closely correlated with hardware structure, the software should be programmed carefully to avoid any mismatch, and thoroughly tested before actual hardware is involved.

5. SYSTEM INTEGRATION

The CCD imaging system is composed of many related units including the digital electronics and analog circuitry. A balanced combination of each unit in the whole system with associated software is the critical factor for reliable performance. Any problem even in one part of the system may result in improper operation. The design of video processing and digitisation circuitry is not discussed here, because these can be considered as passive units in the whole system structure. However the designs of such circuit are also very significant factor for low light level performance, considering potential noise contribution from them. An important procedure before digitisation is to eliminate reset noise of the CCD. This is caused by uncertainty on mean values of reset level, which is a function of the output node capacitance and operation temperature of a CCD. These procedures are accomplished by means of the well known correlated double sampling (CDS) technique by elimination of mean signal differences before and after a charge readout of one pixel. Some available examples of the video processing circuit can be found elsewhere (McLean 1989, Leach and Beal 1990) and the further discussions were also made by Han (1993) and Clayton (1994).

Based on the design concept of this approach, most designs of a system can be accommodated into a single circuit board by careful arrangement of the components. With recently developed *surface mount devices* and *multilayor printed circuit board* technique, it is possible to design a complicated circuitry within a minimal space. Recently, many commercial software packages are also available for this purpose. In this case, attention has to be paid to the ground arrangement of digital and analog electronics to avoid any potential noise contribution. In practice, this is one of the determining factors for the system performance. After integration of the units of the system, experiments have to be made to optimise performance with proper adjustment of individual units. According to the test results, various different operating conditions have to be attempted to find which combination provides more stable and reliable performance.

The system design approach of this concept allows the opportunity of such optimisation process conveniently even to the novice users without having background experience in system design. It is with these two long term goals – flexibility and compactness – in a view that we consider the prospect for a versatile universal CCD controller. As for the future application of this design approach in astronomy, it can

be utilised for direct imaging and spectroscopic purposes with optimum low level performance. Auto-guiding system of a large telescope, infrared observation and x-ray detector systems are potential application areas. At outside astronomy, this design concept can be implemented in several fields, such as remote sensing CCD electronics, security monitoring, or under-water surveillance camera system.

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