Integration of 5-V CMOS and High-Voltage Devices for Display Driver Applications

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CONTENTS

ABSTRACT

Reduced surface field lateral double-diffused MOS transistors for the driving circuits of plasma display panel and field emission display in the 120 V region have been integrated for the first time into a low-voltage 1.2 μm analog CMOS process using p-type bulk silicon. This method of integration provides an excellent way of achieving both high power and low voltage functions on the same chip; it reduces the number of mask layers and also the cost of fabrication. The lateral double-diffused MOS transistor with a drift length of 6.0 μm and a breakdown voltage greater than 150 V was self-isolated to the low voltage CMOS ICs. The measured specific on-resistance of the lateral double-diffused MOS is 4.8 mΩ·cm^2 at a gate voltage of 5 V.

I. INTRODUCTION

High voltage and power integrated circuits find numerous applications such as display, power regulation, motor control, automotive and telecommunication. Many technologies have been developed for those applications, but what limited the rapid growth of these ICs is the cost of integration compared to hybrid alternatives with the combination of discrete components. Especially, flat-panel displays such as plasma display panel (PDP), electroluminescent (EL), and field emission display (FED) have been extensively studied to provide low cost and full color displays competing with CRTs [1]-[3]. Consequently, low cost electric drivers are bound to play an important role in the flat panel display system. When compared to power bipolar transistors, power MOSFETs have the advantageous features of high-input impedance, high switching speed, ease of paralleling, and much superior safe operating area [4]-[6]. The self-isolated devices are especially desirable because of their relative ease of integration with low voltage devices, less area, and less cost.

This paper presents a cost-effective integration scheme that achieves lateral double diffused MOSFETs (LDMOSFETs) in high performance 1.2 μm analog CMOS technology [7] and self-isolation process on bulk silicon substrates. By combining the high performance 1.2 μm low-voltage analog CMOS, self-isolation, and reduced surface field (RESURF) LDMOS transistors [8], this integration approach can provide an excellent method to achieve high performance, mixed power and low-voltage functions on the same chip, and reducing mask layer and cost.

II. DEVICE STRUCTURE AND PROCESS INFORMATION

An LDMOS transistor aimed at PDP and FED driving IC application in the 120 V region is integrated into a low-voltage 1.2 μm analog CMOS process. The process cross-section of this technology, including the LDMOS, is presented in Fig. 1. As seen here, the power IC consists of LDMOS, NMOS, PMOS, and self-isolation structure on bulk p-type silicon substrate. The p^+ source of the LDMOS provides a source-p-tub shunt and better contact to the p-tub. Another p^+ layer underneath the source suppresses a parasitic bipolar phenomenon. A n-tub for a drift region and a p-tub for a channel of the LDMOS are formed in order to apply RESURF principle and to enhance compatibility with CMOS process because these tubs are formed simultaneously with n-well and p-well of the CMOS. The RESURF technique provides the lightly doped drain (LDD) LDMOS transistor in a lightly doped n-drift region on top over a bulk p-type silicon substrate.

The bulk p-type silicon substrate instead of an epitaxial p/p^+ silicon substrate was used because the cost of the epi-wafer is high and electrical characteristics of the

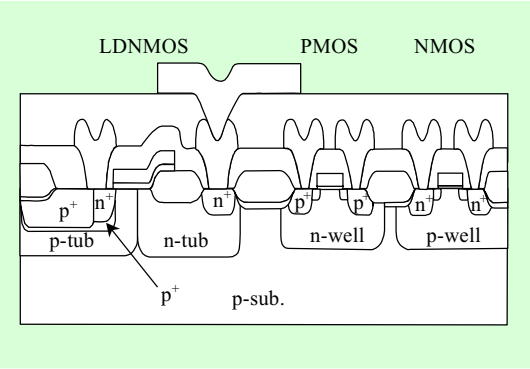


Fig. 24. Cross section of power IC.

epi-wafer varies according to the variation of epi thickness and doping concentration in epi-layer. The process to manufacture these devices is completely compatible with a low-voltage analog CMOS process except a p^+ layer formation underneath the source. This means that no extra masks and a few processing steps are added. Because of the large quantity of wafers now manufactured, and the cost sensitive nature of the power MOS business, it is very desirable to simplify the process by reducing the number of steps, corresponding to reducing the number of masking steps.

The power IC was fabricated on bulk p-type silicon substrate (R_S=30∼50 Ω·cm) using a standard 1.2 μm analog twin well CMOS process. A n-tub, which forms the drift region of the LDMOS and a n-well for low voltage PMOS are implemented by using phosphorus with implant doses of 1.0∼ 6.5×10^{12} cm^{-2} simultaneously. This implant dose is carefully controlled so that the RESURF principle is satisfied. The p-tub and p-well implant of dose $1.0\sim4.0\times10^{13}/cm^2$ using boron at 70 keV is followed for the channel of high voltage LDMOS and p-well for low voltage NMOS, respectively. The n-tub, p-tub, n-well and p-well are annealed at 1,150 °C to obtain 3.0∼4.5 μm junction depth. The remaining process is a standard 1.2 μm analog CMOS with key steps as follows: 1) active area opening, field implantation, and a field oxidation of 6000 Å; 2) boron threshold implantation at 1.7×10^{12} cm^{-2} and gate oxidation of 200 Å; 3) 3800 Å polysilicon deposition and definition; 4) source and drain implantation and annealing to achieve 0.3∼0.4 μm junction depth; 5) contact opening window opening and metallization. Only one additional mask process compared to the standard CMOS mask processes was required to implant boron into the p-tub region to form p^+ buried layer underneath the source, preventing the device from parasitic bipolar action.

In the development of the LDMOS device and CMOS/LDMOS process, DESSIS [9] and SILVACO SUPREM-4 were used to simulate the electrical characteristics, doping profile, junction depth of the device, and studies on low-voltage CMOS and high-voltage LDMOS device interaction. The optimization of lateral power device is mainly achieved by controlling the n- and p-tub doping concentration and thickness as well as the substrate resistivity.

III. RESULTS AND DISCUSSION

The high voltage NMOS device is illustrated in Fig. 2. As can be seen in the fig-

ure, the device is constructed within two tubs. The ploysilicon gate extends over the thin gate oxide and terminates on the thick field oxide. The effect of the polysilicon gate edge on breakdown voltage is thus greatly reduced. The n-tub has a lower surface doping concentration than the n-LDD region. Therefore, the surface electric field is decreased and a high breakdown voltage is expected. Various layout parameters, indicated in Fig. 2, were investigated to determine their effects on the performance of the high voltage NMOS device. The most important layout parameter is the channel length L, which affects overall performance of the device including breakdown and punchthrough voltage, specific on-resistance, switching speed and transconductance. The other layout parameters include the device tub spacing (the opening for the field oxide) L_{ds}, the polysilicon layer over the n-tub on the thin gate oxide L_{gp} and on the thick field oxide L_{fp}. The portion of the polysilicon layer out of the channel region functions as a field plate, which affects the electric field distribution in the n-tub. The drift region length L_d is simply equal to the sum of L_{gp} and L_{ds}.

The typical room-temperature measured reverse blocking characteristics are shown in Fig. 3 which indicates a sharp transition into avalanche breakdown regime. The device has a breakdown voltage in excess of 150 V with ion dose for the drift region of 4×10^{12} cm^{-2} and the parameters, L=2.0 μm, L_{gp}=1.5 μm, L_{fp}=1.5 μm,

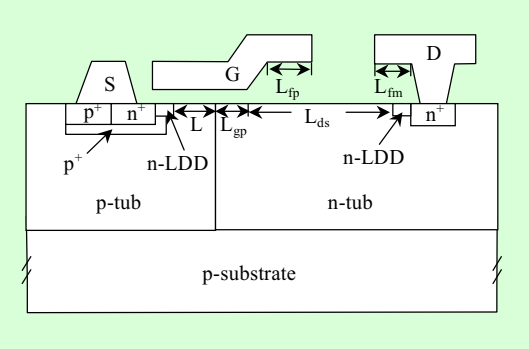


Fig. 25. Cross section of LDMOSFET using simple layout manipulations.

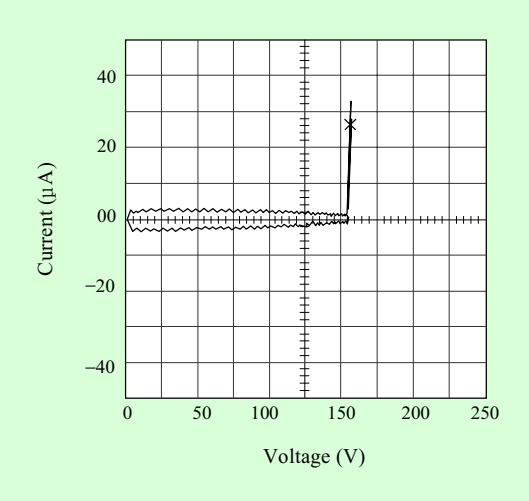


Fig. 26. The reverse breakdown characteristics of simulated 153 V LDMOS transistor with a twin-tub.

L_{fm}=1.5 μm and L_{ds}=5.5 μm are optimized and used in order to obtain higher breakdown voltage. Since the n-drift layer is now sandwiched among the n^+-drain, p-tub and p-substrate, its charge density and implant dose is very critical in achieving optimal RESURF condition in the high-voltage NMOS device. Experimental results on the

breakdown voltage of the device as functions of the implant dose in the n-drift layer are presented in Fig. 4. From the figure, it is clear that an implant dose in the n-drift layer of 4×10^{12} cm^{-2} is very close to the optimum value for maximum breakdown voltage. The high-voltage NMOS device is, therefore, resurfed under the influence of the n-drift layer. As a result, the breakdown voltage of the device using the dimension increases from 110 V to 153 V with a deviation of 5 %, as shown in Fig. 4. It is therefore known that a lower or higher implant dose in the n-drift layer would move the device out of the resurf condition, resulting in premature surface breakdown at low voltage.

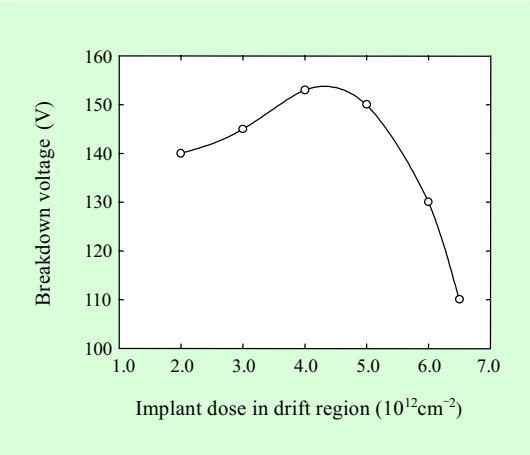


Fig. 27. Breakdown voltage as a function of ion dose in drift region.

Simulations were also carried out on the high-voltage NMOS device with the same device used in this experiment in order to observe the breakdown phenomena. The potential contours, surface electric fields, and current density distributions obtained from the high voltage NMOS at the onset of avalanche breakdown voltage are shown in Figs. 5, 6, and 7, respectively. The breakdown voltage was simulated to be ∼145 V, as shown in Figs. 5, 6, and 7. The breakdown occurs at the edge of the thick field oxide, near the channel and drain edge, where a very high electric field is observed, as shown in Fig. 6. A high current density flow along the surface and substrate of the device is observed, as shown in Fig. 7. This means that avalanche breakdown occurs through the vertical and planar junction simultaneously, corresponding to the optimization of the device and process.

Some discrepancy exists between the experimental and simulation results at high breakdown voltage. This may be attributed to the longer effective drift length caused by the over-etching of the L_{fp} and L_{fm}, leading to longer effective drift length and higher breakdown voltage. Simulations also indicates that the breakdown voltage decreases slightly with increasing L_{fm} and L_{fp}.

Figure 8 presents the experimental results on the specific on-resistance of the resurfed high-voltage NMOS device. The applied voltage across the source and drain is 0.1 V and the total channel resistance between the source and drain is about 582 Ω. As can be seen from the figure, a maximum breakdown voltage of 153 V with a corresponding specific on-resistance of 4.8 mΩ·cm^2 for an active device area of

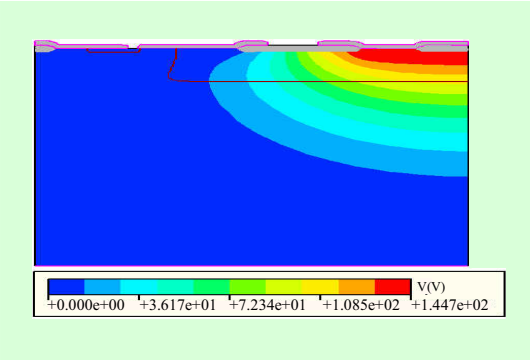


Fig. 28. Equipotential contours of a LDMOS at gate voltage of 5 V.

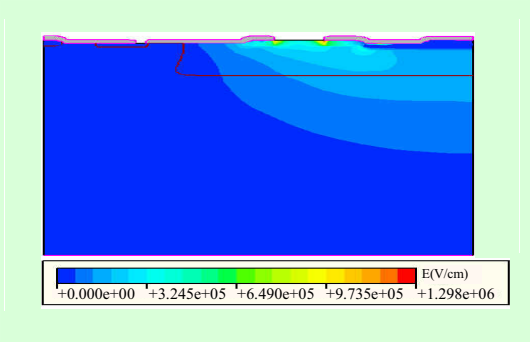


Fig. 29. Electric field distribution of a simulated current 145 V LDMOS transistor with a twin-tub.

8.3×10^{-6} cm^2 was obtained at a drift region length of 5.5 μm and a gate voltage of 5 V. The threshold voltage adjust is a boron implant which sets the p-channel transistor threshold voltage for low voltage and high voltage devices. The threshold voltages of the LDMOS, NMOS, and PMOS are about 0.8 V, 1.0 V, and −1.3 V, respectively. Other electrical parameters of low voltage transistors are shown in Table 1.

A typical test result for 5-V CMOS

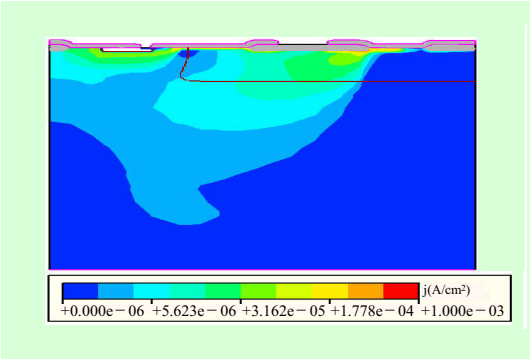
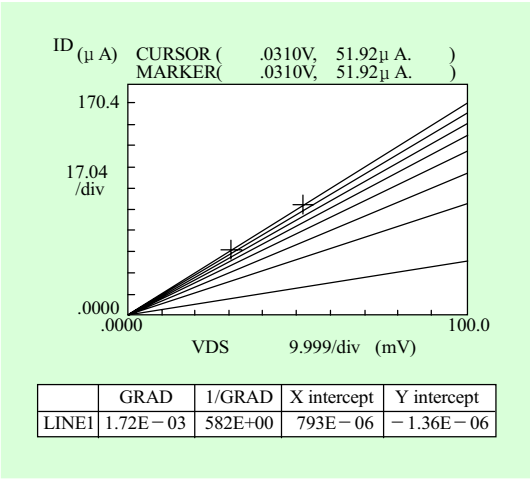


Fig. 30. DESSIS simulated current distribution of LDMOS at breakdown.



	GRAD	1/GRAD	X intercept	Y intercept
LINE1	1.72E−03	582E+00	793E−06	−1.36E−06

Fig. 31. Forward on-resistance characteristics of LDMOS. The applied voltage across the source and drain is 0.1 V and the total channel resistance between the source and drain is about 582 Ω.

switching of an LDMOS carrying 1.9 mA from a 100 V supply is shown in Fig. 9 using an external resistive pull-up road. This power integrated circuit consists of one low voltage CMOS inverter and one open drain LDMOS transistor. Under such gate and supply voltage test conditions, it confirms

Table 3. Electrical parameters of the low voltage CMOS transistors.

Parameter	PMOS	NMOS	Unit
Threshold voltage	−1.3±0.1	1.0±0.1	V
Field threshold	≤ −12	≥ 12	V
Breakdown voltage	≤ −12	≥ 12	V
S/D resistance	50∼60	40∼50	Ω/□
S/D junction depth	0.3∼0.4	0.25∼0.3	μm
Poly resistance	30∼35	25∼30	Ω/□

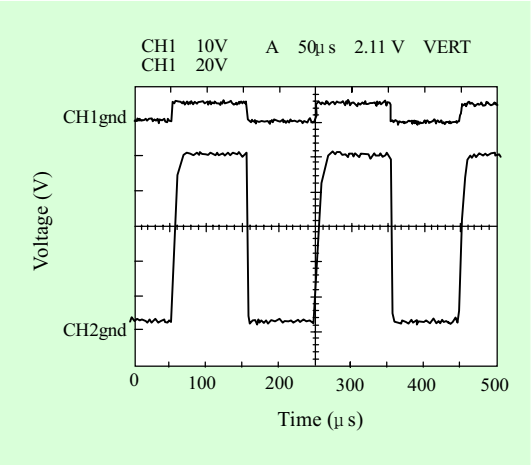


Fig. 32. Switching waveforms related to 5 V CMOS input (upper) and 100 V output signal (lower). Horizontal scale: 50 μs/div; input voltage, 10 V/div; output voltage, 20 V/div.

that the two regions, high and low voltage regions, are completely self-isolated when 5 V and 100 V are supplied to low voltage region and high voltage regions, respectively. The 120 V LDMOS (I_D=1.9 mA with an external resistor and C_L=50 pF) output can also be controlled for the experimental integrated circuits with 5 V logic input data signal.

IV. CONCLUSION

An LDMOS transistor aimed at flat panel display application in the 120 V region is integrated for the first time into a low-voltage 1.2 μm analog CMOS process using p-type bulk silicon. By combining the high performance 1.2 μm low-voltage analog CMOS, self-isolation, and RESURF LDMOS transistors, this process technique provides an excellent method to achieve high performance, mixed power and low-voltage functions on the same chip and especially reducing the mask layer and cost. The power device with a drift length of 5.5 μm and a breakdown voltage greater then 150 V at gate voltage of zero voltage was completely self-isolated to the low voltage CMOS integrated circuits. The specific on-resistance of the resurfed high-voltage NMOS device is about 4.8 mΩ·cm^2 for an active device area of 8.3×10^{-6} cm^2 and a gate voltage of 5 V. Therefore, to provide a cost effective chip integrating logic with high-voltage devices, the CMOS/ LDMOSFET approach using self-isolation and bulk silicon substrates seems to be the most appropriate one from the viewpoint of process complexity and especially cost.

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