Characteristics of Ferroelectric Transistors with $BaMgF_4$ Dielectric

Jong-Son Lyu, Jin-Woo Jeong, Kwang-Ho Kim, Bo-Woo Kim, and Hyung Joun Yoo

CONTENTS

ABSTRACT

The structure and electrical characteristics of metal-ferroelectric-semiconductor FET (MFSFET) for a single transistor memory are presented. The MFSFET was comprised of polysilicon islands as source/ drain electrodes and $BaMgF_4$ film as a gate dielectric. The polysilicon source and drain were built-up prior to the formation of the ferroelectric film to suppress a degradation of the film due to high thermal cycles. From the MFS capacitor, the remnant polarization and coercive field were measured to be about 0.6 μC/cm^2 and 100 kV/cm, respectively. The fabricated MFSFETs also showed good hysteretic $I-V$ curves, while the current levels disperse probably due to film cracking or bad adhesion between the film and the Al electrode.

I. INTRODUCTION

Metal-Ferroelectric-Semiconductor FETs (MFSFETs) have attracted much attention since they can potentially be used as memory and functional neuron devices [1]-[3]. The MFSFET offers a non-destructive read-out memory, while the capacitor approach cannot. Since Moll and Tarui have successfully demonstrated the conductivity modulated transistor using a semiconducting CdS film on a TGS crystal [4], several resear- ches have reported on the ferroelectric field-effect transistors [5]-[8]. Some of ferroelectric materials used in these applications are $Bi_4Ti_3O_{12}$, $LiNbO_3$ and $BaMgF_4$. However, ferroelectric films may loose their original characteristics after high temperature thermal cycles. Such is the case for the ferroelectric films mentioned above when they are processed over 700 °C. As conventional FETs need high thermal budgets for diffusion junctions, the films may not maintain their original characteristics. In this regard, novel device structures and/or fabrication processes are required for the MFSFET.

In this paper, we present a novel MFSFET which conserves its original ferroelectric characteristics, because the source and drain are formed prior to the formation of the gate dielectric. In the experiment, the polysilicon source and drain were formed using chemical-mechanical polishing (CMP) technology [9]. An LPCVD SiO_2/ LPCVD Si_3N_4/thermal SiO_2 stack prevented the channel from mechanical damage during the CMP, and suppressed out-diffusion of channel boron atoms during thermal treatments. The gate dielectric was formed by co-evaporating BaF_2 and MgF_2 in a high vacuum and then rapid-thermal-annealing (RTA) at 600 °C for 20 s. Residual process steps followed a conventional MOS process. The characterization of the fabricated MFSFETs includes polarization $(P-E)$ curves of the ferroelectric capacitor, drain current $(I_{\mathrm{D}}-V_{\mathrm{D}})$ and ferroelectric switching $(I_{\mathrm{D}}-V_{\mathrm{G}})$ curves of the MFSFETs. Although the MFSFETs have some problems such as film cracking and bad adhesion between the metal gate and the film, hysteretic characteristic curves of the MFSFETs showed an application feasibility of the proposed device structure to non-volatile memory devices.

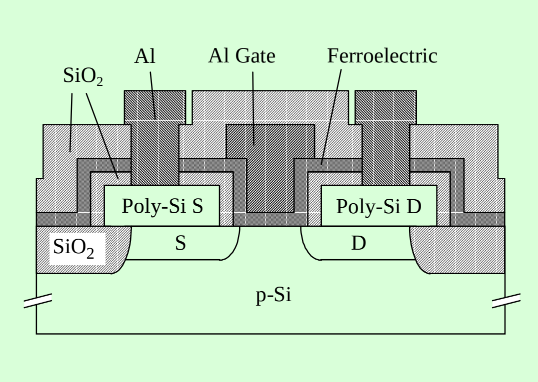

Fig. 1. The proposed structure of the MFSFET.

II. EXPERIMENT

The device structure of the proposed

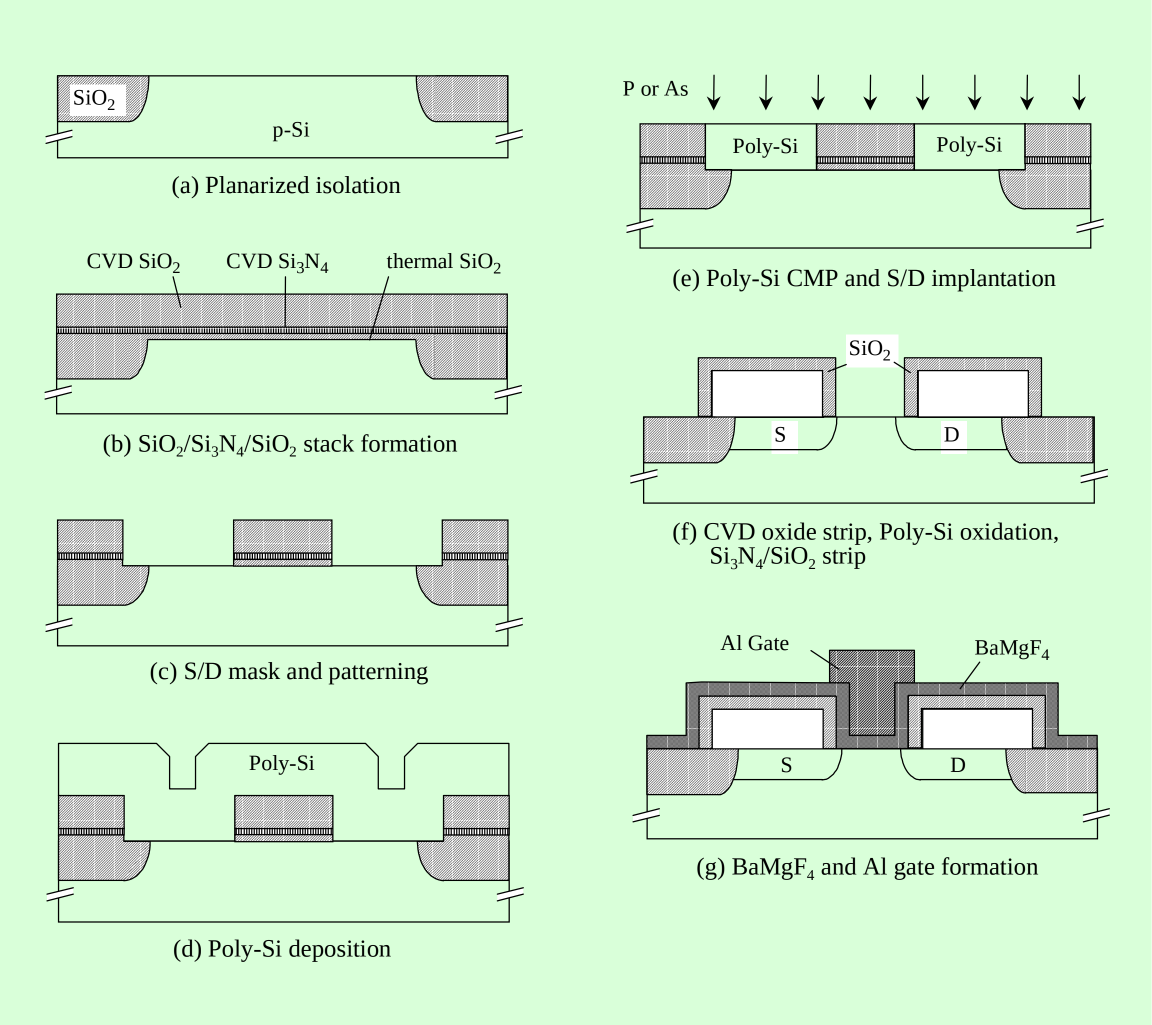

Fig. 2. Fabrication sequence of the MFSFET.

MFSFET with polysilicon source/drain is shown in Fig. 1. The polysilicon source and drain are formed prior to the deposition of the gate dielectric and the channel is recessed under the polysilicon source/drain. This structure was devised to lower the effective junction depth and the source/drain resistance, reducing the short channel effect [10]-[11]. The fabrication steps are shown in Fig. 2. Boron doped p-type silicon wafers with resistivities of 2-5 Ωcm and (100)-orientation were used for this experiment. Active regions were formed using a planarized isolation technique [12]. After the isolation process step, 120 Å thermal SiO_2, 120 Å LPCVD Si_3N_4 and 2000 Å LPCVD SiO_2 were formed sequentially. After the photomask process for the source/drain, the LPCVD SiO_2/LPCVD Si_3N_4/thermal SiO_2 stack in the source/drain areas were dry-etched down to the silicon surface. A 3000 Å-thick polysilicon was deposited by LPCVD and then polished down to the LPCVD SiO_2 surface by using CMP technology [9]. After the implantation of P ions for n^- LDD and As ions for n^+ diffusion junctions into the polysilicon islands and the removal of the LPCVD SiO_2 layer, a 600 Å-thick oxide was thermally grown to activate the dopants and to reduce the gate-to-source/drain overlap capacitance. Channel areas were prevented from the oxidation by the Si_3N_4 layer. Then the LPCVD Si_3N_4/thermal SiO_2 layer on the channel region was stripped off and a 1500 Å-thick $BaMgF_4$ ferroelectric film was deposited in a UHV chamber [8]. The deposition temperature was 300 °C, and the post-deposition RTA was done at 600 °C for 20 sec. Then Al was deposited on the gate dielectric. After the formation of the metal gate, a 4500 Å-thick oxide was deposited by PECVD at 380 °C. After the photomask process for contact holes, the PECVD oxide was dry-etched and the residual $BaMgF_4$ was wet-etched in HCl solution. Figures 3 and 4 show the cross-sectional SEM photograph and the TEM photograph of the fabricated MFSFET, respectively.

III. RESULTS

The remanent polarization P_r and coercive force E_c of the MFS apacitor with a film thickness of about 150 nm were about 0.5 μC/cm^2 and 100 kV/cm, respectively. The dielectric constant of the film and the interface trap density were 10-13 and $8-10 \times 10^{10}$/eVcm^2, respectively. The leakage current at a field of 1 MV/cm was

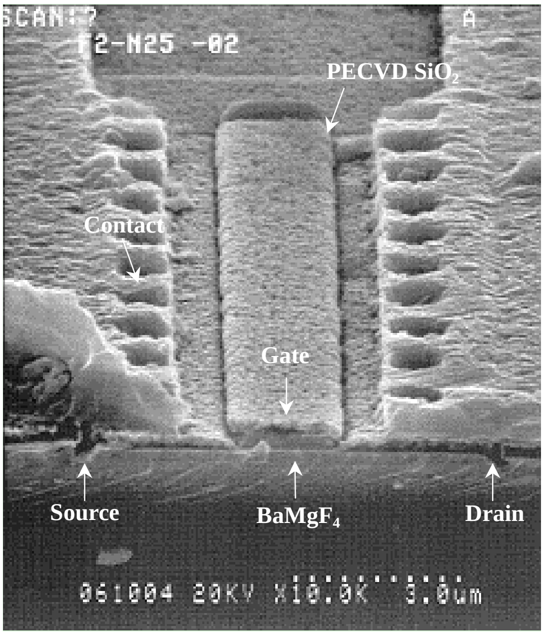

Fig. 3. SEM photograph of the 1 μm channel MFSFET.

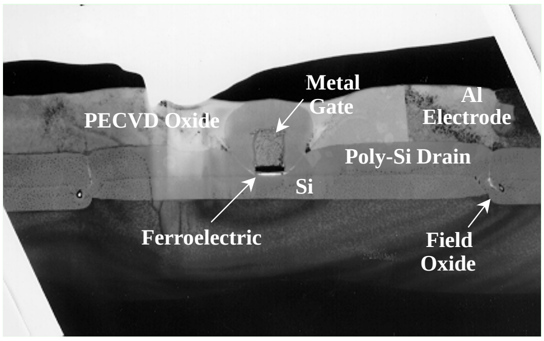

Fig. 4. TEM photograph of the 1 μm channel MFSFET.

less than 5×10^{-7} A/cm^2. The $I_D - V_G$ curves of the MFSFET with $W/L = 5$ μm/1 μm, which followed a PECVD process at 380 °C for the insulating oxide prior to the contact, exhibited a hysteresis due to ferroelectric switching, as shown in Fig. 5. On the other hand, the $I_D - V_G$ characteristics of the MFSFET with $W/L = 5$ μm/1 μm, which followed an LPCVD process at 750 °C for the oxide, exhibited a narrower hysteretic window and lower drain current level as compared with the former device. This result is due to the loss of the original ferroelectric characteristics by the high temperature process [13]. The programming characteristics of the MFSFET was tested by a soft bias stress. The amplitude and duration of the stress pulse were ±5 V and 1 μs, respectively. The current level did not change under the stress up to 10^7 cycles. After 10^9 cycles of the stress, the current level decayed by 20%. This degradation was somewhat larger than that of the ferroelectric capacitor, which may come from a nonuniform dielectric thickness on the channel edge of the MFSFET [13]. The change in I_D of the MFSFET with $W/L = 25$ μm/2 μm under a hard stress was also monitored, as shown in Fig. 6. The amplitude and duration of the stress pulse were ±7 V and 10 ms, respectively. There was nearly no I_D degradation below 10 cycles, however, the drain current increased by about 50 % at 10^2 cycles. The increase may be due to the leakage current from the threshold voltage lowering. Beyond 10^3 cycles of the stress, the current level decayed slowly due to the degradation of the ferroelectric characteristics.

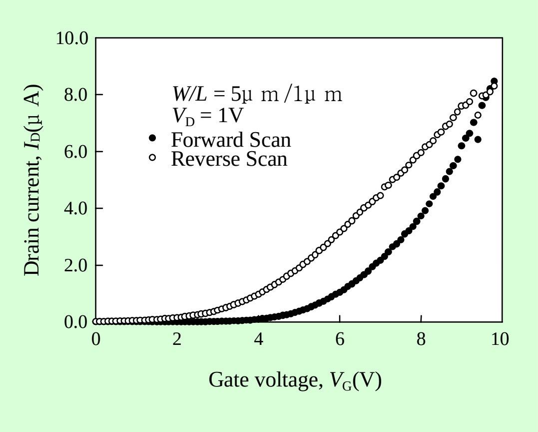

Fig. 5. Hysteretic $I_D - V_G$ characteristics of the MFSFET.

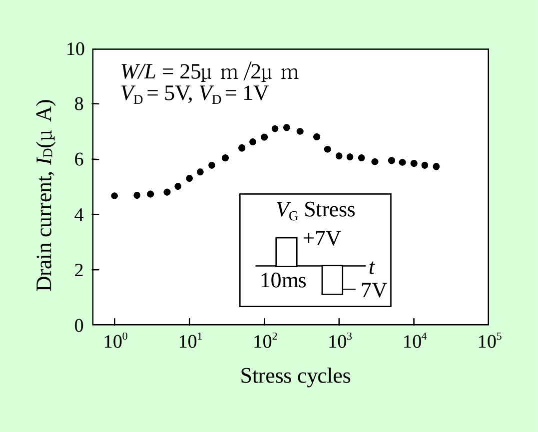

Fig. 6. Drain current shift of the MFSFET by the hard stress condition.

Although the MFSFETs showed good programming characteristics, there remains some problems to be solved. Cracking of the films were observed, as shown in Figs. 8

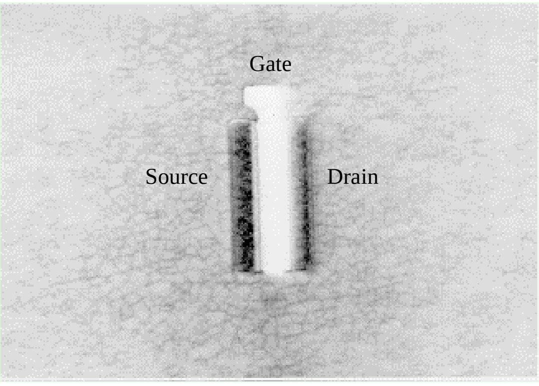

Fig. 7. Top view of the cracking.

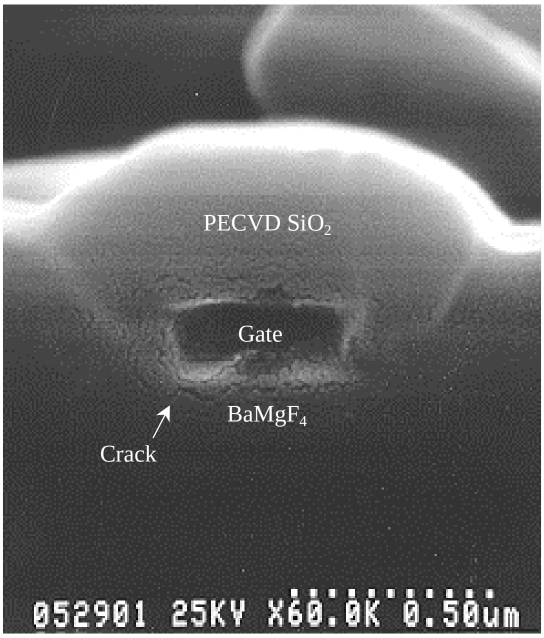

Fig. 8. Cross-sectional view of the cracking.

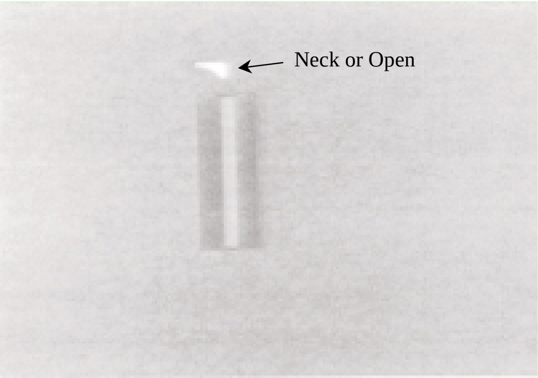

Fig. 9. Necking or opening phenomena of the narrow Al gate due to the bad adhesion between the Al gate and $BaMgF_4$ film.

and 9. The cracks might be formed by the loss of stoichiometry of the film or the temperature gradient during the RTA process. Chemical solutions may penetrate into the channel through the cracks, resulting in a low device performance or reliability problems. The bad adhesion between the film and the Al gate may cause extremely necking or peeling phenomena as shown in Fig. 9. The bad adhesion may also degrade the device performance and reliability, showing poor hysteretic $I_D - V_G$ curves as shown in Fig. 10. For that case, the effective gate voltage biased on the film may be reduced, lowering the drain current drivability and raising the programming voltage. Therefore, further material studies and experimental analyses are required.

The current level of the MFSFET is somewhat low as compared with a usual MOSFET, due to the relatively lower polarization as compared with a high polarization material such as PZT. For the application of the proposed MFSFET to scaled memory or neuron devices, further studies on higher polarization material with low dielectric constant are also required.

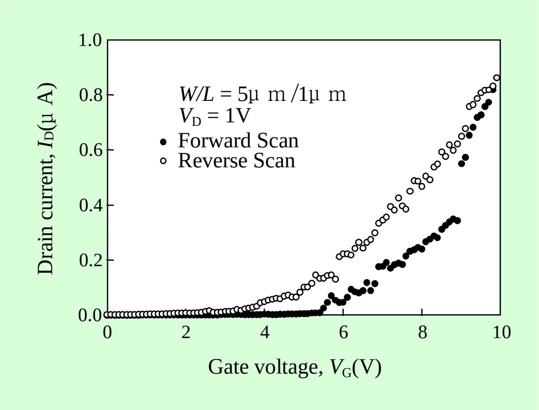

Fig. 10. Poor hysteretic I_D-V_G characteristics of the MFSFET due to the film cracking or bad adhesion.

IV. CONCLUSION

We developed a novel MFSFET with polysilicon islands as source/drain electrodes and $BaMgF_4$ film as a gate dielectric. The polysilicon source/drain islands were formed by CMP technique, and $BaMgF_4$ gate dielectric was deposited in a UHV chamber and treated with the RTA. The fabricated MFSFET showed a good $I - V$ hysteretic curve, confirming the usefulness of the proposed MFSFET for ferroelectric memory transistors. Further studies on the formation of stable films and the preservation of remanent polarization during the thermal cycles are required to use $BaMgF_4$ film in memory applications or other devices.

ACKNOWLEDGMENT

We thank the technical staffs of the semiconductor laboratory of ETRI for their assistance in fabricating the MFSFETs. We are also grateful to Ministry of Science and Technology, Ministry of Information and Communications, and Ministry of Trade and Industry for their financial support for this research.

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Jong-Son Lyu was born in Taegu in 1957. He received the B.S. degree in physics from Kyungbook National University, Taegu, Korea, in 1979. He received M.S. and Ph.D. degree in applied physics from Korea Advanced Institute of Science and Technology, Taejon, Korea, in 1981 and 1993, respectively. He joined Korea Institute of Electronics Technology, Gumi, in 1981, which has been reorganized and unified into ETRI, Taejon, in 1985. He is now a principal member of engineering staff at semiconductor technology division. He has been engaged in the process integration of MOS devices, modeling and characterization of CMOS devices, and silicon-on-insulator (SOI) devices for low power analog/digital applications. His current research interests are ferroelectric thin films and devices for nonvolatile memory, especially for single transistor-type ferroelectric memory cell for IC memory cards.

Jin-Woo Jeong is working toward Ph.D degree in applied physics at Kyungbook National University in

Taegu, Korea. He served as a visiting engineer in ETRI from March to December 1997 for supporting the characterization of ferroelectric devices.

Kwang-Ho Kim was born in Korea in 1958. He received the B.S. degree in eltronics engineering from Hanyang University, Korea in 1983 and M.S. and Ph.D.degrees in applied electronics from Tokyo Institute of Technology, Japan in 1987 and 1990 respectively, where he worked on heterostructure of GaAs and insulators for MIS devices. In 1990, he joined the Department of Semiconductor Engineering, Cheongju University, Korea, where he is now an associate professor. His teaching and research interests include semiconductor materials and devices, fabrication of heterostructure devices of ferroelectric materials and semiconductors, and fabrication of GaAs MIS structure for MISFETs. Dr. Kim is a member of the IEEE and the Japan Society of Applied Physics and the Institute of Electronics Engineers of Korea and the Korean Institute of Electrical and Electronic Material Engineers.

Bo-Woo Kim was born in Busan, Korea, on August 7, 1952. He received the B.S. and M.S. degrees in physics from Busan National University, in 1975 and 1978, respectively. From 1978 to 1981, he served as a research engineer at Samsung Semiconductor Inc., Korea, where he worked on process integration and characterization of MOS devices. Since 1981 he has been with ETRI, where his work has included high density MOS technology, high speed Bipolar technology, and BICMOS technology. He also has been responsible for developing the advanced unit and modular process to improve small geometry devices. From July 1986 to June 1987, he studied an evaluation method of electron and hole traps on dielectric film at Tokyo University, Japan, as a foreign researcher. Recently, He is playing a leading role as director in the Advanced Technology Research Department for ULSI devices and micro/nano systems at ETRI.

Hyung Joun Yoo was born in Seoul, Korea in 1953. He received his B.S. degree in physics from Seoul National University in 1979, and M.S. and Ph.D. degrees, also in physics, from Korea Advanced Institute of Science and Technology in 1990 and 1994, respectively. He had worked at the Agency for Defense Development from 1979 to 1982. He joined ETRI in 1983, where he had served as a director of Advanced Technology Research Department. Since 1998 he is serving as Professor at the Information and Communications University. His research interests include advanced semiconductor devices and process technologies, displays, and microelectromechanical systems.