

CMOS Microcontroller IC와 고밀도 원형모양SOI 마이크로센서의 단일집적

A Monolithic Integration with A High Density Circular-Shape SOI Microsensor and CMOS Microcontroller IC

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Abstract

It is well-known that rectangular bulk-Si sensors prepared by etch or epi etch-stop micromachining technology are already in practical use today, but the conventional bulk-Si sensor shows some drawbacks such as large chip size and limited applications as silicon sensor device is to be miniaturized. We consider a circular-shape SOI(Silicon-On-Insulator) micro-cavity technology to facilitate multiple sensors on very small chip, to make device easier to package than conventional sensor like pressure sensor and to provide very high over-pressure capability. This paper demonstrates the cross-functional results for stress analyses(targeting 5 μ m deflection and 100MPa stress as maximum at various applicable pressure ranges), for finding permissible diaphragm dimension by output sensitivity, and piezoresistive sensor theory from two-type SOI structures where the double SOI structure shows the most feasible deflection and small stress at various ambient pressures. Those results can be compared with the ones of circular-shape bulk-Si based sensor^[17]. The SOI micro-cavity formed the sensors is promising to integrate with calibration, gain stage and controller unit plus high current/high voltage CMOS drivers onto monolithic chip. Key Words: iSOC, Circular SOI Sensor, Micro-cavity technology, IC compatible MCU, Residual stress, Transducer, Piezoresistance, Smart Sensor.

1. Introduction

As communication era comes in reality, SOC(System On Chip) in microelectronics is not only

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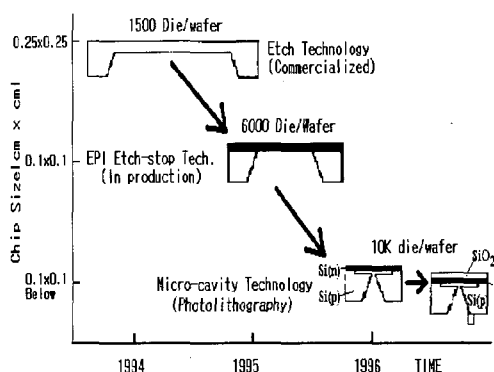
an emerging issue for multiple applications, but iMEMS, the combination of sensor and the SOC, has attracted many researchers for several years. iSOC(integrated SOC) in μ -electronics with CMOS logics and embedded memory where CMOS logic is leading the technology against memory technology is quickly evolving from ASICs(Application Specific Integrated Circuits) as various applications are required, and the combination of the iSOC and non-electronic systems, iMEMS, has attracted university and industrial

researchers for many years. These interfaces, rapidly observed using integrated bulk-Si sensors and microactuators, are growing in more higher value added sophistication. Multimedia, portable communications and automotive/industrial markets can benefit from the integration of macros functions of diverse multi-purpose sensor on a chip due to the power and cost reductions^[1]. Many companies are involved in producing IC compatible sensors based on standard sensor processes such as a timed cavity etch or Direct Wafer Bonding (DWB) oxide-etch stop or electrochemical EPI etch stop, but those processes are difficult to produce thin diaphragm and to handle and process through diffusion/photo steps and they need very aggressive etch. And then IC-compatible cavity-last etch stop processes look promising, but limits initial cost, chip size capability and high over-pressure. Lately bulk-Si micro-cavity technology out of micromachining technologies is promising for small chip size capability^[2,3] since it facilitates multiple sensors on one chip for absolute plus differential pressure, makes device easier to package than conventional sensor like pressure sensor^[4,5] and also makes diaphragm be any shape such as circular to save chip space. In this paper, current trends on micromachining technologies such as the micro-cavity process, application areas of intelligent pressure sensors and IC-compatible smart sensors chips will be briefly mentioned, and some advantages of SOI-based sensors are simulated for fundamental stress analysis along with the residual stresses as a function of the temperature for varying cavity pressure where radius, depth, and membrane of the cavity dimensions are 400, 0.1/10/0.1, and 10 μ m as the target^[12,16], respectively. Those structures for micro-cavity technology of bulk-Si and SOI structures are shown in Fig. 1.

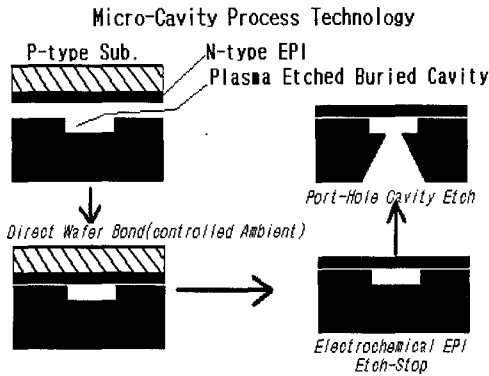
II. Semiconductor Integration and Technology Migration

Trends on the micromachining technology and

main process sequences of recent micro-cavity technology are shown in Fig. 1(a) and (b), respectively. It is essential to determine a target sensing position and IC interface^[6-8] from sensing elements such as piezoresistor, transducer and/or pulse after constructing proper diaphragm. Starting with the piezoresistor's physics, piezoresistance in silicon is changed by conductivity of a material in response to an applied stress. When silicon is stressed, the mobility of the majority carrier(holes) decreases due to increased scattering of carriers. This situation is quite similar to normal silicon implantation or injection into silicon substrate. It is important to understand mechanical properties such as Young's modulus and residual stress for the pure bulk-Si or SOI structure^[9-11] because piezoresistive sensors can be fabricated using two types: one by pure bulk-Si structure and the other by SOI structure which consists of various thin films such as Si, SiO₂, Si₃N₄ and Al₂O₃. Unlike standard sensor process sequences, the micro-cavity technology usually executes the cavity as the last etch after passivation formation for single-side polished 4" epi wafer. It is well-known that device characteristics such as sensitivity and resonance frequency, which strongly depend on thin film mechanical properties^[13-15], are important. In the MEMs world, it would



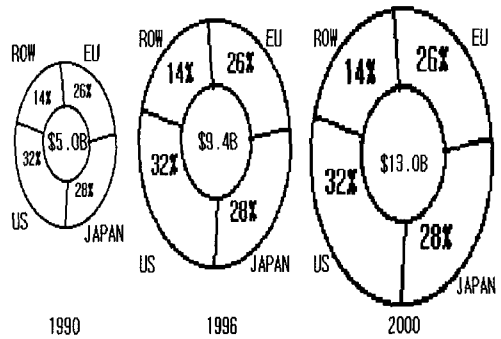
(a)



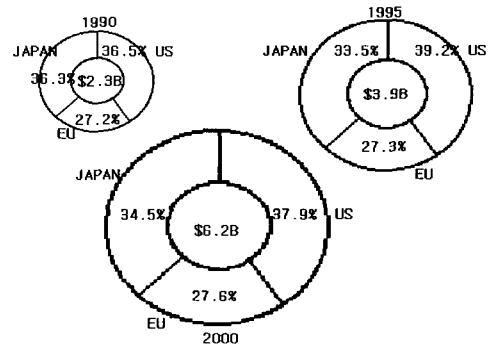
(b)

Fig. 1. (a) Trend on bulk-Si micromachining technology.
 (b) Process for bulk-Si micro-cavity technology.

be ideal to establish a technology platform for future smart sensors with fully integrated sensor system in long term, while to develop high density micro-cavity Si-substrate technology and to integrate a pressure sensor for future chemical sensor or/and an acceleration sensor for intelligence/integration with MCU^[11] onto a single chip on the Si-substrate in short term. Some of these short term goals already indicated that over 60 million units have been shipped and within last 3-year almost 40% is automobile purpose and most of the shipped sensors in production are silicon-based micromachined pressure sensors. The world sensor market is fast growing business as indicated in Fig. 2(a) and Fig. 2(b). There are a variety of silicon sensors under development which are available to measure acceleration, temperature, pressure, chemicals, stress and light. While these sensors may be constructed in silicon, all the manufacturing processes for these sensors are not compatible with each other or with other semiconductor devices or systems. Traditional methods of manufacturing larger electromechanical



(a)

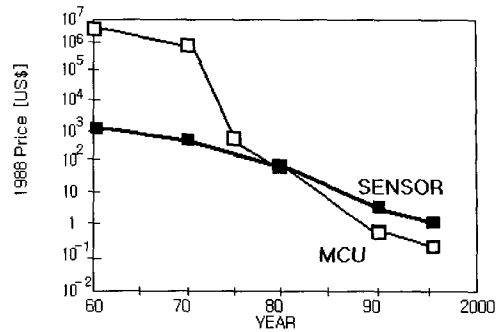


(b)

Fig. 2. (a) Total sensor market by overall region.
 (b) Automotive sensor market by region where EU stands for Europe, ROW for rest of world.

sensors and providing a housing for the signal processing have been proven effective in applications where size, cost, or power consumption have a small impact. There is in fact some desirability for a large and robust mechanism in many applications. But many other applications are emerging that require smaller, lower cost, lower power solutions than traditional methods can address. It is these applications that not only require a silicon based solution, but also require future migration paths that may combine the sensor, signal conditioning and output drivers all on the same silicon wafer. In this

case, incompatible processes must be eliminated if they are not compatible with the mainstream MOS ones used in making microcontrollers (MCU)^[12]. Why target compatibility with microcontrollers? The flexibility and rapid time to market offered by microcontroller solutions with their programmability and wide variety of peripheral options are quite attractive from a design standpoint. In addition, the low cost, high quality and excellent reliability associated with the high volume production of MOS microcontrollers are serious manufacturing consideration. Many popular sensor technologies have several characteristics that make them difficult to use with microcontrollers. These include low-level signals, nonlinearities, temperature sensitivity, and production variation in offset and/or basic sensitivity. A discrete device approach is the first level in the development of low cost, dedicated sensor systems^[3] as shown in Fig. 3(a). These variations and effects can be compensated by a variety of signal conditioning techniques using external components and then interfacing them to the microcontroller using standard MCU digital I/O(input/output) or A/D(analog-digital) microcontroller using standard components external to the MCU. Additional discrete drivers are typically used in cases where the sensor system must directly drive heavy loads. This multiple device approach may be flexible, but it can have cost or size disadvantages against more advanced levels

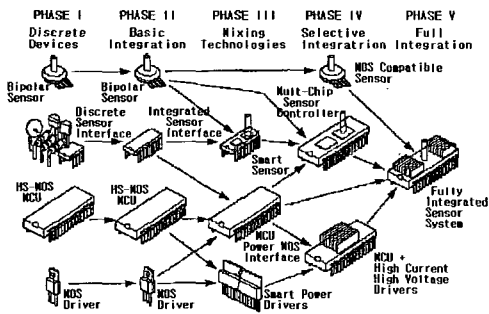


(b)

Fig. 3. (a) Future sensor technology migration.

(b) Cost comparison of sensor and IC-MCU chip.

of systems integration. The ultimate Level V concept contains a sensor of approximately $0.2 \times 0.2 [\mu\text{m}^2]$, which represents about 9% of area. For this type of integration, the total chip is possible but is currently not lower in cost than processing the MCU and sensor separately. To take this concept into production will require one or more significant volume customers to provide specific product definition and minimum target volume which would therefore fuel the production learning curve in a reasonable timeframe. The accelerometer can be used to show how compatibility of the CMOS process with surface micromachining will allow further integration at Level IV by combining the accelerometer interface with the MCU or even allow the possibility of a full Level V combination of an MCU with embedded accelerometer. It must be pointed out that this is a likely integration path and its timing mainly depends on achieving projected costs at intermediate levels. But, by nature, micromachining and other special chemical depositions create more defects than high-volume MCU processes. Therefore, full integration at Level V is more of a business issue than a technology issue. If an extremely small form factor is required, full integration may be required. The actual point at which a Level V total solution can be placed into mass production depends on the



(a)

process complexity and defectivity of the MCU and the sensor processes as estimated as shown in Fig. 3(b). Likewise bulk-Si μ -machining technology, SOI μ -machining technology would attract high sensing and diverse applications since SOI technology in μ -electronics has demonstrated ultra-high speed and ultra-low power performance^[9-11] by many researchers. This research presents some significant results to find permissible diaphragm dimension by piezoresistive sensor theory from the high density circular-shape SOI structure on the Si-substrate for future smart sensor chip. Further, this paper also proposes a way of integrating the current smart sensor macros with MCU as a monolithic chip solution.

III. Design and Technology for IC EMS

This section describes the fundamental transducer operation and its stress analysis and sensitivity parameters for the transducer or sensing element. The smart sensor design with micro-controller integration and the intelligent pressure sensor will be presented.

III-1. Target Design of High Density SOI Sensor

Based on transducer analysis, the sensitivity parameters for the X-ducer's output voltage and their limiting factors are concisely drawn in Table 1 where π_{ijkl} : piezocoefficient, τ_{kl} : stress, N_A : impurity concentration and x_j : junction depth of a transducer or a sensing element. It is found out, based on the optimization technique as mentioned previously, that thin($t=10\mu\text{m}$) and relatively large($r=400\mu\text{m}$), high supply voltage, lower impurity concentration and lowering junction depth for sensing elements such as X-ducer or piezoresistor or pulse provide an excellent sensitivity on the circular shape diaphragm. From Fig. 4, it is observed that larger radius($800\mu\text{m}$) indicates a good sensitivity of $94(\text{mV}/\text{atm})$, however it shows more shear stress, which can not endure high pressure.

Table 1. Sensitivity parameters and limiting factor.

Parameters	Limiting factors
Diaphragm thickness & radius : down/up $V_{OUT} \propto (r/t)^2$	· Wafer shaping tech. · Output Voltage · Linearity
Supply Voltage : up $V_{OUT} \propto (W/L)V_{ss}\pi_{44}\tau_{12}$	· n-well pinch-off · High voltage CMOS tech.
W/L Ratio : up $V_{OUT} \propto (W/L)V_{ss}\pi_{44}\tau_{12}$	· Micro fabrication process tech. · Potential pulling by edge effect
X-ducer impurity Concentration : down $\pi_{44} = \pi_{44}(N_A)$	· n-well pinch-off/CMOS process compatibility · Temperature coefficient
X-ducer Junction Depth : down $V_{OUT} \propto (W/L)V_{ss}\pi_{44}(\frac{1}{x_j})$ $\int_0^{x_j} \tau_{12}(x) dx$	· CMOS S/D process compatibility

More importantly, the output voltage sensitivity of the sensing element(e.g., X-ducer) in mV/atm shows less than $100(\text{mV}/\text{atm}) \approx 1(\text{mV}/\text{kPa})$ under the assumption of fixed thickness of $10\mu\text{m}$, the ratio of 0.5 in Width/Length of the transducer and supply voltage of 5V of which ranges are very close to current pressure sensor products at supply voltage of 5V. The output voltage sensitivity of the X-ducer in mV/atm shows less than $30(\text{mV}/\text{atm}) \approx 0.3(\text{mV}/\text{kPa})$ under the same assumption of the radius whose ranges are very close to current pressure sensor products at supply voltage of 5V. It is observed that smaller thickness ($10\mu\text{m}$) indicates a good sensitivity of $27.6(\text{mV}/\text{atm})$ at fixed

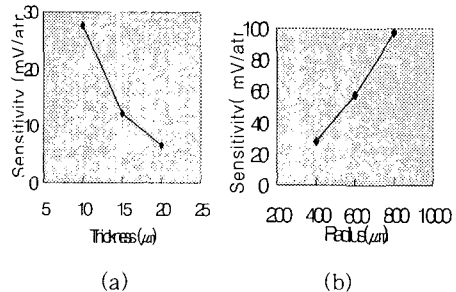


Fig. 4. Output voltage sensitivity for a sensing element in (a)radius- (b)thickness-variation.

radius of $10\mu\text{m}$. Both sensitivities by the radius and the thickness demonstrate a good linearity according to the pressure as shown in Fig. 4, which facilitates the accuracy of the measurement in reality.

For diverse application of the sensors, permissible target dimensions for the maximum stress and deflection must be first determined, i.e., the maximum deflections and stresses for the designed SOI structures satisfy the desired target range (less than $5\mu\text{m}$ max. deflection and 120MPa max. stress for current pressure sensor products) at around 0.1-10 atm pressure range and thereby merges multiple modules on the same silicon material with small dimensions of length and thickness of our designed SOI diaphragm to the final IC-compatible monolithic chip on the same wafer.

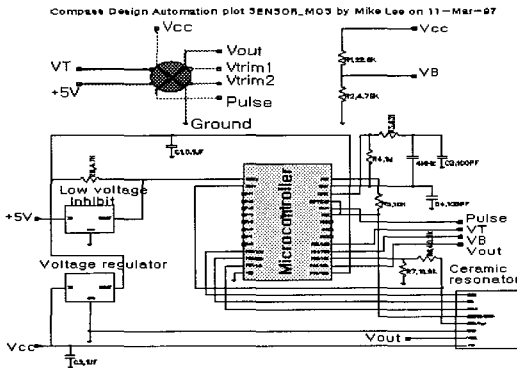


Fig. 5. A proposed MEMS smart sensor with IC compatible micro-controller unit.

It is well-known that maximum stresses and deflections are increasing as the pressure increases, regardless of the top or cavity portion (bottom as shown in Fig. 1(b)) of the designed diaphragm. It is found that the SOI structure indicates safe deflection and small stresses, compared with the bulk-Si structure as expected^[17]. A target position of the sensing element also predicts a product direction for any applicable high sensing micro-cavity sensor in the high technology world. It is also pointed out that the effect of the piezoresistance due to the residual stress must be corrected since the residual stress and the stress by the pressure is directly linked to the piezoresistance effect of the piezoresistor (or transducer) of sensing element.

III-2. IC-Compatibility with Sensors

From the industrial standpoint for the product, there has been an argument that there are significant technology and cost challenges associated with DRAM and logic integration, analog and digital integration, and integration of photons and MEMS with CMOS circuits. The cost of separate chips and yield loss for the MEMS with ICs may never allow some of the merged solutions to be competitive and may also limit the usefulness of iSOCs. Moving a typically higher defectivity sensor process onto another chip becomes increasingly more costly as the die size increases. In all cases, adding a sensor to another silicon device will cost more due to the increased silicon area for a fixed batch size (wafer diameter). The cost penalty of adding a sensor on chip can decrease if the defectivity of the sensor process decreases or the size of the wafers increases. As these improvements occur, the added cost can be traded off against packaging and assembly costs for the two-chip (Sensor Chip + MCU Chip) approach. Table 2 shows the implications of different process defectivities on the net cost of a combined solution. CMOS plus sensor, in the goal of the research. From Table 2, to demonstrate the costs of combining a sensor with an MCU, consider a small size $0.13 \times 0.13\text{cm}^2$ MCU processed at 0.8 defects/ cm^2 and a $100 \times 100\text{mil}$ sensor processed at 4.0 defects/ cm^2 .

Table 2. Theoretical relative die costs.

Assumes	Defects per square centimeter			
	Best in Class	Typical MOS Industry	Sensor Development Assumptions	
6" wafer				
Die-Size (cm × cm)	0.2	0.8	2.0	4.0
0.13 × 0.13	0.25	0.25	0.26	0.27
0.25 × 0.25	1.01	1.05	1.14	1.29
0.33 × 0.33	1.70	1.81	2.05	2.50
0.75 × 0.75	10.85	15.15	27.69	65.11
0.80 × 0.80	11.31	16.17	30.89	75.28
		MCU	Sensor	MEMS

the example MCU will have a relative cost of 1.05 versus a $0.13 \times 0.13 \text{cm}^2$ device processed with zero defects; and the sensor will have a relative cost of about 1.29, which gives a combined two chip relative cost of 2.34. If they were combined on a single die using a sensor process that creates 4.0 defects/ cm^2 , the resulting die would be about $0.25 \times 0.25 \text{cm}^2$ and have a relative cost of 2.50 since 2.34×1.07 results in 2.50. This cost increase of only 1.07 times the combined die cost may be less significant than the added assembly and test costs of two separate devices. The cost penalty of adding a sensor on chip can

decrease if the defectivity of chip sensor process decreases or the size of the wafers increases. As these improvements occur, the added cost can be traded off against packaging and assembly costs for the two-chip approach. So our designed small size sensor using micro-cavity technology with IC compatible MCU as shown in Fig. 5.

III-3. Trends and Expectation for Smart Sensor

The monolithic one-chip will be widely applied to automotive engine control, intelligent sensor for gas meter control and semiconductor process control, and medical sensor in the future as listed in Fig. 6(a) and Fig. 6(b) where hatched boxes of MAP, medical and dry air are currently active and potential for increased participation: open boxes of tire, water level, and HVAC are not currently participating though technical and market capabilities exist: filled boxes are not participating since major technology gap exists. Note that technology remedy for MEMS chip development on silicon CMOS as a function of supply voltage should be considered as Table 4. Also MOS design and technology innovation for high voltage

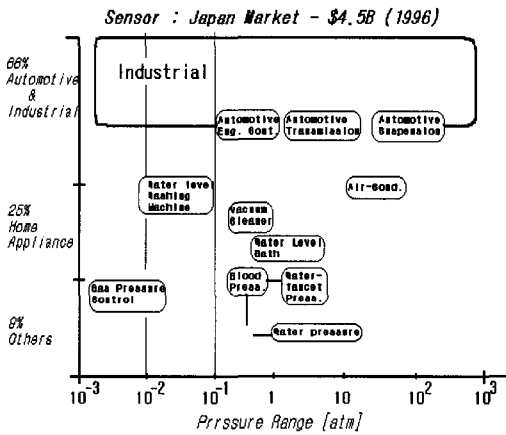


Fig. 6. (a) Application areas and technology gaps for future sensor based on the pressure ranges.

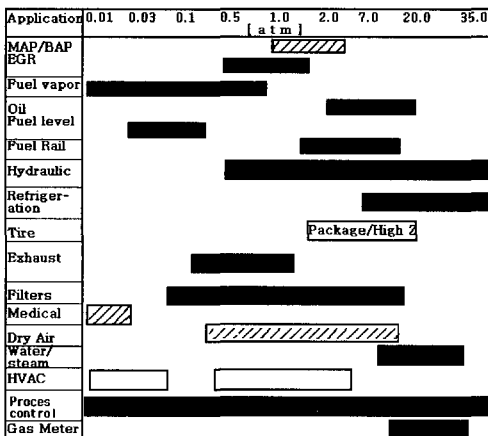


Fig. 6. (b) Technology gaps for future intelligent pressure sensor based on the pressure range.

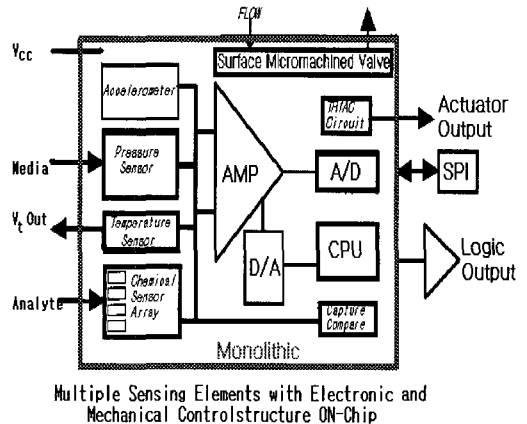


Fig. 7. Multiple sensing MEMS control structure on-chip solution.

circuit are technical challenges as multi-chipmodules with separate die for sensor and the MCU interface as indicated in Table 5. Our proposal is to develop the MEMS chip on 5V CMOS technology since there is no high voltage technology required for high volume, cost sensitive applications such as sensing in automotive control systems. So IC integrated microcontroller compatible sensor are to use of the area where intelligent sensing is really needed in the future. Future sensor technology migration for fully integrated sensor is the final objective of this research as milestone in Fig. 3. Practical application using the smart sensor as listed in Table 3 is intelligent safety gas meter or IHVAC as industrial use where the MCU^[12] and other sensors can be implemented as two-chip or three-chip solution and/or multiple sensing MEMS control system as shown in Fig. 7. So it is important to combine the sensor into current available 5V or 3.3V CMOS technology for a monolithic chip like Fig. 8 with MEMS design and high voltage MOS technology as shown in Table 4 and Table 5 where pressure ranges are from 0.01[atm] to high 10[atm]. It is, therefore, necessary

to overcome the combination of high voltage CMOS design for wide range of pressure and to improve the sensitivity of the designed sensor macros. Economical reality for the cost of total micro-cavity substrate is estimated about \$163.24/Wafer for a 6" bonded wafer, including back port opening of the cavity process.

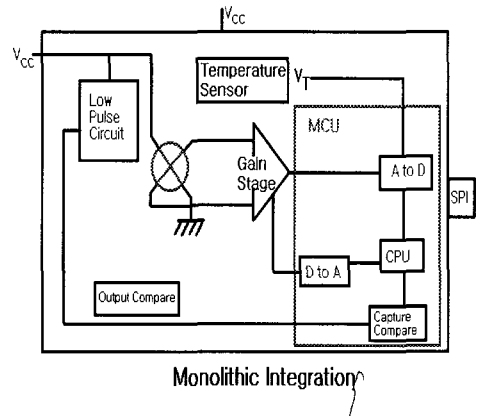


Fig. 8. Monolithic integrated MEMS for automotive and medical applications.

IV. Conclusion

This paper presents the cross-functional results for stress analyses (targeting 5µm deflection and 100 MPa stress as maximum at various applicable pressure ranges) of IC-compatible intelligent circular-shape SOI sensor for finding permissible diaphragm dimension by output sensitivity and the temperature drift from the SOI structures. The double SOI structure shows the most feasible deflection and small stress at various ambient pressure. The SOI micro-cavity formed the sensors is promising to integrate with calibration, gain stage and controller unit plus high current/high voltage CMOS drivers onto monolithic chip on the same silicon wafer, proposing a way of developing it on unified 5V CMOS technology for future smart sensor.

Table 3. Future market for smart sensor.

Market Segment	Required Media	Current Solution	Competition	Possible Applications
Automotive	● Gas ● Oil ● Water ● Air	● Mechanical ● Semicon	High	● Air-bag ● Fuel control ● Engine control ● Ride control
Consumer	● Water ● Air	● Mechanical ● Semicon	Moderate	● Washer & Dryer ● Refrigerator/Air-condition ● Vacuum cleaner
Industrial	● Gas ● Oil ● Water ● Air	● Mechanical ● Semicon	High	● HVAC ● Smart Bldg. ● Earth-Quake detect ● Industrial Meters
Computer	● Air		Low	● Disc Drive protection ● End of Tape Readers
Tele-Comm.	● Water ● Air	● Semicon	Low	● Below surface tubing ● Security
Bio-Medical	● Air ● Fluids	● Semicon	Moderate	● B/P & Heart Monitor ● Saline Pumps ● Respiratory systems

Table 4. Power supply voltage vs. MEMS chip development on silicon CMOS technology.

Line Voltage [V]	Internal Operation Voltage[V]		Technology		Remarks
	X-ducer & drive	MPU	Voltage regulator	X-ducer driver	
24	24	5	24V CMOS (24 to 5)	24V CMOS	<ul style="list-style-type: none"> Same specification with commercial product - Better acceptability by the customers. High Voltage(HV.) CMOS technology required.
24	5	5	24V CMOS (24V to 5)	5V CMOS	<ul style="list-style-type: none"> Same specification with current products: Higher acceptability by the customers. Relying primarily upon improvement of X-ducer sensitivity and/or CMOS amplifier gain. Still HV. CMOS technology is required for the internal regulator.
5	12	5	(External)	12V CMOS	<ul style="list-style-type: none"> 5V power line required. Charge pump with four external capacitors required. 12V CMOS technology required.
5	5	5	(External)	5V CMOS	<ul style="list-style-type: none"> improvement of X-ducer sensitivity and/or CMOS amplifier gain required. No HV. CMOS technology required. External voltage regulator required for HVAC application. Should Target higher pressure range applications.

Table 5. Applications and technology challenges.

Pressure Range	Moderate 0.1 ~ 0.01 atm	High > 0.1 atm
Application	HVAC Water Level Sensing (Washer) Gas Pressure Control	Blood Pressure Vacuum Cleaner Automotive
Technical Challenge	Choice 1: V = 24V Design and MOS Technology Innovation for High Voltage Circuit Choice 1: V ≤ 12V Sensor element innovation for improved sensitivity Design and MOS Technology Innovation for High Performance Amplifier	V ≤ 5V

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References

- [1] K. Wise, "Microelectromechanical Systems: Interfacing Electronics to a Non-Electronic World," *IEEE IEDM'96*, p.10, Dec., 1996.
- [2] H.H. Lee, *et al.*, "Fabrication of Surface Micromachined Polysilicon Actuators Using Dry Release Process of HF Gas-Phase Etching," *IEEE IEDM'96*, s30.1, Dec., 1996.
- [3] R. Frank and Joe Staller, *Proc. of 3rd Int. Forum on ASIC and Xducer Tech.*, Alberta, Canada, May, 1990.
- [4] R. Okojie, A. Ned and A. Kurtz, " α (6H)-Si Pressure Sensor at 350°C", *IEEE IEDM'96*, s20.2, Dec., 1996.
- [5] F. Paoletti, M.-A. Gretillat and N.F. de Rooij, *Proc. IEEE MEMS Workshop*, CA, p.162, 1996.
- [6] M. Shinogi, *et al.*, *IEEE IEDM'96*, s30.3, Dec., 1996.
- [7] H. Baltes, *et al.*, "IC MEMs Microtransducers", *IEEE IEDM'96*, s20.1, Dec., 1996.
- [8] C. Lee, *et al.*, *IEEE IEDM'96*, s20.7, Dec., 1996.
- [9] Y. Yamaguchi *et al.*, "A High-speed 0.6- μ m 16K CMOS gate array on a thin SIMOX film," *IEEE Trans. Electron Devices*, vol.40, p. 179, Jan., 1993
- [10] A. Auberton-Herve, "SOI: Materials and Systems," *IEEE IEDM'96*, p. 1, Dec., 1996.
- [11] T. Fuse, *et al.*, "0.5V SOI CMOS pass-gate logic", *IEEE ISSCC*, p. 88, 1996.
- [12] M. Lee, "Mastery over Low Power Silicon ICs : Process technologies to System architectures", *The 4th Korean Conf. on Semiconductor*, Feb., Kyungju, 1997.
- [13] N.P. Bansal and R.H. Doremus, "Handbook of glass properties", Academic Press, 1986.
- [14] J. Fraden, "Handbook of MODERN SENSORS", AIP press, N.Y., 2nd Ed., 1997.
- [15] J.J. Wortman and R.A. Evans, "Young's Modulus, Shear Modulus, and Poisson's Ratio in Silicon and Germanium", *Journal of Applied Physics*,

Vol. 36, No. 1, pp. 153-156, 1963.

[16] I-DEAS FEM™ User's Guide, MODEL SOLUTION™ Verification Reference Guide, SDRC, 1995

[17] M. Lee and Y.H. Moon, "A High Density IC

Compatible Multi-purposae Circular-Shape Sensor on Micro-Cavity SOI Technology", 1997 대한전기학회 MEMS 연구회 학술발표회 논문집, pp. 49-58, 고려대학교, 4월, 1997

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