# PN Chip Clock Generator for CDMA Code Synchronization

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Abstract

In this paper, we propose a new PN chip clock generator which employs two synchronous counters to achieve precise phase control of chip clock. In a CDMA code acquisition and tracking system, the PN chip clock is required to operate highly reliable without any glitch even under harsh environment conditions such as temperature and voltage fluctu-ations. The digital implementation of the proposed PN chip clock generator imparts it with much desired reliability. Since the proposed chip clock generator can be easily controlled into one of the states: free running, phase advance, and delay state, it can be applied to data processing as well as code synchronization. We have done FPGA implementation of the proposed logic and have verified its satisfactory operation up to 50 MHz.

## I. INTRODUCTION

Code synchronization is a time alignment process between the received PN code and locally generated PN code in spread spectrum receiver. It is divided into a coarse time alignment process (code acquisition) and a fine time alignment(code tracking). Active correlator scheme is widely applied in code acquisition because it has low hardware complexity compared with other code acquisition schemes such as matched filter and parallel correlators. While on the other hand, the phase control of the PN chip clock becomes very complex. After code acquisition the phase of PN chip clock has to be maintained to track the phase of the received PN code [1][3]. Also a reliable chip clock should be generated to provide the system timing to the data processing logic. PN chip clock generator can be implemented by NCO (Numerically Controlled Oscill-ator), but it is difficult to control the exact phase of chip clock with subchips since the chip rate in spread spectrum systems is the order of several MHz. The chip clock generator implemented by using random logic has glitches due to path delay[2]. The path delay in FPGA and ASIC circuit is a random variable due to external temperature variations. The generated chip clock may cause unreliable logic operation. To overcome these problem, a new chip clock generator is proposed in this paper by using dual synchronous counters. Its mechanism is based on state transition control by loading specific value to synchronous counter each other. In section II, the basic requi-rements of the chip clock generator are specified. In section III and IV, functional and operational design are discussed. Finally we

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conclude and summarize our results in section V.

## Ⅱ. BASIC REQUIREMENTS

Code acquisition scheme with active correlator and DLL(Delay Locked Loop) code tracking is considered here as code synchronization model. In code acquisition mode, the energy value is calculated at on chip time and compared with the threshold vaule. If it crosses the threshold value, it is decided that the code sync. is detected and the code tracking follows. Otherwise, 1/2 chip slew is performed to search the next code phase PN code. The phase of chip clock is updated by 1/2 chips in code acquisition mode and 1/8 chips in code tracking mode. And its basic configu-ration is shown as Fig. 1.

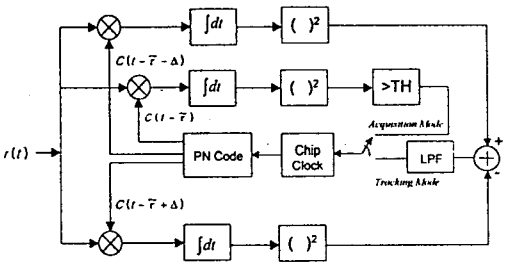


Fig. 1 PN Code Synchronization Model

The design requirements for PN chip clock are

1) The clock phase should be capable of delaying or advancing by 1/2 chip time in code acquisition operation and the rising edge of phase controlled chip clock should coincide with that of chip clock in free running operation as shown in Fig. 2
2) In the code tracking mode, the clock phase should be capable of either delaying or advancing by 1/8 chip time, or remain unchanged and operate stably shown as Fig. 3. Its phases for delay and advance are determined by timing error from DLL phase detector.

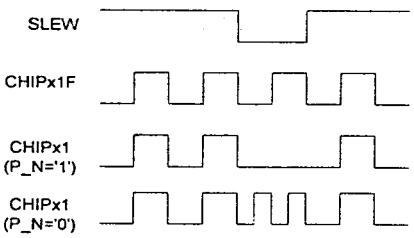


Fig. 2 PN chip timing in slew operation

## Ⅲ. FUNCTIONAL DESIGN

The PN chip clock generator to meet the timing requirements mentioned in section II can be implemented by using dual synchronous counters. Counter-I generates a phase controlled chip clock for code synchronization and is reset by periodic pulse from counter-II. Counter-II is a free running counter which generates a periodic pulse to reset counter-I. The state transition of counter-I is changed by loading value and periodic reset which is generated by external control and pulses from counter-II. The block diagram of this implementation is shown in Fig. 4.

TTE is a tracking enable signal which controls code acquisition and code tracking mode. P_N controls the chip clock to be slewed positively(phase delay) or negatively(phase advance). SLEW indicates that energy value has not crossed the threshold and slew again to search next code phase. Timing error TE[1:0] is output signal of LPF in DLL code tracking mode, which is a quantized value of lowpass filtered timing error. Load value LD[2:0] of counter-I is determined by external control as shown in table 1.

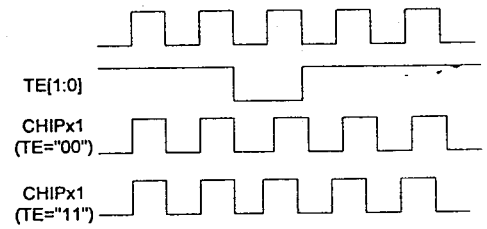


Fig. 3 PN chip timing in code tracking operation

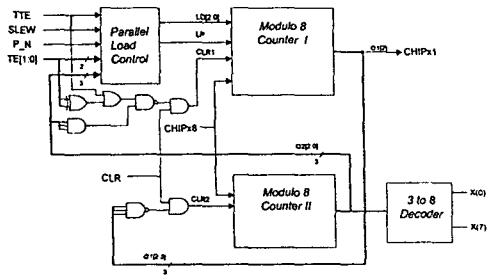


Fig. 4 Block diagram of PN chip clock

Table 1. Load value and Load point of counter I

| TTE | P_N | SLEW/ | TE[1:0] | L[2:0] | Load Point | Operation |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | x | 100<br>010 | X(1)<br>X(3) | 1/2 Chip Delay |
| 1 | 0 | 1 | x | 001 | - | Free Running |
| 1 | 1 | 0 | x | 001 | X(3)<br>X(6) | 1/2 Chip Advance |
| 1 | 1 | 1 | x | 001 | - | Free Running |
| 0 | x | x | 00 | 001 | X(1) | 1/8 Chip Delay |
| 0 | x | x | 01 | 001 | - | Free Running |
| 0 | x | x | 10 | 001 | - | Free Running |
| 0 | x | x | 11 | 011 | X(1) | 1/8 chip Advance |

To meet the truth table, the load value LD[2:0] and load pulse LP, reset pulse CLR1 of counter-I can be expressed by switching function and it is given by

$$LD[2] = TTE \cdot SLEW \cdot \overline{P-N} \cdot Q2[2]$$

$$LD[2] = TTE \cdot SLEW \cdot \overline{A2[2]} + \overline{TTE+(TE[1])\oplus TE[0])}$$

$$LD[0] = \overline{TTE \cdot SLEW} + P-N$$

$$LP = TTE \cdot SLEW \cdot \overline{P-N} \cdot \times[1] \cdot \times[3] + TTE \cdot SLEW \cdot P-N \cdot \times[3] \cdot \times[6] + \overline{\{(TE+[1]\oplus TE[0])) \cdot Q2[1]}$$

$$CLR1 = CLR \; \overline{Q2[2] \cdot Q2[1] \cdot Q2[0] \cdot \{TTE+(TE[1]\oplus TE[0])\}}$$

Also reset signal of conter CLR2 is given by

$$CLR2 = CLR \cdot \overline{Q1[2] \cdot Q1[1] \cdot Q1[0]}$$

## Ⅳ. OPERATIONAL DESCRIPTION

The proposed PN chip clock generation has five operation modes: free running, positive slew by half chip, negative slew by half chip, positive slew by 1/8 chip, and negative slew by 1/8 chip. Referring to the block diagram shown in Fig. 4, counter-I generates the chip clock and counter-II is responsible for generating three bit values LD[2:0]. Whenever we need to change the normal state transition of modulo-8 counter-I, these three bit values LD[2:0] are parallelly loaded into counter-I. Table 2 shows the state transition diagram of counter-I and counter-II in all five modes of operation. In Table 2, S0 to S7 refers to transition states of counter-I and X0 to X7 refers to transition states of counter-II. The state transition of counter-I in the free running mode is hereinafter referred to as its normal state transition. We can note from the Table 2 that the state transition of counter-I differs in each mode to achieve the desired objective.

Table 2. State transition of counter I according to operation mode

| Operation Mode | State Value of Counter I |
|---|---|
| Free Running | S0, S1, S2, S3, S4, S5, S6, S7, S0, S1, S2, S3, ...., |
| Positive Slew by 1/2 chip time | S0, S1, S2, S3, S1, S2, S3, S1, S0,S1, S2, S3, ... |
| Negative Slew by 1/2 chip time | S0, S1, S4, S5, S2, S3, S4, S5, S0, S1, S2, S3, ..., |
| Positive Slew by 1/8 chip time | S0, S1, S1, S2, S3, S4, S5, S6, S7, S0, S1, S2, ..., |
| Negative Slew by 1/8 chip time | S0, S1, S3, S4, S5, S6, S7, S0, S1, S2, S3, S4..., |

The state transition diagram for counter-I is also shown in Figure 5. In this Figure, we have shown

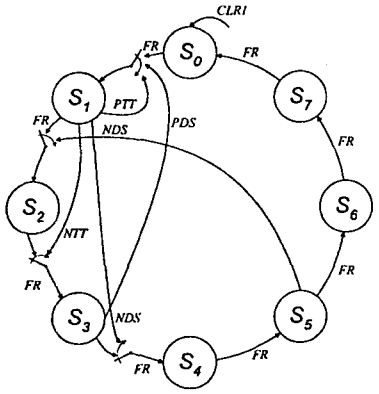


Fig. 5 State transition of counter-I

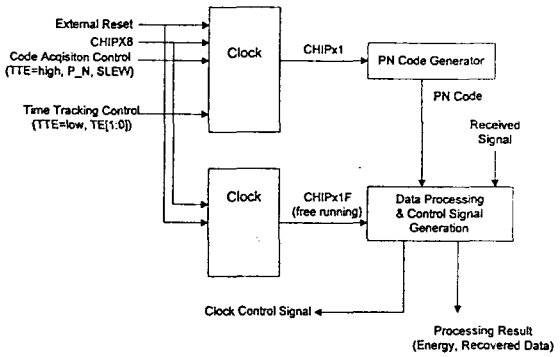


Fig. 6 PN code generation and its application

five different control signals corresponding to five modes of operation of PN-chip clock generator.

* FR is active in the free running mode.
* PDS is active in the 1/2 chip positive slew mode.
* NDS is active in the 1/2 chip negative slew mode.
* PTT is active in the 1/8 chip positive slew mode.
* NTT is active in the 1/8 chip negative slew mode.

Corresponding to the operation mode, one of the five signals is asserted which in turn controls the state transition of counter-I. For example, consider that the PN-chip clock generator is required to be operated in the 1/2 chip negative slew mode. So NDS will be activated and counter-I will follow links in Figure 5 corresponding to NDS. This means that the state transition of counter-I will be as follows :

$S_0$, $S_1$, $S_4$, $S_5$, $S_2$, $S_3$, $S_4$, $S_5$, $S_0$, $S_1$, $S_2$ ....

Similarly, all state transitions of counter-I shown in Table 2 can be derived. We can note from Table 2 that when counter-II reaches the $X_1$ state, counter-I should be loaded with 100 so that next state of counter-I is $S_4$ instead of its normal state $S_2$. Following the same reasoning, when counter-II reaches $X_3$ state, counter-I should be loaded with 010 to take counter-I to $S_2$ in the next state. Similarly, load values in every mode will be determined, as summarized in Table 1.

The chip clock generator can be controlled to operate in free running or phase controlled chip clock mode. In phase controlled mode, the chip clock can be used for PN code generation. In free running mode it is used for data processing in noncoherent code acquisition, code tracking and external control signal of chip clock module. As the chip clock rate is increased, the master chip clock can be replaced by 4 times chip clock and it is easy to update the phase control. Because the chip clock logic is all digitally design and synchronous logic, it is reliable and operates glitch free. Through FPGA implementation its function has been verified to operate satisfactorily up to 50 MHz.

## V. CONCLUSIONS

The phase controlled chip clock generation for code acquisition with active correlator and DLL code tracking is presented in this paper. The phase control of local PN chip clock can be advanced or delayed by 1/2 chips or 1/8 chips. The most important features of the chip clock generator is that it is simple to implement into digital logic and operates reliable and glitch free. The PN chip clock generation is implemented by using dual synchronous counters. The state transitions of two counters are mutually controlled to generate

required chip timing and its logic has been verified through FPGA implementation. Because of the easy control in in free running, phase advance and phase delay mode, the chip clock generator could be applied for both data processing and code synchronization.

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