Design and Performance Analysis of an Asynchronous Shared-Bus Type Switch with Priority and Fairness Schemes

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ABSTRACT

In this paper, we propose an architecture of the asynchronous shared-bus type switch with priority and fairness schemes. The switch architecture is an input and output queueing system, and the priority scheme is implemented in both input and output queues. We analyze packet delay of both input and output queues. In the analysis, we consider the stations with asymmetric arrival rates. Although we make some approximations in the analysis, the numerical results show good agreements with the simulation results.

I. Introduction

It is anticipated that future communication services will be provided largely via packet switching networks [1]. For this reason, many switching architectures for packet networks have been developed[2, 3]. One of the simplest structures for high-speed packet switching is the shared-bus type switch architecture.

In this paper, we propose an asynchronous shared-bus type switch architecture with priority and fairness schemes. The switch architecture is an input-and-output queueing system.

In this paper, we also analyze the delay performance of the switch architecture we propose. Although there are two or more priority levels in the switch, the delay in each priority level can be investigated through one queueing model. We consider the stations with asymmetric arrival rates. In the analysis of input queueing delay, the concept of conditional cycle time[4]

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is used.

II. Switch Structure and Operation

An $N \times N$ asynchronous shared-bus type switch is constructed with N stations, a start pulse generator (SPG) and a high-speed bus as shown in Fig. 1. In a station, there are a bus controller(BC), an address filter(AF), a transmitter(TX), input queues and output queues. Entering packets to a switch input are stored in one of the input queues according to their priority levels. The data rate of an output link is m_1 and the data rate of the bus is m_2 (normally $m_2 > m_1$). All the bus controllers are connected wired-ANDed to the bus. Thus the bus has the AND value of all the bits transmitted from the bus controllers. When a bus controller has no packets to transmit, it transmits contiguous '1's on the bus. The bus controllers are also connected wired ANDed to the active line.

A bus controller informs the SPG through the active line of whether the bus controller is transmitting data on the bus or not. The low value of the active line means that the bus is occupied by a station. The
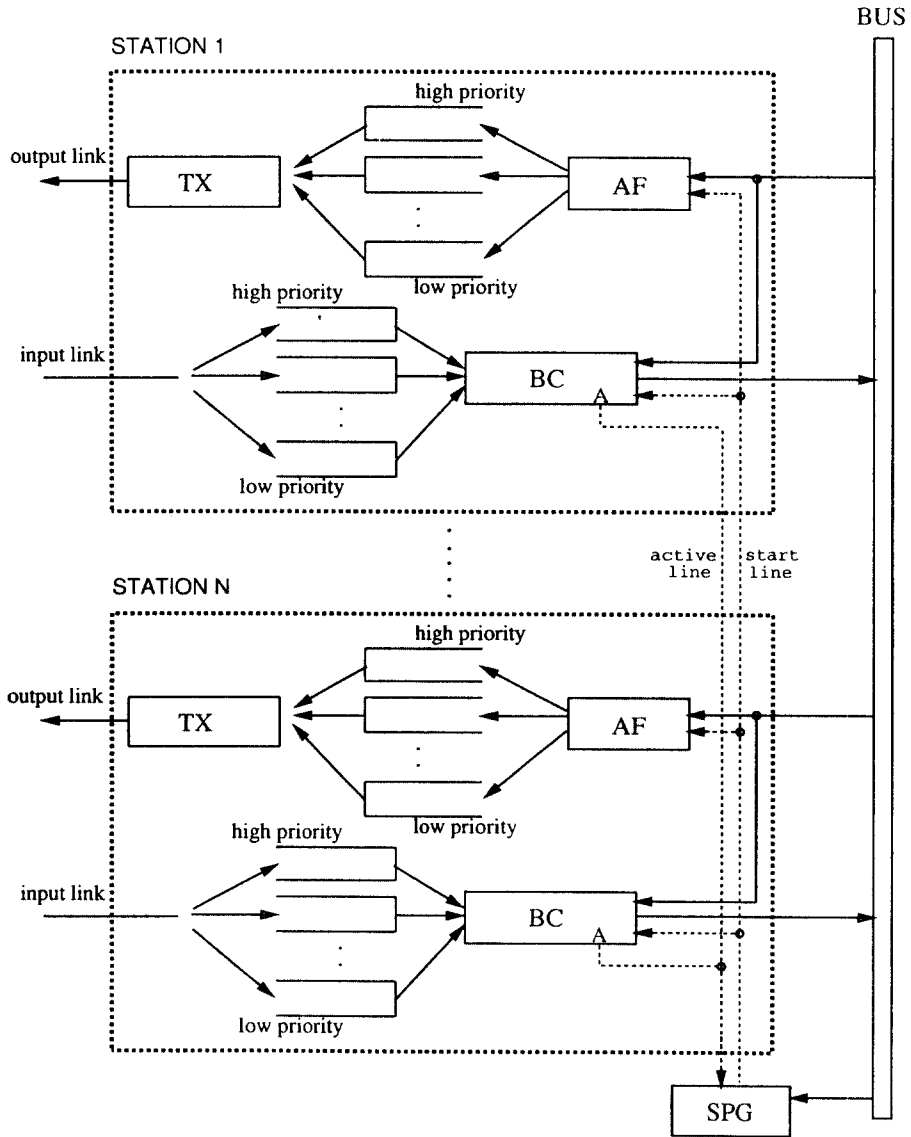
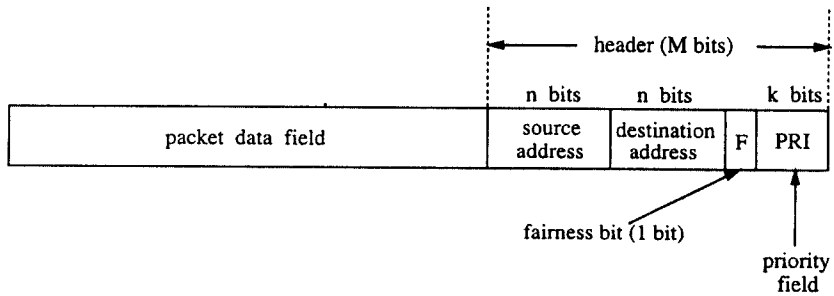Fig. 1 N×N shared-bus type switch structure.

Fig. 2 Packet format.

high value of the line means that the bus is idle. There is another control line in the switch, that is, the start line. The SPG sends start pulses through the start line to the bus controllers, which signals that the bus controllers may start packet transmission.

The packet format is shown in Fig. 2. The destination address field does not have the pattern '111 ... 1'. Thus we have $N \leq 2^n - 1$. Since the priority field is k bits, there can be $K = 2^k$ priority levels in the switch. Here, the PRI value of '000 ... 0' means the highest priority level. The bus controller has K internal variables, F_i $(0 \leq i \leq K-1)$. F_i is used for fair access to the bus in the i-th priority level.

A. *Bus Controller(BC)*: a bus controller does its operation according to the following procedure. Initially, the active line output(A) is set to high.

i) The bus controller sends contiguous '1's on the bus and waits until a start pulse comes through the start line. When a start pulse comes, h is set to zero and go to step (ii).

ii) The bus controller reads the header of the head-of-line(HOL) packet in the highest priority input queue which is not empty and fill the F field of the header with the internal variable F_i for the queue's priority level. If there are no packets in the input queues, the bus controller lets $h = 1$. '$h = 1$' means that the bus controller does not send a packet on the bus at this time.

iii) If $h = 0$, the bus controller transmits the header on the bus. If not, the bus controller sends contiguous '1's on the bus. In both cases, the bus controller monitors the bus.

iv) If, during transmitting the header, the bit value transmitted and the monitored bit value are not the same, the bus controller stops transmitting the header and sets $h = 1$, which means that the bus controller loses in contention. However, the bus controller goes on monitoring the bus.

v) After monitoring the bus during the header duration, the bus controller sets p to the monitored priority field value and sets f to the monitored

fairness bit value. And the bus controller sets F_i $(i < p)$ to zero. If f is 1, the bus controller also sets F_p to zero. This procedure is for the fair access scheme.

vi) If $h = 1$, then go to step (i). If not, the bus controller sets A low and transmits the data field of the packet associated with the header. During the transmission of the packet data field, the bus controller does not monitor the bus.

vii) After the successful transmission of the packet, the bus controller sets F_p to '1' and A high. Then go to step (i).

B. *Start pulse generator(SPG)*: an SPG operates as follows.

i) The SPG monitors the active line and waits until the active line becomes high. When the active line becomes high, then go to step (ii).

ii) The SPG generates a start pulse on the start line and monitors the bus.

iii) If consecutive M bits of '1's are detected on the bus during the header duration, then go to step (ii). If not, go to step (iv).

iv) The SPG waits until the active line becomes low. Low active line means that a transmission of a packet data field is going on. Go to step (i).

C. *Address filter(AF)*: when a start pulse comes through the start line, it begins to monitor the bus. If the destination address field which is received from the bus is the same as the address of the station, it receives the packet and stores it in one of the output queues according to its priority level.

D. *Transmitter(TX)*: a transmitter sends to the output link the HOL packet of the highest priority output queue which is not empty.

Ⅲ. Queueing Model and Delay Analysis

In this paper, we consider the switch with two priority levels. However, the delay analysis which follows can be applied to the case of more than two priority levels. Since we assume two priority levels, there are

high-priority packets and low-priority packets in the switch. We assume that all stations have the arrivals of high-priority packets and low-priority packets independently, according to Poisson distribution processes. The packet length distribution is arbitrary and all stations have the same packet length distribution for each priority level. We consider the stations with asymmetric arrival rates. The destination addresses of input queues are independent and uniformly distributed among all the output ports. We assume that the bus data rate m_2 is H times of the output link data rate m_1, that is $m_2 = H \cdot m_1$. The symbols to be used are defined as follows.

N	Number of stations.
$\lambda_{in, high(low), i}$	Arrival rate to the high(low)-priority input queue of the i-th station.
$\lambda_{in, high(low)}$	Total arrival rate to the high(low)-priority input queues of the switch.
$\lambda_{out, high(low), i}$	Arrival rate to the high(low)-priority output queue of the i-th station.
$a_{in, high(low)}$	Random variable(r.v.) representing high (low)-priority packet service time for the bus.
$a_{out, high(low)}$	R.v. representing high(low)-priority packet service time for output links.
$\rho_{bus, high(low)}$	Bus utilization by all high(low)-priority packets.
$\rho_{outlink, high(low)}$	Utilization of an output link by high(low)-priority packets.

We note that the following relations hold:

$$\lambda_{in, high(low)} = \sum_{i=1}^{N} \lambda_{in, high(low), i} , \quad \rho_{bus, high(low)}$$

$$= \lambda_{in, high(low)} \cdot a_{in, high(low)} . \qquad (1)$$

Since the output addresses of input queues are uniformly distributed among all the outputs, we have the following relation.

$$\lambda_{out, high(low), i} = \frac{\lambda_{in, high(low)}}{N} ,$$

$$\rho_{outlink, high(low)} = \frac{\lambda_{in, high(low)}}{N} \cdot a_{out, high(low)} \qquad (2)$$

Since the M bit header is not transmitted at output links and $m_2 = H \cdot m_1$, we have

$$a_{out, high} = H \cdot (a_{in, high} - M), \quad a_{out, low} = H \cdot (a_{in, low} - M). \qquad (3)$$

Let us assume that the tagged packet belongs to the N-th queue without the loss of generality.

3.1 Packet Delay in Input Queues
A. Queueing Model

Our analyses of high-priority packet delay and low-priority packet delay will be done through one queueing model which will be called the reference system.

In this system there are two priority classes. The number of high-priority queues is N, and the arrival distributions of the high-priority queues are assumed to be Poisson. The number of low-priority queues is only one, and the arrival distribution is arbitrary. Both the high-priority and low-priority queues are assumed to have an infinite waiting room. Each high-priority queue in normal-level contends for bus access and is selected in random. If one high-priority queue succeeds in bus access and in a transmission of a packet, normal-level is changed into lower-level. Only high-priority queues in normal-level can contend for bus access. Lower-level returns back to normal-level when there are no non-empty high-priority queues in normal-level. The low-priority packets can be transmitted on the bus only when there are no packets in the high-priority queues.

The high-priority packet length is represented by a r.v. b, and the arrival rate of the i-th high-priority queue is λ_i. The utilization of the bus by the packets of the i-th high-priority queue only is then $\rho_i = \lambda_i E(b)$ where $E(\cdot)$ denotes expectation. And ρ is the total utilization by all high-priority queue packets. The low-priority packet length is represented by a r.v. b_L.
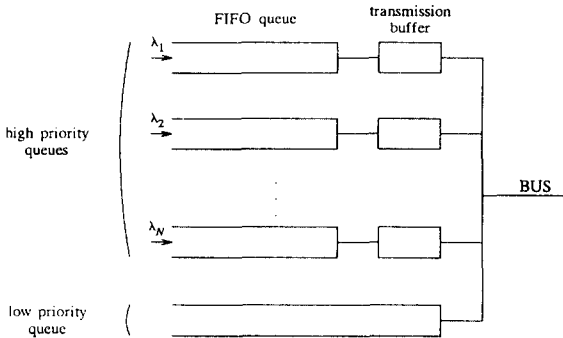
Fig. 3 Queueing model for the reference system.

Here we analyze the queueing delay of high-priority packets. In our analysis, we divide a high-priority queue into two parts, a first-in-first-out(FIFO) queue and a transmission buffer. The transmission buffer is an extension of the FIFO queue, and only one packet is permitted to enter the transmission buffer. In a high-priority queue the packet at the head of the FIFO queue will enter the transmission buffer when it is empty. This packet in the transmission buffer will be in contention for bus access. Accordingly, the queueing delay of high-priority queues consists of two delay factors. One is the delay from which a packet suffers in the FIFO queue (this delay will be referred to the pure queueing delay), and the other is the delay from which a packet suffers in the transmission buffer (this delay will be called the contention delay).

The pure queueing delay is expressed as a r.v. w, and the contention delay is expressed as a r.v. y. The total queueing delay, represented by a r.v. d, is the sum of the pure queueing delay and the contention delay. That is, $d = w + y$. w and y are assumed to be independent. Therefore, we have $D^*(s) = W^*(s)Y^*(s)$ where $D^*(s)$, $W^*(s)$ and $Y^*(s)$ are, respectively, the Laplace transforms (LT) of probability density functions (pdf) of d, w and y.

B. Distribution of Pure Queueing Delay

We now define a cycle as a time interval of a busy period during which the high-priority packets of normal-level are served continuously. Therefore, at most one packet from a high-priority queue can be served in each cycle. Let us define the N-th conditional cycle as the cycle which includes the service of the N-th high-priority queue packet. Since at most one packet can be sent from a high-priority queue in each cycle, the tagged packet of the N-th high-priority queue moves one position forward in the queue after each cycle.

The N-th conditional cycle is divided into two cases. One is made when a packet arrives at the N-th high-priority queue and finds that the queue is empty in normal-level. In this case, we let a r.v. c_0 be the interval between the arrival time of the packet and the end time of the cycle. The other case is made when a packet arrives at the N-th high-priority queue and finds that the queue is not empty or empty in lower-level. In this case, we let a r.v. c be the cycle time which includes the service of the packet.

We apply a modified M/G/1 queueing model to the analysis of the pure queueing delay of the N-th high-priority queue. In the modified M/G/1 queueing model, the packet service time is c, but the service time of a packet which arrives at the empty queue is c_0. In the modified M/G/1 queueing model, let $\tilde{q}_k$ be the number of packets in the queue left behind by j-th packet transmission. Then we have

$$\tilde{q}_{j+1} = \begin{cases} \tilde{q}_j - 1 + \tilde{v} & \tilde{q}_j > 0 \\ \tilde{v}_0 & \tilde{q}_j = 0, \end{cases} \qquad (4)$$

where $\tilde{v}$ and $\tilde{v}_0$ are r.v.'s representing the number of packets arriving during packet service time. Let $\tilde{V}(z)$ and $\tilde{V}_0(z)$ be the Z-transforms of the r.v.'s $\tilde{v}$ and $\tilde{v}_0$, respectively. Then from [5], we have

$$\tilde{V}(z) = C^*(\lambda_N - \lambda_N z), \qquad \tilde{V}_0(z) = C_0^*(\lambda_N - \lambda_N z) \qquad (5)$$

where $C^*(s)$ and $C_0^*(s)$ are, respectively, the LT's of c, c_0.

From (4) and (5), we can obtain a relation between $\tilde{Q}_{j+1}(z)$ and $\tilde{Q}_j(z)$ which are the Z-transforms of $\tilde{q}_{j+1}$ and $\tilde{q}_j$, respectively. Considering the limiting case and defining that $q = \lim_{j \to \infty} \tilde{q}_j$ and $Q(z) = \lim_{j \to \infty} \tilde{Q}_j(z)$, we have

$$Q(z) = P[q=0] \frac{z C_0^*(\lambda_N - \lambda_N z) - C^*(\lambda_N - \lambda_N z)}{z - C^*(\lambda_N - \lambda_N z)} \qquad (6)$$

Let a r.v. g be the system time of a packet in the modified M/G/1 queueing model and let $G^*(s)$ be the LT of g. Since the number of packets in the queue left behind by packet transmissions has the same distribution as the number of packets arriving during the system time g, we have from [5]

$$G^*(s) = P[q=0] \frac{(\lambda_N - s) C_0^*(s) - \lambda_N C^*(s)}{\lambda_N - s - \lambda_N C^*(s)} . \qquad (7)$$

Since g is the sum of the pure queueing delay w, and the packet service time of the modified M/G/1 queueing model, we have $g = w + P[q=0] \cdot c_0 + (1 - P[q=0]) \cdot c$. Thus, $W^*(s)$ is given by

$$W^*(s) = \frac{G^*(s)}{P[q=0] \cdot C_0^*(s) + (1 - P[q=0]) \cdot C^*(s)} . \qquad (8)$$

(i) *Distribution of c*: let α_i be the probability that the service of a packet of the i-th high-priority queue $(i \neq N)$ is included in the time c. The mean value of c can be expressed as

$$E(c) = E(b) + \sum_{i=1}^{N-1} \alpha_i E(b). \qquad (9)$$

Approximating α_i by $\lambda_i E(c)$, we have $E(c) = \dfrac{E(b)}{1 - \rho + \rho_N}$.

Note that α_i should be equal to or less than 1 so that it may be interpreted as a probability. Assuming that all r.v.'s of (9) are independent, we can obtain the LT of the pdf of c as

$$C^*(s) = B^*(s) \prod_{i=1}^{N-1} (\alpha_i B^*(s) + (1 - \alpha_i)) \qquad (10)$$

where $B^*(s)$ is the LT of b.

(ii) *Distribution of* c_0: there are three cases when a packet arrives at the empty N-th high-priority queue in normal-level. The first is the case that the bus is occupied by a low-priority packet. The probability of the case is q_{01} and the cycle time is denoted as a r.v. c_{01}. The second is the case that the bus is occupied by a high-priority packet from another queue. The probability of the case is q_{02} and the cycle time is denoted as a r.v. c_{02}. The last is the case that the bus is free. The probability of the case is q_{03} and the cycle time is denoted as a r.v. c_{03}. Thus we have

$$P[q=0] = q_{01} + q_{02} + q_{03},$$

$$C_0^*(s) = \frac{q_{01} C_{01}^*(s) + q_{02} C_{02}^*(s) + q_{03} C_{03}^*(s)}{P[q=0]} \qquad (11)$$

where $C_{01}^*(s)$, $C_{02}^*(s)$ and $C_{03}^*(s)$ are, respectively, the LT's of c_{01}, c_{02} and c_{03}.

(iii) *Definition and distribution of* $\tilde{b}_L$: $\tilde{b}_L$ is a r.v. representing the low-priority packet service time during which one or more packets arrive at the N-th high-priority queue. Let $P_{b_L}(t)$ and $P_{\tilde{b}_L}(t)$ be the pdf's of b_L and $\tilde{b}_L$, respectively. Also, let $B_L^*(s)$ and $\tilde{B}_L^*(s)$ represent the LT's of bL and $\tilde{b}_L$, respectively. When the service of a low-priority packet starts, there are no packets present in the high-priority queues. While the low-priority packet is being served, a high-priority packet may or may not arrive. The probability that one or more packets arrive at the N-th high-priority queue during the service of a low-priority packet should be proportional to the value of $(1 - e^{-\lambda_N b_L})$ as well as to the relative occurrence of such durations[5]. Thus, we may write $P_{\tilde{b}_L}(t) = \tilde{K}(1 - e^{-\lambda_N t}) P_{b_L}(t)$, where $\tilde{K}$ is a proportionality constant. The constant $\tilde{K}$ can be evaluated so as to properly normalize the pdf $P_{\tilde{b}_L}(t)$. Then, we have

$$P_{\tilde{b}_L}(t) = \frac{1 - e^{-\lambda_N t}}{1 - B_L^*(\lambda_N)} P_{b_L}(t)$$

$$\tilde{B}_L^*(s) = \frac{B_L^*(s) - B_L^*(s + \lambda_N)}{1 - B_L^*(\lambda_N)} . \qquad (12)$$

(iv) *Distribution of* c_{01} : the cycle time c_{01} is made when a packet arrives at the empty N-th high-priority queue during a low-priority packet service. The low-priority packet service time is represented as the r.v. $\tilde{b}_L$. We use the concept of conditional cycle time for obtaining the distribution of c_{01}. Let β_i be the probability that the service of a packet of the i-th high-priority queue($i \neq N$) is included in the time c_{01}. We assume that the mean value of c_{01} is expressed as

$$E(c_{01}) = E(\tilde{b}_L) + E(b) + \sum_{i=1}^{N-1} \beta_i E(b). \qquad (13)$$

Approximating β_i by $\lambda_i E(c_{01})$, we have $E(c_{01}) = \dfrac{E(\tilde{b}_L) + E(b)}{1 - \rho + \rho_N}$. Note that β_i should be equal to or less than 1 so that it may be interpreted as a probability. Assuming that all r.v.'s in (13) are independent, we can obtain the LT of c_{01} as

$$C_{01}{}^*(s) = \tilde{B}_L{}^*(s) B^*(s) \prod_{i=1}^{N-1} (\beta_i B^*(s) + (1 - \beta_i)). \qquad (14)$$

(v) *Definition and distribution of* $r(x, \lambda)$: let a r.v. r (x, λ) be the residual time of the duration which is denoted as a r.v. x, at the first Poisson arrival with rate λ(see Fig. 4). In the definition of $r(x, \lambda)$, we exclude the case that there are no arrivals. Thus we have $r(x, \lambda) > 0$. From [5], we can obtain $P_{r(x, \lambda)}(t)$ and $R^*(x, \lambda, s)$, which are respectively the pdf and LT of $r(x, \lambda)$, as
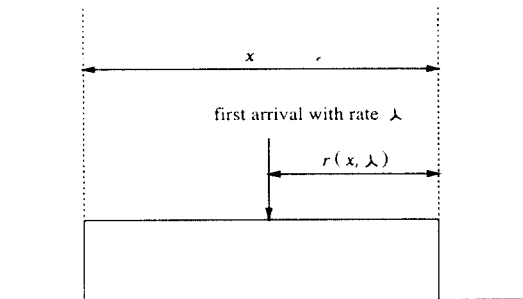

Fig. 4 Definition of $r(x, \lambda)$.

$$P_{r(x, \lambda)}(t) = \frac{\lambda e^{\lambda t}}{1 - X^*(\lambda)} \int_t^\infty e^{-\lambda t} P_x(t) dt \text{ and} \qquad (15)$$

$$R^*(x, \lambda, s) = \frac{\lambda}{(1 - X^*(\lambda))(s - \lambda)} [X^*(\lambda) - X^*(s)], \qquad (16)$$

where $P_x(t)$ and $X^*(s)$ are respectively the pdf and LT of x.

(vi) *Distribution of* c_{02} : the cycle time c_{02} is made when a packet arrives at the empty N-th high-priority queue during the service of a high-priority packet from another queue. Let a r.v. $\tilde{f}$ be $c - b$. We also assume that the LT of $\tilde{f}$, $\tilde{F}^*(s)$ is given by $\dfrac{C^*(s)}{B^*(s)}$. Since it can be considered that the packet which makes the cycle c_{02} arrives in the interval of $\tilde{f}$, we can get c_{02} approximately as $c_{02} = r(\tilde{f}, \lambda_N) + b$. Thus, we have $C_{02}^*(s)$ $= R^*(\tilde{f}, \lambda_N, s) B^*(s)$.

(vii) *Distribution of* c_{03} : the cycle time c_{03} is made when a packet arrives at the empty N-th high-priority queue and finds the bus idle. Since the arrival time of the packet is a starting point of an N-th conditional cycle, we can approximate c_{03} by c. Thus, we have c_{03} $= c$ and $C_{03}^*(s) = C^*(s)$.

(viii) *Value of probability* q_{02} : the values of the probabilities q_{01} and q_{03} are given later. The cycle c_{02} begins when a packet arrives at the empty N-th high-priority queue during the service of a high-priority packet from another queue. Since the packet on the bus is from one of the high-priority queues except the N-th high-priority queue, q_{02} is approximated by $\rho - \rho_N$.

C. Distribution of Contention Delay

The contention delay from which packets arriving at the non-empty N-th high-priority queue or at the empty N-th high-priority queue in lower-level suffer is denoted as a r.v v. And the probability of having that case is $1 - P[q = 0]$. The contention delay from which packets arriving at the empty N-th high-priority queue in normal-level suffer is denoted as a r.v v_0. And the probability of having that case is $P[q = 0]$. There are three cases when a packet arrives at the empty N-th

high-priority queue in normal-level. The first is the case that the bus is occupied by a low-priority packet. The probability of the case is q_{01} and the contention delay of the N-th high-priority queue packet in the case is denoted as v_{01}. The second is the case that the bus is occupied by a high-priority packet from another queue. The probability of the case is q_{02} and the contention delay of the N-th high-priority queue packet in the case is denoted as v_{02}. The last is the case that the bus is free. The probability of the case is q_{03} and the contention delay of the N-th high-priority queue packet in the case is denoted as v_{03}. Let $V^*(s)$, $V_0^*(s)$, $V_{01}^*(s)$, $V_{02}^*(s)$ and $V_{03}^*(s)$ be the LT's of v, v_0, v_{01}, v_{02} and v_{03}, respectively. Then we have

$$Y^*(s) = (1 - P[q=0]) \cdot V^*(s) + P[q=0] \cdot V_0^*(s), \text{ and } \quad (17)$$

$$V_0^*(s) = \frac{q_{01} \cdot V_{01}^*(s) + q_{02} \cdot V_{02}^*(s) + q_{03} \cdot V_{03}^*(s)}{P[q=0]} . \quad (18)$$

(i) *Distribution of v* : in the cycle time c, the probability that a packet from the i-th high-priority queue $(i \neq N)$ is served is α_i. Thus the probability that there do not exist any packets except the packet from the N-th high-priority queue in the cycle is $\prod_{j=1}^{N-1} (1 - \alpha_j)$. In that case, v becomes zero. The probability that only a packet from the i-th high-priority queue is served with the packet from the N-th high-priority queue in the cycle is $\alpha_i \cdot \prod_{j=1, j \neq i}^{N-1} (1 - \alpha_j)$. In that case, v becomes $\frac{1}{2} \cdot 0 + \frac{1}{2} b$. In this way, we can get $V^*(s)$ as

$$V^*(s) = \sum_{h_1=0}^{1} \sum_{h_2=0}^{1} \cdots \sum_{h_{N-1}=0}^{1} \prod_{j=1}^{N-1} \gamma_{h_j} \frac{1}{m} \frac{1 - (B^*(s))^m}{1 - B^*(s)} \quad (19)$$

where $\gamma_{h_j} = h_j \alpha_j + (1 - h_j)(1 - \alpha_j)$ and $m = \sum_{j=1}^{N-1} h_j + 1$.

(ii) *Distribution of v_{01}* : a packet which arrives at the empty N-th high-priority queue during the low-priority packet service on the bus has to wait for bus access until the low-priority packet service finishes. The

residual time of the low-priority packet service is represented as $r(b_L, \lambda_N)$. At the end of the low-priority packet service, the probability that the i-th high-priority queue$(i \neq N)$ is not empty is given by $1 - \tilde{B}_L^*(\lambda_i)$. In obtaining the distribution of v_{01}, we neglect the high-priority packet arrivals after the end of the low-priority packet service, for simplicity of analysis. The packet from the N-th high-priority queue contends for bus access with the packets from the other non-empty high-priority queues. Let us define δ_{h_j} as $\delta_{h_j} = h_j(1 - \tilde{B}_L^*(\lambda_j)) + (1 - h_j)\tilde{B}_L^*(\lambda_j)$. By the similar procedure for obtaining $V^*(s)$, we have

$$V_{01}^*(s) = R^*(b_L, \lambda_N, s) \cdot \sum_{h_1=0}^{1} \sum_{h_2=0}^{1} \cdots \sum_{h_{N-1}=0}^{1} \prod_{j=1}^{N-1}$$
$$\delta_{h_j} \frac{1}{m} \frac{1 - (B^*(s))^m}{1 - B^*(s)} \quad (20)$$

where $m = \sum_{j=1}^{N-1} h_j + 1$.

(iii) *Distribution of v_{02}* : the packet, which arrives at the empty N-th high-priority queue in normal-level and finds a high-priority packet from another queue is served on the bus, has to wait for bus access until the end of the current high-priority packet service. The residual time of the high-priority packet service is represented as $r(b, \lambda_N)$. We let t_a be the end time of the packet service. Thus, at the time t_a, the packet of the N-th high-priority queue begins to contend for bus access with the packets of the other high-priority queues. We let t_b be the start time of the last packet service in the cycle to which they belong. We can get the time interval $f_1 = t_b - t_a$ approximately and it is given by $f_1 = r(\tilde{f}, \lambda_N) - r(b, \lambda_N)$. We let t_c be the start time of the N-th high-priority queue packet service. We assume that t_c is uniformly distributed on f_1. We let f_2 be the interval of $t_c - t_a$. We let $P_{f_1}(t)$ and $P_{f_2}(t)$ be the pdf's of f_1 and f_2, respectively. We also let $F_1^*(s)$ and $F_2^*(s)$ be the LT's of f_1 and f_2, respectively. $F_1^*(s)$ can be given by $F_1^*(s) = \frac{R^*(\tilde{f}, \lambda_N, s)}{R^*(b, \lambda_N, s)}$. Since f_2 is uniformly

distributed on f_1, we have $P_{f_1}(t) = \int_t^\infty \dfrac{P_{f_1}(t)}{x} dx$ and

$F_2^*(s) = \dfrac{1}{s} \int_{s_1=0}^s F_1^*(s_1) ds_1$. Therefore, we have $v_{02} = r(b, \lambda_N) + f_2$ and $V_{02}^*(s) = R^*(b, \lambda_N, s) \cdot F_2^*(s)$.

(iv) *Distribution of* v_{03} : when the bus is idle, a packet which arrives at an empty high-priority queue in normal-level is served immediately. Thus, we have $v_{03} = 0$ and $V_{02}^*(s) = 1$.

D. Analysis of High Priority Packet Delay

For the analysis of high-priority packets in the asynchronous switch, we use the results of the analysis of the reference system. We consider all low-priority packet queues in the asynchronous switch as a single queue with the arrival rate $\lambda_{in,\ low}$. Considering a high-priority packet in the switch as a high-priority packet in the reference system and a low-priority packet in the switch as a low-priority packet in the reference system, the switch system is similar to the reference system. We have the following relations:

$$b = a_{in,\ high}, \quad b_L = a_{in,\ low}, \quad \lambda_i = \lambda_{in,\ high,\ i}, \quad \text{and}$$

$$\rho = \sum_{i=1}^{N} \lambda_i E(b) \qquad (21)$$

During a low-priority packet service time, b_L, a packet may or may not arrive at the N-th high-priority queue. The probability that one or more packets arrive at the N-th high-priority queue during the low-priority packet service time is $1 - \tilde{B}_L^*(\lambda_N)$. The average number of such low-priority packets in unit time is given by $\lambda_{in,\ low}(1 - B_L^*(\lambda_N))$. Thus we have $q_{01} = \dfrac{\lambda_{in,\ low}}{\lambda_N}$ $(1 - B_L^*(\lambda_N))$. Since the cycle c_{03} begins when the bus is idle, the probability q_{03} is given by $q_{03} = 1 - \rho_{bus,\ high} - \rho_{bus,\ low}$.

E. Analysis of Low Priority Packet Delay

For the analysis of low-priority packets in the asynchronous switch, we use the results of the analysis of the reference system. We consider all high-priority

queues in the asynchronous switch as a single queue with the arrival rate $\lambda_{in,\ high}$ and the service time distribution $a_{in,\ high}$. When a low-priority packet gets service, there is no high-priority packet present in the switch. While it is being served, high-priority packets may arrive. Before the next low-priority packet is served or until the bus is idle, those arriving high-priority packets and their successors must be served. The service time of a low-priority packet ahead of the one waiting in the low-priority queue consists of $a_{in,\ low}$ and the time required to get the switch system free of high-priority packets. This time interval will be called the blocking time. Denoting the LT of the distribution of blocking time $\tilde{h}$ as $\tilde{H}^*(s)$, we have from the renewal theory[5]

$$\tilde{H}^*(s) = A^*_{in,\ low}(s + \lambda_{in,\ high} - \lambda_{in,\ high} T^*(s)) \qquad (22)$$

where $T^*(s) = A^*_{in,\ high}(s + \lambda_{in,\ high} - \lambda_{in,\ high} T^*(s))$, and $A^*_{in,\ high}(s)$, $A^*_{in,\ low}(s)$ are the LT's of $a_{in,\ high}$, $a_{in,\ low}$, respectively. Then, $\tilde{h}$ can be equivalently considered as the service time of a low-priority packet. Considering a low-priority packet in the switch as a high-priority packet with an equivalent service time of $\tilde{h}$ in the reference system, this switch system is similar to the reference system. Hence, we have the following relations:

$$B^*(s) = \tilde{H}^*(s), \quad \lambda_i = \lambda_{in,\ low,\ i}, \quad \text{and} \quad \rho = \sum_{i=1}^{N} \lambda_i E(b). \quad (23)$$

b_L is effectively the busy period of the high-priority packets generated only when the bus is idle. Then, from the renewal theory[5], we find $B_L^*(s) = A^*_{in,\ high}(s + \lambda_{in,\ high} - \lambda_{in,\ high} B_L^*(s))$. The cycle c_{01} can be generated when a packet arrives at the N-th low-priority queue of the switch during b_L. Since the average number of occurrences of bL in unit time is $\lambda_{in,\ high}(1 - \rho_{bus,\ high} - \rho_{bus,\ low})$, the average number of cycle c_{01} in unit time is given by $\lambda_{in,\ high}(1 - \rho_{bus,\ high} - \rho_{bus,\ low})(1 - B_L^* (\lambda_N))$. Thus we have $q_{01} = \dfrac{\lambda_{in,\ high}}{\lambda_N} \cdot (1 - \rho_{bus,\ high} - \rho_{bus,\ low})$

$(1 - B_L^*(\lambda_N))$. Since the cycle c_{03} begins when the bus is idle, the probability q_{03} is given by $q_{03} = 1 - \rho_{bus,\ high}$ $- \rho_{bus,\ low}$.

IV. Simulation Results and Discussion

In this section, we compare numerical results with simulation results for the mean packet delay of the asynchronous switch. Figs. 5 through 8 show the comparisons of the mean packet delay of input queues of the N-th station, in the case of asymmetric systems where $\lambda_{in,\ high,\ N} = 2 \cdot \lambda_{in,\ high,\ i}$ and $\lambda_{in,\ low,\ N} = 2 \cdot \lambda_{in,\ low,\ i}$ for $1 \leq i \leq N-1$.

In these figures, it is seen that the numerical results have good agreement with the simulation results for low-to-medium values of $\rho_{bus,\ high}$ for the high-priority packet delay and $\rho_{bus,\ high} + \rho_{bus,\ low}$ for the low-priority packet delay. The high-priority packet always
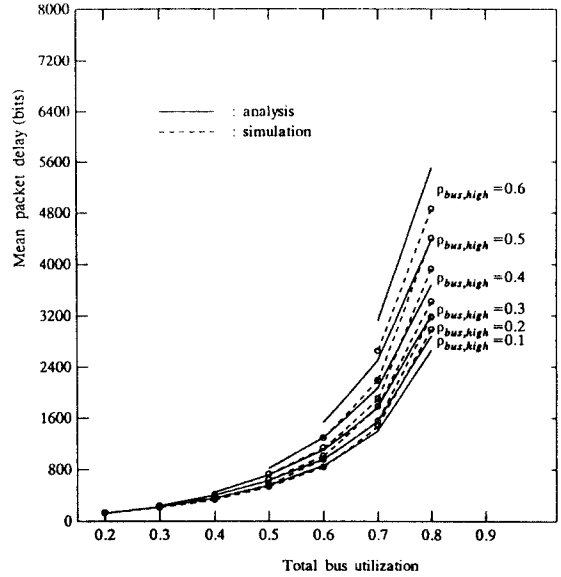

Fig. 6 Mean packet delay in the N-th low priority input queue: $N = 7$, $H = 6$, geometric packet data field length with mean 424, $\lambda_{in,\ low,\ N} = 2\lambda_{in,\ low,\ i}$ for $1 \leq i \leq N-1$, $M = 8$, $n = 3$, and $k = 1$.
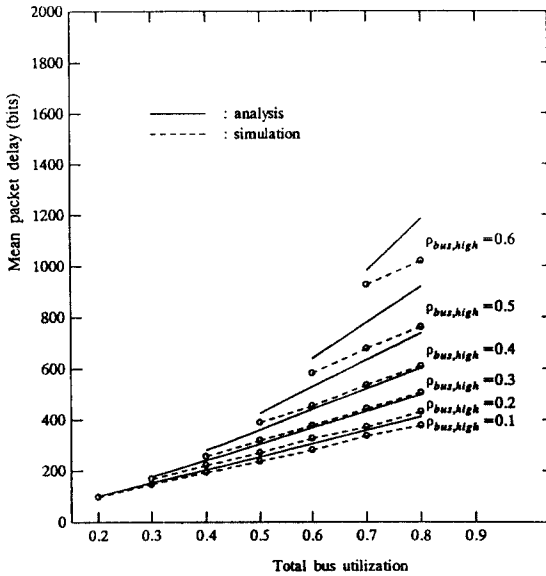

Fig. 5 Mean packet delay in the N-th high priority input queue: $N = 7$, $H = 6$, geometric packet data field length with mean 424, $\lambda_{in,\ high,\ N} = 2\lambda_{in,\ high,\ i}$ for $1 \leq i \leq N-1$, $M = 8$, $n = 3$, and $k = 1$.
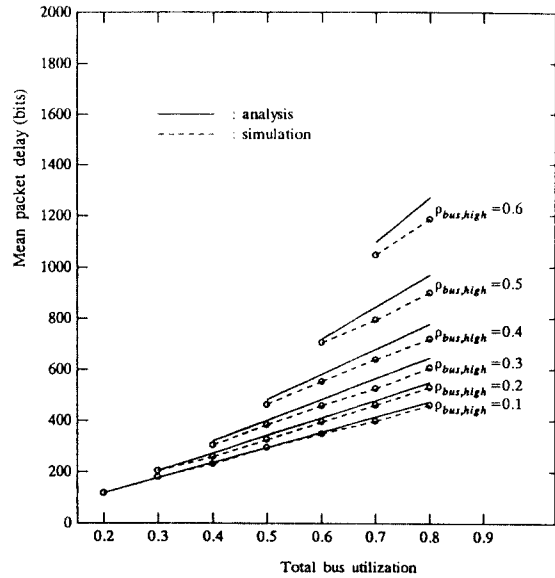

Fig. 7 Mean packet delay in the N-th high priority input queue: $N = 15$, $H = 14$, fixed packet data field length with mean 1024, $\lambda_{in,\ high,\ N} = 2\lambda_{in,\ high,\ i}$ for $1 \leq i \leq N-1$, $M = 10$, $n = 4$, and $k = 1$.
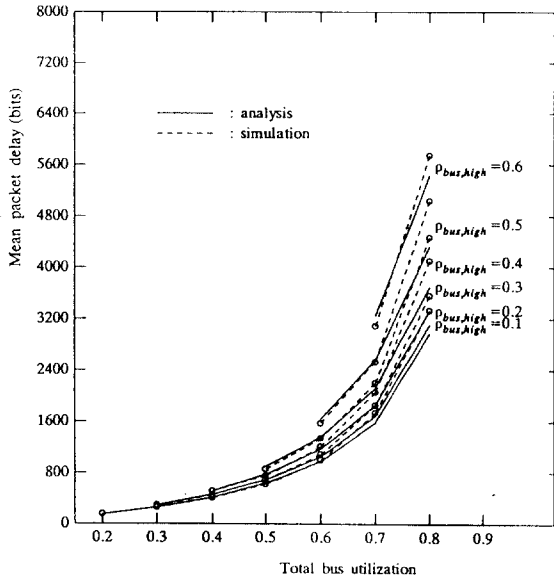
Fig. 8 Mean packet delay in the N-th low priority input queue: $N = 15$, $H = 14$, fixed packet data field length with mean 1024, $\lambda_{in, low, N} = 2\lambda_{in, low, i}$ for $1 \leq i \leq N - 1$, $M = 10$, $n = 4$, and $k = 1$.

has non-preemptive priority over to the low-priority packet in the switch. Therefore, the high-priority packet will receive service before any waiting low-priority packet even though it might arrive later. Consequently, when the utilization of the high-priority packet is fixed, the high-priority packet delay increases slightly although the total bus utilization tends to be unity. It can be said from the figures that the low-priority packet utilization has little effect on the high-priority packet delay.

V. Conclusions

In this paper, we proposed an architecture of an asynchronous shared-bus type switch with priority and fairness schemes. The switch architecture is an input and output queueing system, and the priority scheme is implemented in both input and output queues.

We analyzed the packet delay of both input and output queues. We considered only a two-priority system. However, the analysis can easily be extended to a system with more than two priority levels. We made some approximations in the analyses. However, the numerical results show good agreements with the simulation results.

References

1. J.S. Turner, "Design of an integrated services packet network," *IEEE Select. Areas Commun.*, vol. SAC-4, pp. 1373-1380, Nov. 1986.

2. F.A. Tobagi, "Fast Packet Switch Architectures for Broadband Integrated Services Digital Networks," *Proc. IEEE*, vol. 78, pp. 133-167, Jan. 1990.

3. H. Ahmadi and W.E. Denzel, "A Survey of Modern High-Performance Switching Techniques," *IEEE Select. Areas Commun.*, vol. SAC-7, pp. 1091-1103, Sep. 1989.

4. P. J. Kuehn, "Multiqueue System with Non-exhaustive Cycle Service", *Bell System Technical Journal*, Vol. 58, No. 3, March, 1979.

5. L. Kleinrock, *Queueing Systems Vol. I: Theory*, John Wiley & Sons, 1975.

6. R. W. Conway, W. I. Maxwell and L. W. Miller, *Theory of Scheduling*, Addison-Wesley, 1967.

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