Fabrication of Novel Metal Field Emitter Arrays(FEAs) Using Isotropic Silicon Etching and Oxidation

Chang-Woo Oh, Chun-Gyoo Lee, Byung-Gook Park, Jong-Duk Lee, and Jong-Ho Lee

Abstract

A new metal tip fabrication process for low voltage operation is reported in this paper. The key element of the fabrication process is that isotropic silicon etching and oxidation process used in silicon tip fabrication is utilized for gate hole size reduction and gate oxide layer. A metal FEA with 625 tips was fabricated in order to demonstrate the validity of the new process and submicron gate apertures were successfully obtained from originally 1.7 μm diameter mask. The emission current above noise level was observed at the gate bias of 50V. The required gate voltage to obtain the anode current of 0.1 μA/tip was 74V and the emission current was stable above 2 μA/tip without any disruption. The local field conversion factor and the emitting area were calculated as $7.981 \times 10^5 cm^{-1}$ and $3.2 \times 10^{-14} cm^2$/tip, respectively.

I. Introduction

Since the first invention of thin-film field emission cathode (TFFEC) in 1968 based on an electron beam evaporation scheme [1], the optimum geometry and the fabrication method of the device to improve emission characteristics have been intensively investigated[2, 3].

For most applications of microfabricated field emitter arrays (FEAs), it is important to have as low an operating voltage as possible in order to minimize demands on the drive electronics and to maximize device reliability[4]. The tip emission is strongly dependent on the diameter of the gate hole and on the height of the tip with respect to the top of the gate electrode[5]. The gate aperture is more important parameter than the tip height for low voltage operation, because the height of the tip can be always optimized in most field emitters. From this point of view, uniform and reliable gate hole size reduction even with a conventional photolithography is a good solution for low cost as well as for low voltage operation.

A metal tip process with local oxidation of silicon (LOCOS) was proposed and successfully fabricated[6]. The key element of this metal tip process is forming the gate insulator by LOCOS, resulting in the reduction of the gate hole size due to the lateral encroachment of oxide. In terms of the process margin, it is somewhat difficult to form gate holes uniformly on a substrate. The buffer oxide removal to form a gate hole can bring some spatial variation of gate hole size. The smaller the gate hole is, the thinner the gate oxide between the gate metal and the silicon substrate around the gate hole might be. For thermally grown SiO_2, a field of 7×10^6 Vcm^{-1} generally lead to irreversible breakdown and the thickness of 5 nm/V is needed to allow a margin for safety[7]. To obtain high current density, a thicker gate oxide around the gate hole is required. Therefore, to overcome the weakness, we propose a new fabrication process using isotropic silicon etching and oxidation without any sacrifice of merits that the metal tip using LOCOS has.

The basic concept of the new metal tip fabrication process is that isotropic silicon etching and oxidation process used for silicon tip formation is utilized for gate hole size reduction and gate oxide layer formation. There is virtually no limitation in gate hole size reduction. Even if a gate hole is sufficiently reduced, the gate oxide around the gate hole can be thick enough.

II. Fabrication

The new fabrication process of metal FEAs with submicron gate apertures is shown in Figure 1. As a starting material, a boron-doped (100)-oriented silicon wafer with a resistivity of 10 ~20 Ω-cm was used. A cathode electrode was formed by phosphorus diffusion. A 210 nm-thick silicon nitride was conformally deposited using low pressure chemical vapor deposition (LPCVD). Then, the nitride film was patterned into 1.7 μm-diameter disks using a conventional aligner and a reactive ion etcher (RIE). 200 nm silicon was etched by RIE, for easy oxidation under nitride

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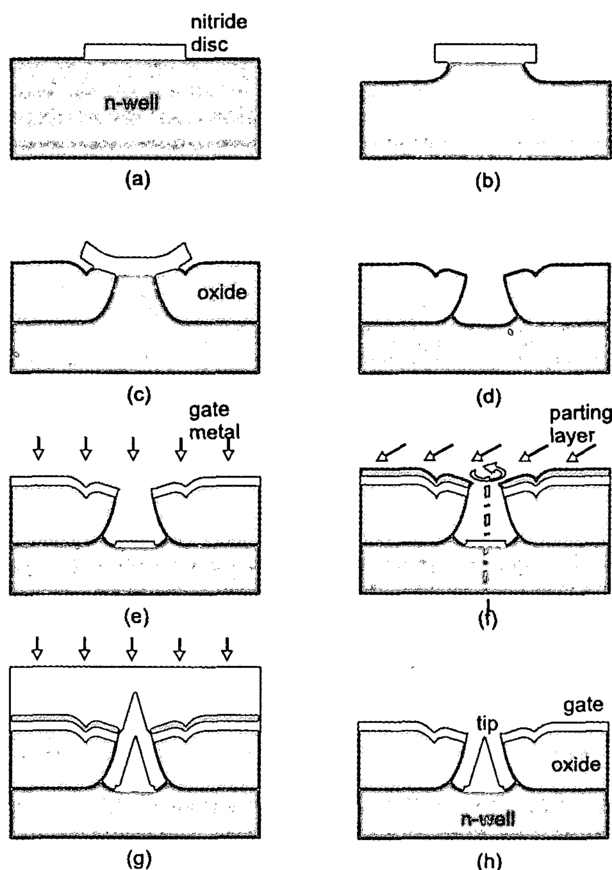


Fig. 1. Process sequences of a new metal field emitter using isotropic silicon etching and oxidation.

disks, and the exposed surface was thermally oxidized to form a 630 nm gate oxide layer. The nitride disk was removed in phosphoric acid. The exposed silicon was isotropically etched by RIE using SF_6 to form a gate hole. In these steps, the diameter of the gate hole reduced from 1.7 μm to 0.7 μm. Thereafter, the conventional Spindt process was applied.

Molybdenum was evaporated perpendicularly on the wafer by a E-gun evaporator in order to avoid the bridging between the gate and the cathode. Aluminum was deposited at a grazing angle to form a parting layer by E-gun evaporation. Then, molybdenum deposition for tip formation was done. The parting layer was selectively removed in KOH solution. As a result, the fabrication of gated FEAs was completed. Process parameters are summarized in Table 1.

III. Results and Discussion

Figure 2 shows the cross-sectional scanning electron micrograph image of a gated field emitter fabricated by the new process and by LOCOS process. As shown in the figure, the newly fabricated metal emitter has thicker gate oxide around the gate hole than the metal emitter using LOCOS. This means that higher gate bias can

Table 1. Process parameters of a new metal emitter array.

Parameter	Values
Silicon substrate	P-type, (100), 10~20Ωcm
Tip mask diameter	1.7μm
Tip mask thickness (Si_3N_4)	210nm
Isotropic silicon etching	200nm
Gate dielectric thickness	630nm
Gate metal thickness	160nm
Tip to tip spacing	10μm

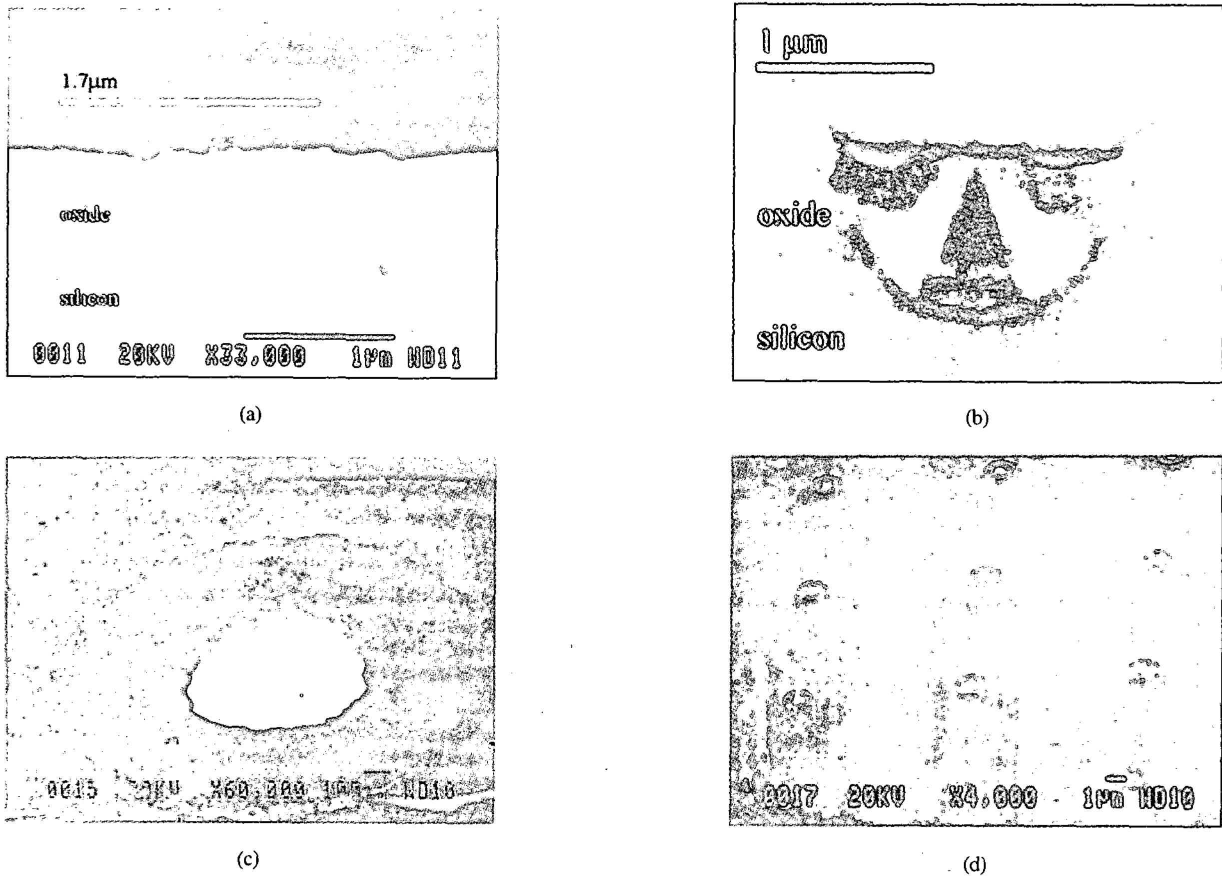
be applied to the new metal emitters, guaranteeing high current density. The nitride disk with a diameter of 1.7 μm patterned by the conventional photolithography resulted in the much smaller gate aperture with a diameter of 0.7 μm through the new process, namely, 0.6 μm reduction by etching and oxidation and 0.4 μm by the lateral encroachment of oxide. The aspect ratio of the height to the bottom diameter of the cone is about 1.3 : 1 and tip radius is less than 200 A.

In spite of the absence of a pad oxide, narrow bird's beak oxide is shown in Figure 2 (a). A similar phenomenon was investigated by J. Hui, *et al.*[8, 9]. It is thought that the stress between the nitride disk and the silicon substrate caused during oxidation generates defects, dislocations and then, relatively rapid oxidation occurs in there. However, the bird's beak can be easily eliminated by etching oxide slightly before the gate metal deposition step(Figure 3). Owing to the slope of the oxide edge, the variation of the gate hole size is negligible in Figure 3. If this bird's beak oxide is not attacked in nitride removing step (Figure 1 (c)), it might be even desirable in terms of the reduction of the gate hole and the prevention of bridging between the gate and the cathode. For this reason, the etch rate of oxide in phosphoric acid, nitride etchant, was checked. It was 12 nm/hour. This figure gives the possibility of the utilization of bird's beak oxide.

Electrical testing was performed in an ultra high vacuum (UHV) chamber at the pressure of 2.8×10^{-9} Torr. The chamber was baked at 250℃ for 10 h before testing. During the measurement, the cathode was grounded, the anode was biased at +400 V and the positive bias was applied to the gate. The distance between the anode and the gate was maintained to be about 1 mm.

Figure 4. shows the I-V characteristics obtained from FEA with 625 tips fabricated by the new process. The emission current above noise level was observed at the gate bias of 50 V. The required extraction voltage to obtain the anode current of 0.1 μA/tip was 74 V, the gate current is less than 0.2% of the anode current, and the emission current was stable above 2 μA/tip. These characteristics are comparable to the Spindt-type emitter[4]. If the peak of the tips is aligned to the top plane of the gate electrode, the highest emission current can be obtained at the same gate voltage.

The Fowler-Nordheim plot (F-N plot) is shown in Figure 5. The good linearity of F-N plot shows that the anode current and



(a) (b) (c) (d)

Fig. 2. The cross-sectional view of (a) a metal emitter with a 0.7 μm gate aperture fabricated by the new process and (b) a metal emitter with 0.55 μm gate aperture using LOCOS. The top view of (c) single emitter and (d) the field emitter array showing uniform gate apertures fabricated by the new process.

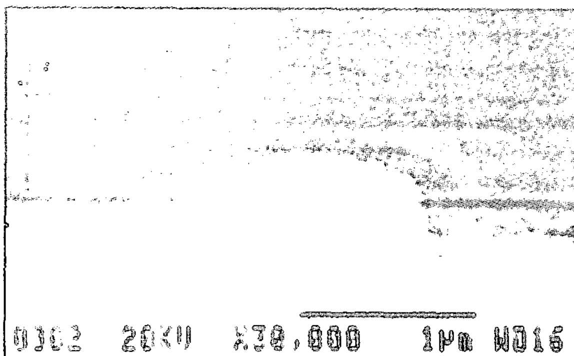


Fig. 3. The shape of the gate aperture after the slight etching of oxide by RIE.

the gate current are due to field emission.

Using the slope of the F-N straight line, F-N equation, and taking the molybdenum work function of 4.5 eV, the local field conversion factor β and the emitting area α was calculated as 7.981×10^5 cm^{-1} and 3.2×10^{-14} cm^2/tip, respectively[5]. As compared with the typical Spindt cathode, the value of a is more or less larger, which means the good emission efficiency.

Table 2. Geometrical and electrical parameters of a 625-tip array with 0.7 μm gate apertures.

Parameter	Values
Gate hole diameter	0.7μm
Tip radius	< 200Å
Tip height	1.2μm
Aspect ratio	1.3 : 1
Gate turn-on voltage	50V
Gate voltage (1 μA/tip)	74V
Field conversion factor (β)	7.981×10^5 cm^{-1}
Emitting area (α)	3.2×10^{-14} cm^2/tip

Figure 6 shows the emission current fluctuations of a new emitter array. The current was saturated after a gradual increase for about 10 hours. It seems that the initial increase of the emission current was due to the desorption of impurities adhered to tip and the saturation of the emission current was due to the stabilization of emitting surface variations.

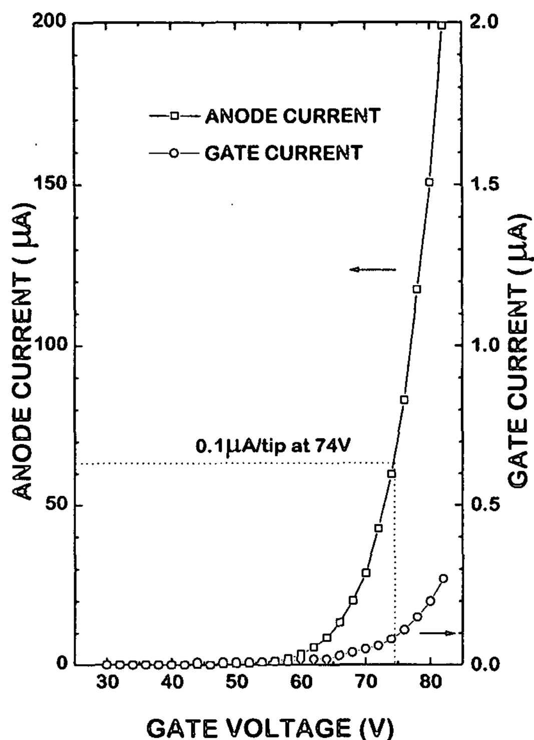


Fig. 4. I-V characteristics of a metal emitter array for 625 tips with 0.7 μm gate hole apertures.

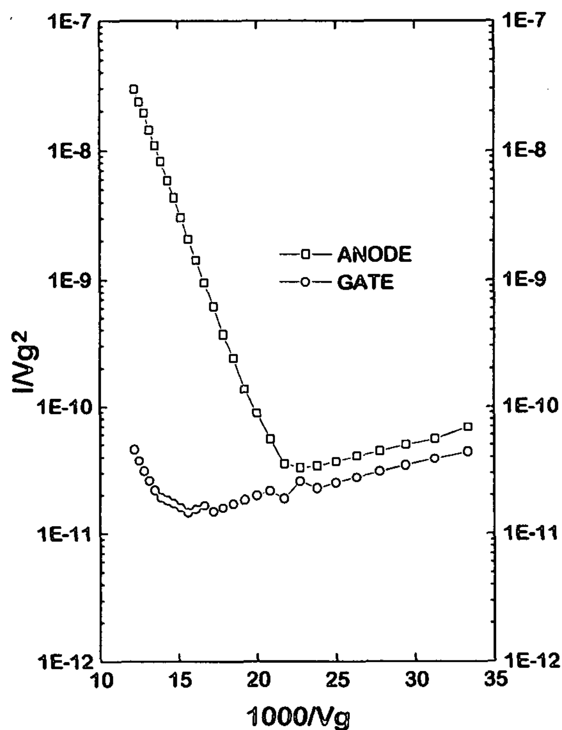


Fig. 5. The Fowler-Nordheim plot of a 625-tip array with 0.7 μm gate apertures.

Geometrical and electrical parameters was summarized in Table 2.

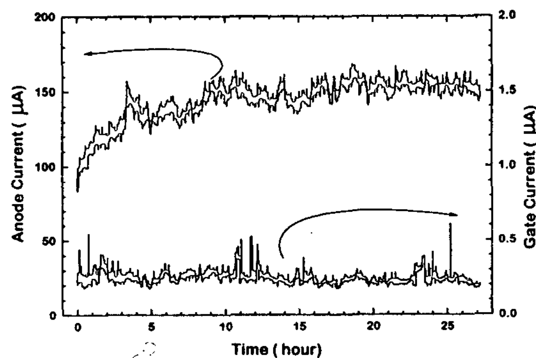


Fig. 6. The emission current fluctuations of a 625-tip array fabricated by the new process at the gate bias of 80V.

IV. Conclusion

A new metal tip fabrication process was proposed and its validity was demonstrated. The fabricated metal emitter has thick gate oxide around the gate hole, which means more stable operation and has the bird's beak, which caused by the stress between nitride disk and silicon substrate. Gate apertures of FEAs fabricated by the new process were reduced from 1.7 μm to 0.7 μm in diameter. Scaled field emitter can be easily obtained by changing the isotropic silicon etching and oxidation condition.

The electrical performance of the metal emitter is comparable to Spindt-type emitter. The anode current of 0.1 μA/tip was obtained at the gate bias of 74 V and the gate current is less than 0.2% of the anode current. The local field conversion factor and the emitting area were calculated as 7.981×10^5 cm^{-1} and 3.2×10^{-14} cm^2/tip, respectively.

It is required to study the effect of nitride film thickness on bird's beak shape, to increase the silicon recess depth, and to optimize the tip height.

Acknowledgement

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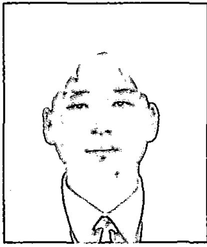

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