Dual Gate-Controlled SOI Single Electron Transistor: Fabrication and Coulomb-Blockade

Byung T. Lee and Jung B. Choi

Abstract

We have fabricated a single-electron-tunneling(SET) transistor with a dual gate geometry based on the SOI structure prepared by SIMOX wafers. The split-gate is the lower-level gate and located ~100Å right above the inversion layer 2DEG active channel, which yields strong carrier confinement with fully controllable tunneling potential barrier. The transistor is operating at low temperatures and exhibits the single electron tunneling behavior through nano-size quantum dot. The Coulomb-blockade oscillation is demonstrated at 15 mK and its periodicity of 16.4 mV in the upper-gate voltage corresponds to the formation of quantum dots with a capacity of 9.7 aF. For non-linear transport regime, Coulomb-staircases are clearly observed up to four current steps in the range of 100 mV drain-source bias. The I-V characteristics near the zero-bias displays typical Coulomb-gap due to one-electron charging effect.

Ⅰ. Introduction

Rapidly advancing nanofabrication technology of the semiconductor industry makes it possible to laterally confine electrons to very small geometries with reduced dimensionality, which have proven to be remarkably rich experimental systems for the investigation of mesoscopic electrical transport[1, 2]. In particular, Coulomb-blockade(CB) and quantum effects, enhanced in such small scales, has been a subject of intensive studies with hopes for practical applications to future high density and low power memory devices. Various Si-based single electron tunneling(SET) device structures using CB effect have been proposed and experimentally demonstrated[3]. In particular, SET structures based on split-gates-control, conventinal type for GaAs single electron devices, have capability yielding strong carrier confinement with fully controllable electrostatic potential barriers. Even operating at low temperatures, this structure promises to be optimum for systematic investigation of the interplay between Coulomb-blockade and quantum effects which must play a critical role in operating the future Si-SET devices.

In this work, we newly applied the split-gated geometry to silicon-on-insulator(SOI) structures and fabricated SOI-SET transistors operating with double-layered gates. The CB oscillations were demonstrated for low temperatures and the Coulomb-staircases were observed up to four current steps. Similar device structures were found in the recent works of Hitachi and Cambridge groups [4, 5], but they are fabricted on bulk-silicon and basically different from ours in positioning the split-gates. In their dual-gate SET structures, the split-gate is the upper-level gate, and located considerably far from the 2DEG carriers. This has a critical drawback in fine-controlling the nano-size quantum dot(QD) by varying the split-gate electrostatic potential. In contrast, for our SET devices the split-gates is lower-level, just located ~100Å above the 2DEG carrier, and more fine and stronger carrier-confinement is possible. Although our dual-gate SET structure is operating at low temperature, when further developed in combination with the oxidation technique, it promises to be optimun geometry directed to future high-temperature operating and fully controllable SET devices.

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Ⅱ. Experiment

The SOI films prepared by SIMOX wafers(p-type Si substate, 800Å-buried SiO2 and 1800Å-top Si) were used for the SET transistor. The transistor consists of double-layered gates as seen in Fig. 1. The lower poly-gate, multilple patterned, was fabricated by e-beam lithography with SAL601 negative resistor on the top-Si active channel which was formed by etching to a narrow wire of 0.4 μm-width widening into source and drain carrier reservoir. The upper layered-metal gate, positively biased, induces an inversion 2DEG layer beneath the gate oxide of 200Å-thickness. Quantum dots(QD) for SET operation are formed in the active channel by negatively biasing poly-lower gate. Figure 2 shows a SEM picture of the core parts of the SET transistor; lower split-gates and the active transport channel. The main process flow for

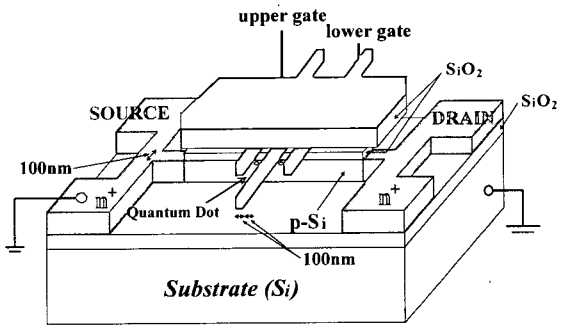

Fig. 1. A schematic drawing of the SOI-SET device structure with a dual gate.

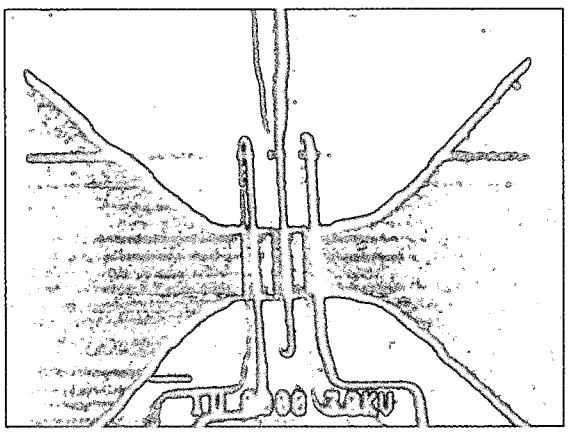

Fig. 2. SEM picture of the core part of the SOI-SET transistor: the lower split-gates and the Si active channel.

Table 1. The main process flow for the SOI-SET transistor fabrication.

Active photolithography & etching (Isolation and active define)	⇩
⇩	Gate E-Beam lithography
Gate oxidation	⇩
⇩	Inter oxide formation
Poly-Si deposition	⇩
⇩	Contact photolithography & etching
Gate photolithography & etching	⇩
⇩	Metal deposition
n^+ Source/Drain implantation	⇩
	Metal photolithography & etching

the SET device fabrication is summarized in Table 1.

Upper and lower gate characteristics were measured by HP 4145 B parameter analyzer at 300 K and 77 K. For Coulomb-blockade experiment the devices were Al wire-bonded and put in a dilution refrigerator with liquid helium at its base temperature down to 15 mK. The actual sample temperature is expected to be typically 100 mK due to RF-induced heating. The linear transport was measured at a fixed lower split gate and for drain-source bias

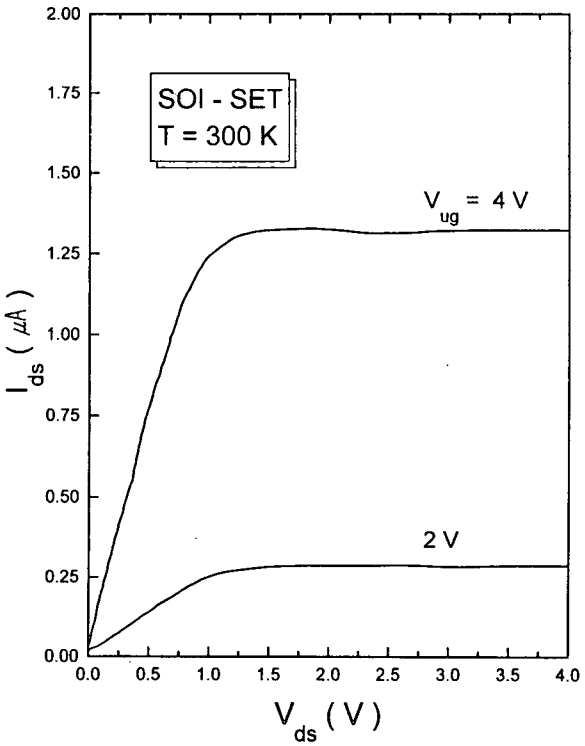

Fig. 3. The I-V characteristics for different values of the upper-gate voltage at 300K.

voltage under 1 mV, while the upper-gate voltage was scanned with a function generator. For nonlinear transport, I-V characteristics was measured at a fixed upper- and lower-gate voltages and for varying bias voltag up to 100 mV. A current amplifier was used to detect the weak and sensitive current peaks and a 10 MΩ road resistor was installed next to the sample inside the cryostat to reduce thermal noise.

III. Results and Discussion

Figure 3 shows the upper-gate characteristics of the SET transistor at 300 K. It displays a typical MOSFET I-V characteristics and confirm the formation of an inversion layer with the 2DEG carrier. The lower split-gate voltage dependence of drain-to-source current at 300 K is seen in Fig. 4. For various upper-gate voltages V_{ug}, I_{ds} rapidly decreases with increasing negative bias V_{lg}. This feature confirms the formation of electrostatic tunneling potential barrier below the lower split-gates, which induces the nano-size quantum dots and cuts off the channel current. I_{ds} vanishes at a cut-off voltage V_{lg} = -0.3 V for 300 K. It is noted that as device temperature decreases the cut-off voltage is found to shift to positive value direction. At 4.2 K the cut-off V_{lg} approaches 0.8 V. This indicates that the number of channel electrons rapidly decreases with temperature, and even under V_{lg} = 0 V, the lower-gate effectively screens the electrostatic field of the upper gate and makes isolated quantum dots.

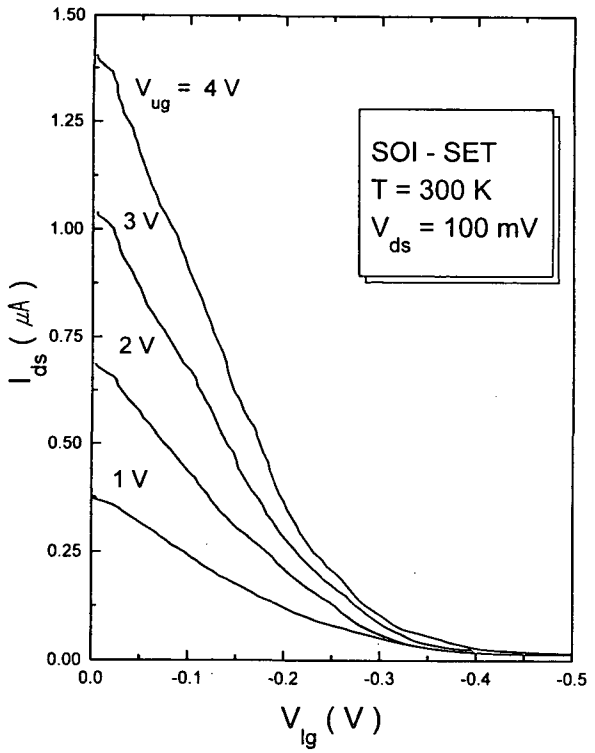

Fig. 4. Drain current vs lower-gate voltage for different values of the upper gate voltage at 300 K.

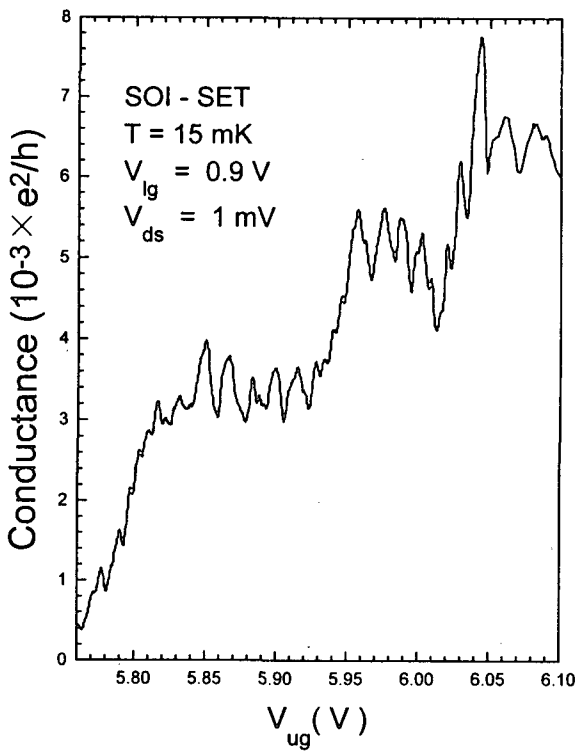

Fig. 5. Conductance(in unit of e^2/h) vs upper-gate voltage for a fixed lower-gate voltage and 1 mV bias at 15 mK. The period of Coulomb-blockade oscillation of 16.4 mV is deduced from the Fourier transform power spectrum and persists up to 2 K.

The CB oscillations and Coulomb-staircase were observed for low temperatures. Figure 5 shows the drain-source conductance vs upper gate voltage, V_{ug} for a fixed V_{lg} at 15 mK. The bias voltage V_{ds} is 1 mV which is far below Coulomb charging energy of single electron, typically order of 10 mV for 100 nm size QD. The drain current of 100 pA level is expressed by the conductance in unit of quantum conductance e^2/h. The conductance is order of $10\text{-}3\times e^2/h$, very far below the quantum conductance. This means that the quantum fluctuation is negligible, and transport occurs in the Coulomb-blockade regime. The current exhibits the CB oscillations and its period ΔV_{ug}, deduced from Fourier transform power spectrum, is found to be about 16.4 mV. This Coulomb oscillations are due to the single electron tunneling and persist up to 2 K. The periodicity of 16.4 mV corresponds to the voltage difference for adding one electron to the QD, and the capacitance between the upper-gate and QD is $e/\Delta V_{ug} \sim 9.7$ aF. This implies that the area of the QD is about 8500 nm^2 for $V_{lg} = 0.9$ V, and the electrostatic repulsion induces strong carrier-confinement in a much smaller region than the geometrical area(400×100 nm^2 defined by the split-gate structure).

The single electron tunneling through the QD is further demonstrated in the Coulomb-staircase observed in non-linear transport regime. Figure 6 displays dI/dV vs V_{ds} for a fixed values of V_{ug} = 6.2 V and V_{lg} = 0.2 V. CB effect is clearly observed via four current steps in the range of 100 mV bias. The step period corresponding to one electron tunneling is about 20 mV, same order of that of CB oscillation observed in the linear-transport regime. The current suppression, called Coulomb-gap. can be more clearly seen near the zero-bias voltage. Figure 7 shows I-V characteristics near the zero-bias for different lower split-gate voltages at 15 mK. The Coulomb-gap appears with decreasing V_{lg}, i. e., increasing tunneling potential barrier. For $V_{lg}g = 0.3$ V the extrapolated Coulomb-blockade threshold voltage is estimated to be 6 mV. Non-zero value of current below the CB threshold is considered to be a leakage arising from the quantum mechanical co-tunneling[6]: the simultaneous tunneling of different electrons across different barrier via virtual intermediate charged-states in the quantum dot. This co-tunneling current becomes dominant in the CB regime when the single-electron sequential tunneling is suppressed.

Ⅳ. Summary

We have fabricated a SET transistor with a dual gate geometry based on the SOI structure prepared by SIMOX wafers. The Coulomb-blockade oscillation was demonstrated at 15 mK and its periodicity of 16.4 mV in the upper-gate voltage corresponds to the formation of quantum dots with a capacity of 9.7 aF. For non-linear transport measurement, Coulomb-staircases were clearly

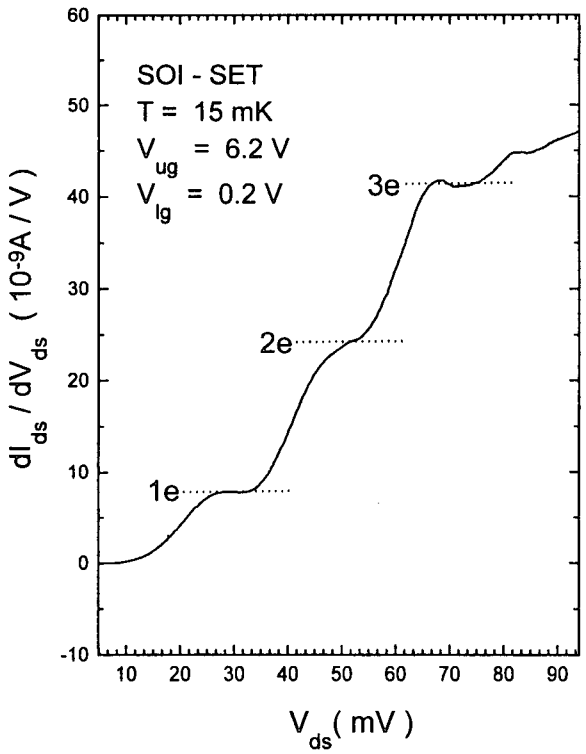

Fig. 6. First derivative of drain current vs bias voltage for a fixed upper- and -lower gate voltages at 15 mK. The Coulomb-staircases are observed up to four current steps.

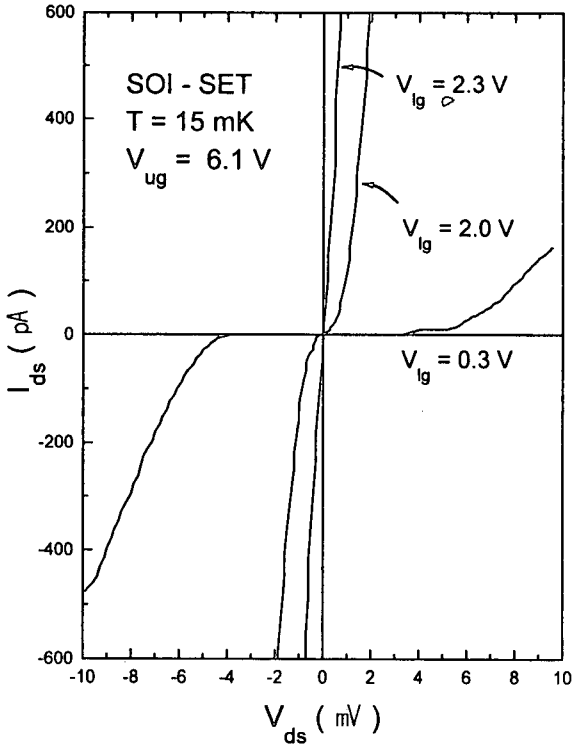

Fig. 7. I-V characteristics near zero-bias for different values of the lower-gate voltage at 15 mK. Coulomb-gap appears with decreasing lower-gate voltage.

observed up to four current steps in the range of 100 mV drain-source bias. The I-V characteristics near the zero-bias displays typical Coulomb-gap due to one electron charging effect.

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