Effects of Offset Gate on Programming Characteristics of Triple Polysilicon Flash EEPROM Cell

Nam-Soo Kim, Yeon-Wook Choe, and Yeong-Seuk Kim

Abstract

Electrical Characteristics of split-gate flash EEPROM with triple polysilicon is investigated in terms of effects of floating gate and offset gate. In order to search for the effects of offset gate on programming characteristics, threshold voltage and drain current are studied with variation of control gate voltage. The programming process is believed to depend on vertical and horizontal electric field as well as offset gate length. The erase and program threshold voltage are found to be almost constant with variation of control gate voltage above 12V, while endurance test indicates degradation of program threshold voltage. With increase of offset gate length, program threshold voltage becomes smaller and the drain source voltage just after program under constant control gate voltage becomes higher.

I. Introduction

Flash EEPROM is a nonvolatile memory device whose data is stored in the floating gate. Various studies have been done with regard to the structure of the memory cells. Two typical structures[1-3] are stack-gate and split-gate flash EEPROMs. In this work, we used the split-gate flash memory device which is composed of control gate, floating gate and erase gate. This device is erased by application of high voltage to the erase gate, thus the stored charge in floating gate is emitted. But more work is required for the optimum structure of cell and operation condition. In case of the stack-gate structure, the program and erase cycles can cause the carrier trap in gate oxide and both program and erase threshold voltages can be deteriorated. On the other hand, the erase operation in the split-gate structure is occurred between the floating gate and the erase gate. Therefore, the endurance characteristics of the split-gate device is superior to those of stack-gate structure.

Compared to MOSFET device, EEPROM cell has one more gate, floating gate for programming. The floating gate can often have overerase state which is opposite-charge programming. Application of offset gate in EEPROM is effective way to reduce the overerase state. The programming and cell current characteristics due to the offset gate of triple-poly EEPROM are well studied[4] in terms of the length of floating gate in channel. Another study to be able to reduce the overerase state can be the speculation on channel current with application of vertical or horizontal electric field. The effects of horizontal electric field between drain and source on electrical characteristics do not get much attention as there are almost same with MOSFET. On the other hand, vertical electric field can have many variations on current and programming characteristics, as this device has the offset gate above the channel. In this work, we focused on the channel current due to the control gate voltage and the offset gate which is rarely done by others. As floating gate does not fill out the channel length of EEPROM cell, the electric field between control gate and channel is not uniform, thereby, programming characteristics is difficult to forecast and can be significantly dependent on where the offset gate is located in the channel and, also, the reliability in terms of programming and erase threshold voltage can be influenced by the length of offset gate.

II. Device Structure and Experiment

This device is composed of triple polysilicons, which are polysilicon 1 for floating gate, polysilicon 2 for control gate and polysilicon 3 for erase gate. Electrical characteristics is done by HP 4155 semiconductor parameter analyzer. The erase operation of this triple polysilicon flash EEPROM is done by Fowler-Nordheim tunneling current from floating gate to erase gate, while charge input in floating gate by channel hot electron is the program status.

The cell structure and its equivalent circuit are shown in Fig. 1. In Fig. 1(b), L and L_1 are source-drain channel length and offset gate length, respectively. The thickness of polysilicon and oxide

Manuscript received March 20, 1997; accepted May 26, 1997.

N. S. Kim and Y. S. Kim are with Dept. of Electrical and Electronics engineering Chungbuk National University.

Y. W. Choe is with Dept. of Control and Instrumentation Bukyong National University.

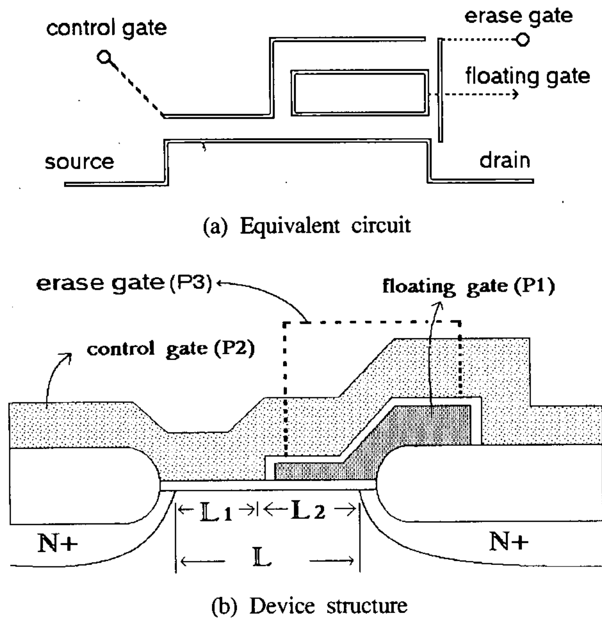


Fig. 1. (a) Equivalent circuit. (b) Structure of split-gate flash memory cell.

between ploysilicons are 3000-3500Å and 300-400Å, respectively. The channel length and width in this device are 1.3μm and 2μm. Polysilicon 1 is for preserving charge for data programming, polysilicon 2 for inducing carrier in channel and polysilicon 3 for erasing the charge in polysilicon 1. The offset gate is for reducing over-erase charge in floating gate.

III. Results

In this work, programming characteristics due to the offset gate under constant channel length is analyzed in terms of program and erase threshold voltages and channel current by application of vertical and horizontal electric field.

Fig. 2 shows drain current with variation of control gate voltage under 0.8μm offset gate length. The program and erase threshold voltages are obtained just under the maximum conductances. The higher program threshold voltage, compared to erase one, can be explained that the charges in floating gate after programming induces holes in channel, thereby, more vertical field is necessary to induce same number of electrons. The read operation can be done by checking out the threshold voltage. The "1" is at the state of higher threshold voltage and the "0" is the opposite case.

The cell-endurance characteristics as shown in Fig. 3 explains that, up to 10^4 cycle time, erase threshold voltage shows almost constant despite large decrease in program threshold voltage. The decreasing program threshold voltage which begins at about 500 cycle seems to be generated from charge trap in oxide. The charge trap near the edge of floating gate is considered to prevent

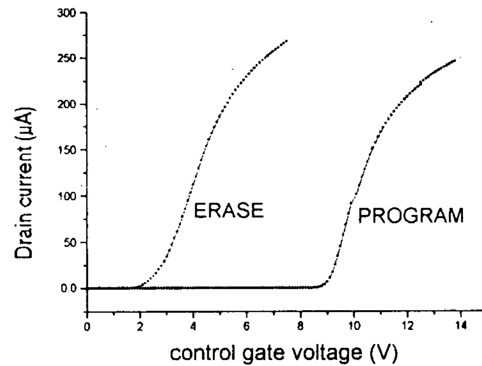


Fig. 2. Characteristics of drain current at constant drain-source voltage of 7V.

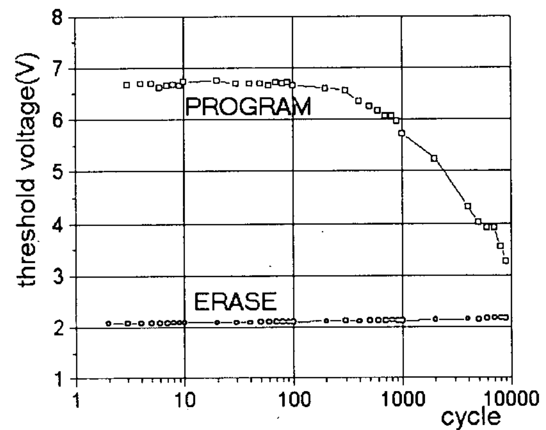


Fig. 3. Charateristics of cell-endurance at constant offset gate length.

the migration of hot electrons to the floating gate. Stack-gate EEPROM usually has the endurance characteristics that both erase and program threshold voltage show window-closing[5] after long cycle which comes from gate oxide degradation. As triple poly flash EEPROM has independent erase gate, erase threshold voltage can be constant, even though large decrease in program threshold voltage occurs after long cycle. In the test of erase characteristics of triple poly EEPROM, the phenomenon of time dependent dielectric breakdown(TDDB) or data retention between floating gate and erase gate seems to be more important rather than that of erase threshold voltage.

Fig. 4 shows the program threshold voltage with variation of control gate voltage. Each threshold voltage is obtained after increase of horizontal voltage Vds up to 10V under constant control gate voltage. It indicates that program threshold voltage increases a little. It also shows the phenomenon of Fig. 2 which is program threshold voltage is almost four times higher than erase one. Small increase of program threshold voltage with higher control gate voltage seems to be generated from charge trap in oxide between drain and floating gate or variation of charge-quantity in floating gate. Rapid increase of program threshold voltage at 12V control gate voltage means that there

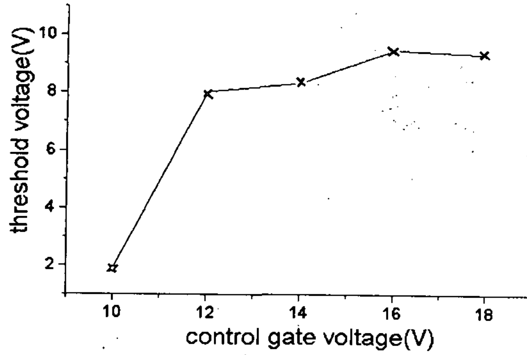


Fig. 4. Program threshold voltage with change of control-gate voltage at constant offset gate length of 0.8㎛. (Erase $V_T \cong 2V$)

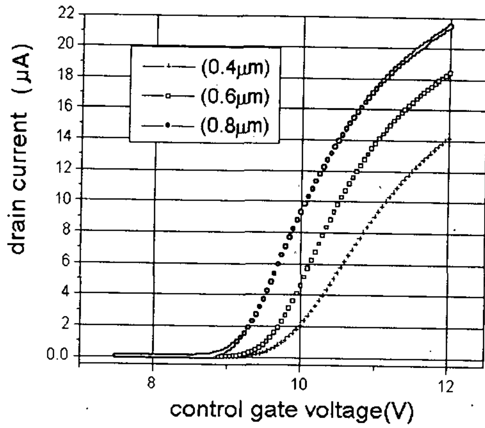


Fig. 5. Characteristics of threshold current after programming with various offset gate length.

isn't programming in floating gate under 10V control gate voltage and the lower vertical field isn't enough to induce carriers in channel to get a hot carrier effect.

Up to now, we have seen the electrical characteristics in terms of threshold voltage with the variation of control gate voltage. When offset gate triple-poly EEPROM is compared with stack-gate EEPROM cell in terms of program threshold voltage, the effect of offset gate is shown in Fig. 5 that program threshold voltage becomes higher with shorter offset gate length and program threshold voltage of stack-gate cell will be larger than that of offset gate cell. It is supposed that the charge in floating gate of offset gate EEPROM cell after programming induces smaller number of holes in channel with higher offset gate length. When program threshold voltage is considered in Fig. 1(b), device structure, it can be

$$V_{tp} = V_{te} + \Delta V_t, \quad \Delta V_t = \frac{Q_{fg}}{C_{cf}} \tag{1}$$

where Vtp, Vte, Qfg and Ccf are program threshold voltage, erase threshold voltage, charge in floating gate and capacitance between control gate and floating gate, respectively. When offset gate length L_1 becomes smaller under constant channel length, the current to floating gate becomes larger and it makes Qfg larger. The above equation shows that the program threshold voltage becomes larger with decrease of offset gate length.

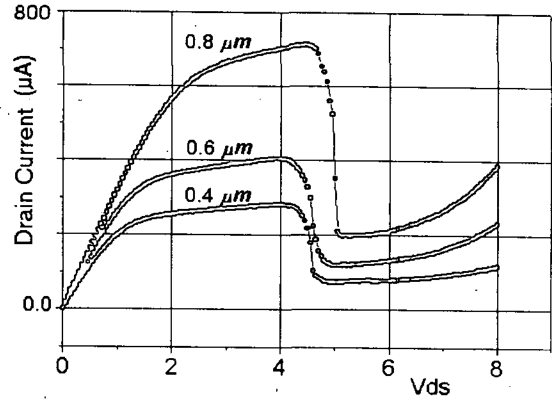


Fig. 6. Characteristics of Id-Vds curve with change of offset gate length at constant control-gate voltage of 12V and drain voltage 7V.

Fig. 6 shows the drain current characteristics with variation of horizontal voltage Vds and offset gate length. The characteristics of current vs. Vds at constant offset gate length indicates there are four regions which are linear, saturating, sudden-decreasing, and constant one. The general trend of this graph shows two things. One is that current increases with higher offset gate length, the other is the Vds at the instant of current-drop is also increasing with higher offset gate length. Refering to C. Sodini et al.[6], the saturating Vds, Vdsat, can be expressed as

$$V_{dsat} = \frac{(V_{cg} - V_t)LE_{sat}}{(V_{cg} - V_t + LE_{sat})} \tag{2}$$

where Vt is the threshold voltage, L is the effective channel length and Esat is a constant value which is the critical field for velocity saturation. This equation can be modified to

$$\frac{1}{V_{dsat}} = \frac{C_1}{L} + \frac{1}{C_2 - V_t} \tag{3}$$

where C_1 and C_2 are constant and C_2 is larger than Vt. After programming state, the induced holes in channel under floating gate can act as enlarged drain, thereby, offset gate length is considered as an effective channel length. As already shown in Fig. 5, Vt becomes smaller with increase of offset gate length. The equation(3) clearly indicates that, with higher offset gate length, Vdsat becomes larger as the second term in equation(3) decreases.

Ⅳ. Conclusion

Programming characteristics of triple polisilicon split gate flash EEPROM cell is studied with variation of offset gate length and control gate voltage. The programming process in terms of hot carrier effects is explained with the dependence of offset gate length on saturating drain source voltage. With increase of offset gate length, program threshold voltage becomes lower. Endurance test shows degradation of program threshold voltage and constant erase threshold voltage. On the other hand, under change of control gate voltage, erase and program threshold voltages show almost constant. It indicates that control gate voltage under constant offset gate length doesn't change the threshold voltages, while offset gate length can affect drain current and program threshold voltage.

Acknowledgement

This work was supported by Korea Ministry of Education through Inter-University Semiconductor Research Center(ISRC 96-E-4009) and NON-DIRECTED RESEARCH FUND(96F-12), National Special Support Project of Chungbuk National University.

References

[1] F. Masuoka, "A 256-kbit Flash E^2PROM Using Triple-Polysilicon Technology", IEEE Joural of Solid-State Circuits, Vol. SC-22, No. 4, pp. 548-551, Aug. 1987.

[2] A. Kolodny, S. T. K. Nien, B. Eitan, and J. Shappir, "Analysis and Modeling of Floating-Gate EEPROM Cells", IEEE Transaction on Electron Device, Vol. ED-33, No. 6, pp. 128-137, Jun. 1986.

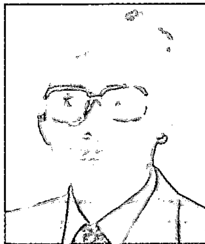
[3] V. N. Kynett, A. Baker, M. L. Fandrich, G. P. Hoekstra, O. Jungroth, J. A. Kreifels, S. Wells, and M. D. Winston, "An In-System Reprogrammable 32K×8 CMOS Flash Memory", IEEE Journal of Solid-State Circuits, Vol. 23, No. 5, pp. 170-175, Oct. 1988.

[4] 황현상, 박근형 저, 플래시 메모리 기술, 지성출판사, Korea, pp. 46-49, May. 1995.

[5] Y. S. Kim, Y. Okada, K. M. Chang, P. J. Tobin, B. Morton, H. Choe, M. Bowers, C. Kuo, D. Chrudimsky, S. A. Ajuria, and J. R. Yeargain, "Low-Defect-Density and High-Reliability FETMOS EEPROM's Fabricated Using Furnace N_2O Oxynitridation", IEEE Transaction on Electron Devices, Vol. 14, No. 7, pp. 342-344, Jul. 1993.

[6] C. Sodini, P. K. Ko, and J. L. Moll, "The effect of high fields on MOS device and circuit performance", IEEE Transaction on Electron Device, Vol. ED-31, pp. 1386-1393, 1984.

Nam-Soo Kim refers to Journal of Electrical Engineering and Information Science Vol. 1, No. 4, p. 107.



Yeon-Wook Choe was born in Pusan, Korea, in 1955. He received the B.S. and M.S. degrees in electronics engineering from Han-Yang University, Korea, in 1978 and 1980, respectively, and Ph.D. degree in control engineering from Kyoto University, Japan, in 1990. From 1996 to 1997 he was a visiting professor at the University of South Australia, Australia. Since 1990, he has been with the department of control & instrumentation at Pukyong National University, Korea. His current research interests are system modeling and robust control system design, device circuit analysis and design. He is a member of KITE, ICASE and SICE.

Yeong-Seuk Kim was born in Kyung-nam, Korea, in 1957. He received the B.S. and M.S. degrees in electronics from Seoul National University, Korea, in 1980 and 1982, respectively, and the Ph.D. degree in electrical engineering from the University of Florida, Gainesville, Florida in 1990. From 1982 to 1985, he was with the Central Research Laboratories of LG Electronics, Seoul, Korea, where he designed analog and digital IC's for consumer electronics. In 1990, he joined the Advanced Products Research and Development Laboratory of Motorola, Austin, Texas, where he worked on bipolar transistor modeling, CMOS and EEPROM technology development. Since 1993 he has been with Chung-Buk National University, Korea. Currently he is an associate professor in the School of Electrical and Electronics Engineering, Chung-Buk National University.