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V|비정질-V_2O_5|V 박막소자에서의 양자화된 컨덕턴스 상태로의 문턱 스위칭

(Threshold Switching into Conductance Quantized States in V|amorphous-V_2O_5|V Thin Film Devices)

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(Eui-Jung Yun)

요 약

이 논문은 새로운 형태의 낮은 전압 문턱 switch (LVTS)에 대하여 연구하였다. 많은 다른 타입의 전자적 문턱 switch들과는 구별되게, 이 LVTS는 전압에 의해 제어되고, 낮은전압(<1V)에서 발생하며, 메모리 현상을 내포하지 않고, bias하에서 장기간의 dynamical 안전성을 갖는다. 가장 중요하게 이 switch는 초기의 낮은 컨덕턴스 상태에서 연속적으로 양자화된 높은 컨덕턴스 상태로 스위칭이 된다. LVTS는 100개이상의 as-deposited된 V/비정질-V_2O_5/V 소자에서 발견되었다. 낮은 평균 문턱 전압(V_{LVT})은 218mV이고 (Standard deviation=24mV~kT/q, 여기서 T=300K), 소자의 면적 (x100)과 비정질 oxide 두께 (x10)와는 무관하게 일정하였다. 전자적 이동의 광범위한 연구는 V|비정질 V_2O_5 contact의 ~22Å 두께의 경계면에서 스위칭이 일어난다는 것을 결론적으로 보였다. V_{LVT}에서 초기의 낮은 컨덕턴스(OFF) 상태에서 연속적으로 양자화된 높은 컨덕턴스 상태(ON)로의 선이가 이루어졌다. OFF상태는 공간적으로 균질이있고 경계면으로의 tunneling에 의하여 지배되었다. ON상태의 컨덕턴스는 일차원적인 quantum point contact를 통한 ballistic transport의 양지화된 컨덕턴스와 일치하였다. V_{LVT}의 온도 의존성, 그리고 물질의 매계변수들 (dielectric 함수, barrier 에너지, 전도도)의 얻어진 data와의 적응 결과들은 OFF 상태에서 ON 상태로의 전이가 반도체이며 금속성의 VO_2의 성질을 갖는 경계면에서 일어난다는 것을 보였다. 실험적인 결과는 LVTS가 비탄성적인 에너지이전과 관련된 critical 사건에 의해서 경계면에서 발견되어진다고 제시하고 있다.

Abstract

This paper investigated a new type of low voltage threshold switch (LVTS). As distinguished from the many other types of electronic threshold switches, the LVTS is; voltage controlled, occurs at low voltages (<1V), involves no memory, and has long term dynamical stability under bias. Most importantly, it switches from an initially low conductance state into a succession of quantized states of higher conductance. The LVTS was observed in more than 100 as-deposited V|amorphous-V_2O_5|V devices. The average low threshold voltage $\langle V_{LVT}\rangle$=218 mV (standard deviation=24mV~kT/q, where T=300K), and was independent of the device area (x100) and amorphous oxide thickness (x10). Extensive studies of the electronic transport conclusively showed that switching occurred in an ~22Å thick interphase of the V|amorphous-V_2O_5 contacts. At V_{LVT} there was a transition from an initially low conductance (OFF) state into a succession of quantized states of higher conductance (ON). The OFF state was spatially homogeneous and dominated by tunneling into the interphase. The ON state conductances were consistent with the quantized conductances of ballistic transport through a one dimensional, quantum point contact. The temperature dependence of V_{LVT}, and fit of the material parameters (dielectric function, barrier energy, conductivity) to the data, showed that transport in the OFF and ON states occurred in an interphase with the characteristics of, respectively, semiçonducting and metallic VO_2. The experimental results suggest that the LVTS is likely to be observed in interphases produced by a critical event associated with an inelastic transfer of energy.

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I. Introduction

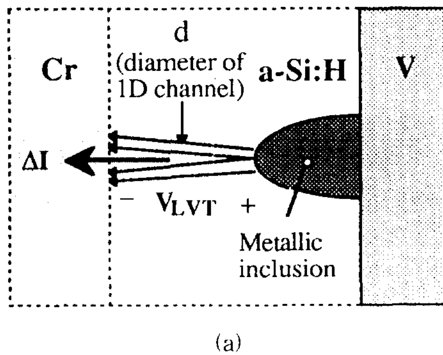
Low voltage threshold switching into quantized conductance states (LVTS) was first observed in studies conducted jointly by researchers at the University of Dundee and the University of Edinburgh in the U.K[1-6]. LVTS was initially observed at low temperatures (from 4.2 K to 190 K)[2, 3] and subsequently at room temperature[1, 4-7] in electroformed Cr|a-Si:H|V thin film sandwich devices. Recently, however, another LVTS was investigated at room temperature in as-prepared V|a-V_2O_5|V devices at U.T. Austin in U.S.A.[8]. These are the only occurrences of LVTS reported to date. Measurements of the current-voltage (I-V) characteristics revealed that, for $V>V_{LVT}$, the conductance of the LVTS devices was quantized in integer and half integer values of $(2e^2/h)=G_q=77.5\mu S$. Conductance quantization is unambiguous evidence of ballistic electron wave transmission in a one-dimensional constriction with lateral dimension W comparable to the Fermi wavelength λ_F. Quantization reflects the constraint imposed on the population of the one-dimensional (1D) subbands of the constriction when λ_F is an integer multiple of W. Since even in high mobility semiconductors at low temperatures $\lambda_F \leq 100$nm, prior to these experiments, state of the art nanolithography and cryogenic temperatures were required to observe one-dimensional conductance quantization (1DCQ) in GaAs-AlGaAs semiconductor heterostructures[9], metals[10], or Si-inversion layers[11, 12]. In the semiconductor experiments, electrons in a electrostatically constrained two-dimensional electron gas are forced to flow through a one dimensional nanoscale constriction in the surface potential established by the potential across nanolithographed electrodes.

Some features of the 1DCQ observed in the Cr|a-Si:H|V and V|a-V_2O_5|V devices are difficult to reconcile with the conventional physics of the phenomenon: (i) some quantum steps are skipped, (ii) half integer quantum steps are observed in the absence of an external magnetic field, and (iii) the subband splitting must be anomalously large to prevent the steps from being thermally smeared out at 300 K.

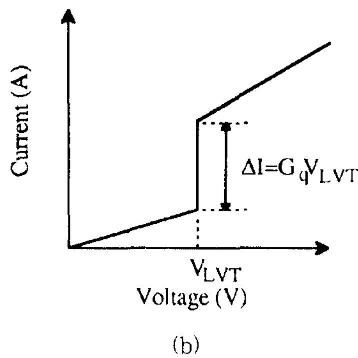
Since the LVTS observed in the Cr|a-Si:H|V was not observed prior to electroforming, it was assumed that IDCQ in Cr|a-Si:H|V devices resulted from electron transport through an electroformed one-dimensional constriction with $W \sim \lambda_F$. The maximum upper estimate for λ_F at 300 K in *any material* is ~10 nm. This reasoning, if valid, suggests that nanoscale structure, smaller than that producible by current state-of-the-art nanolithography was, either produced by the electroforming process, or formed by processes occurring at the threshold voltage in the LVTS. It is important to resolve this issue and determine *where* the 1D constrictions are formed in these structures, so that the process involved can be studied.

Independent of the physics, if the first conductance step of the LVTS in the Cr|a-Si:H|V LVTS device is attributed to electronic conduction through a single constriction, the I-V data indicates that an extremely large current density and power density would be localized in it. For example, the data shows a step in the current $\triangle I \approx 0.01$ mA at the low threshold voltage of $V_{LVT} \approx 0.55$ V (see Fig. 1). Assuming a diameter d=120Å[1], the current density and power density in a cylindrical constriction would be $\frac{\triangle I}{A} = \frac{10^{-5}}{\pi(60Å)^2} \approx 10^7 A/cm^2$ and $\frac{(\triangle I)V_{LVT}}{A} = \frac{5.5\times 10^{-6}}{\pi(60Å)^2} \approx 6\times 10^6 W/cm^2$, respectively. These values are at least an order of magnitude larger than, for example, the ~10^6 A/cm^2 critical current densities that cause electromigration failures in microcircuits[13], and the ~10^5 W/cm^2 output power densities of the most intense CW lasers[14]. These comparisons suggest that at the threshold in the

LVTS, a filamentary state somewhere in the thin film structure has either undergone, or is near a structural transformation.



(a)



(b)

그림 1. (a) 직경 d를 갖는 원통형의 1D 통로 (b) 전류흐름 △I와 전압 강하 V_{LVT}(LVTS에서, $V_{LVT} \leq 1V$)을 나타내는 첫 번째 step에서의 LVTS I-V 특성

Fig. 1. (a) A cylindrical 1D channel with diameter d and (b) LVTS I-V characteristic at the first step, showing the current flow △I and the voltage drop V_{LVT}(in the LVTS, $V_{LVT} \leq$ 1V).

Since electroforming processes in thin film structures produce structural rearrangements that are difficult to experimentally resolve, and since the LVTS is not observed in the Cr|a-Si:H|V devices without forming, it was considered inadvisable to experiment with these devices to determine the structure-property relationships involved in the LVTS. Assuming that the requirement for a low threshold voltage is that $V_{LVT} \leq 1$ volt, a review of the literature revealed no previous reports of a LVTS *into a higher conductance state* in any other device structure. These observations motivated the research objectives and focused the initial research on efforts to identify metal | amorphous-nonmetal contact systems in which the LVTS could be investigated without electroforming.

The primary problem addressed in this paper was to isolate and investigate the film structure-electrothermal property relationships associated with this unique LVTS phenomena.

Ⅱ. Experimental

The typical experimental devices used in this study were V|a-V_2O_5|V sandwich structures. The preparation, phase identification, and geometry of V|a-V_2O_5|V devices have been described elsewhere[8]. The thicknesses of a-V_2O_5 layer were varied from 5 to 250(±2) nm. One hundred identical devices with a junction area of 10^{-10} or $(10^{-8} \pm 4x10^{-12})$ m^2 were fabricated on a single substrate.

The current-voltage (I-V), first derivative-voltage (dV/dI-V), resistance-voltage (R-V), and conductance-voltage (G-V) characteristics of more than fifty identical as-prepared devices were measured at 300 K using microprobes and an HP4145B Semiconductor Parameter Analyzer in the voltage source mode. All measurements were made with the positive potential of a voltage ramp (either 0 to 0.5 V, or 0 to 1 V, at 0.08 V/sec, in 2mV steps) applied to the top V contact. The capacitances of devices were measured at 300 K and ac (from 5±0.1Hz to 1MHz±0.1 Hz) with a test signal level of (50±2.5)mV AC RMS using an HP4192A Low Frequency Impedance Analyzer with HP16047A test fixture. After connecting two pad metals of as-deposited V|a-V_2O_5|V devices to the outside silver wires using silver epoxy, the temperature dependence of the threshold voltage was measured in the temperature range 298-363 K using a digital temperature controller and an

HP4145B Semiconductor Parameter Analyzer in the voltage source mode. To eliminate local heating effects, the temperature was increased at a rate of 5 °C/min. The sample temperatures were measured to ± 2°C with a OMEGA K-type thermocouple (chromel-alumel) bonded to the sample surface with a ceramic bond.

The resistivity of the amorphous V_2O_5 films was measured by the four point probe technique using a constant DC current source and a digital multimeter. The sheet resistance was measured with a rectangular-shaped sample of finite size, and then corrected to eliminate edge effects [15]. The measured film thickness was used to obtain the sample resistivity from the sheet resistance.

Ⅲ. Results and Discussion

1. Interphase phenomenon

In this section, we first discuss briefly the observation of LVTS in a symmetric M|a-NM|M (M=metal, NM=nonmetal) sandwich structure consisting of V|a-V_2O_5|V layers (see ref [8] for the details). *Without prior electroforming*, current steps were observed at low voltage in the I-V characteristics of as-deposited devices. Substantially similar LVTS was observed for either polarity. Thus a ballistic point contact was formed in the non-metal|metal interphase either by a laterally unstable contact reaction during deposition, or by electronic injection at low bias voltage. *In the interphase region there is a transition from the composition and structure of the a-NM to that of the contact metal.*

Fig. 2 illustrates the I-V and R-V characteristics of a typical as-prepared V|a-V_2O_5|V device measured at 300 K during a single voltage sweep from 0 to 0.5 V with 2 mV step, showing the LVTS. The conductance-voltage (G-V) characteristic in Fig. 3, which is replotted using Fig 2, clearly shows seven discrete steps in the conductance. The abrupt increase at the first step (from V=0.218V to V=0.220V) appears to accompany the onset of 1D channel formation. The interphase conductance G_b is in parallel with the quantized conductance G_q of the ballistic channel switched on at threshold voltage $V=V_T$(=0.218V). G_q was obtained as the series of discontinuous conductance plateaus shown in Fig. 3 and assumed to occur at V_n for which the local derivative of G with V is more than ten times the average slope of the previous 5 data points. The parallel interphase conductance G_b was then obtained from ($G - G_q$). Figs. 2 and 3 are replotted from the Figs. 2 and 3 of the previous paper [8], respectively.

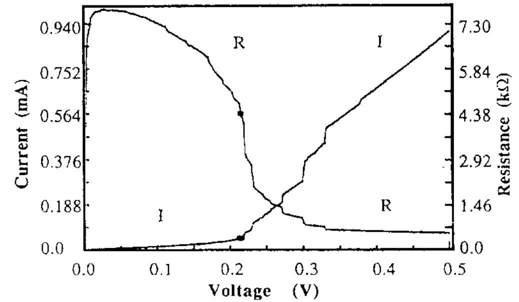


그림 2. 양자화된 ballistic 전자이동과 관련된 저항 step들을 나타내고 있는 as-prepared된 V|a-V_2O_5|V 소자의 300K에서의 I-V와 R-V 특성들

Fig. 2. I-V and R-V characteristics of an as-prepared V|a-V_2O_5|V device at 300K, showing resistance steps associated with quantized ballistic electron transport.

In order to show that the LVTS is an "interphase" phenomenon, we made electrical measurements to reveal "where" or "what" region of a device determines the I-V or capacitance-oxide thickness characteristics. With the parallel interphase conductance versus voltage (G_b-V) characteristic in Fig. 3, we fit the current vs voltage (I_b-V) characteristics with the calculated I-V obtained from the Simmons equations [16] for electron tunneling between metal electrodes separated by a thin insulating film using a rectangular barrier with image forces included.

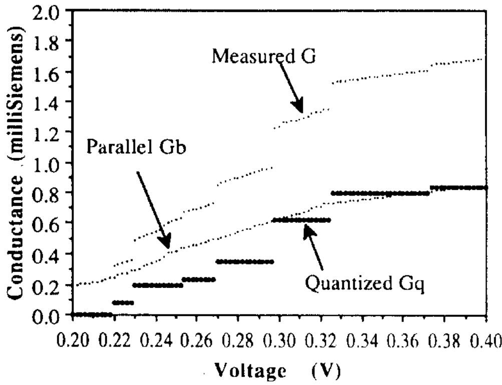


그림 3. 대표적인 V|a-V_2O_5|V 소자에 대한 G, G_b, 그리고 G_q-V 특성들. G, G_b, 그리고 G_q는 각각 측정된, 병렬 경계면, 그리고 양자화된 컨덕턴스들이다.

Fig. 3. G, G_b, and G_q versus V characteristics for a typical V|a-V_2O_5|V device. G, G_b, and G_q are the measured, parallel interphase, and quantized conductances, respectively.

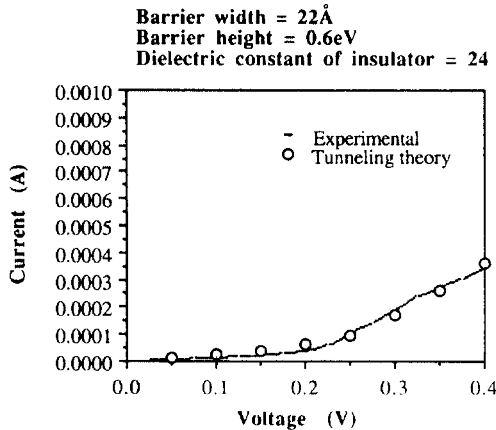


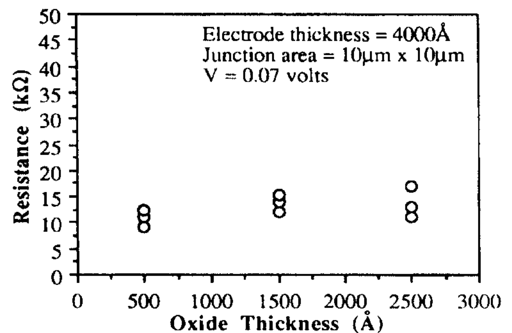
그림 4. 그림 3에 있는 G_b-V 특성으로부터 얻어진 실험적인 I-V 특성의 tunneling 이론으로부터 얻어진 이론적인 I-V 특성과의 Computer fitting "-" 기호는 실험적인 data를, "0" 기호는 이론적인 data를 나타낸다.

Fig. 4. Computer fitting of experimental I-V characteristics obtained from G_b-V characteristic in Fig. 3 to the theoretical I-V obtained from the tunneling theory. The "-" symbol refers to the experimental data and "O" open circle symbol shows the theoretical data.

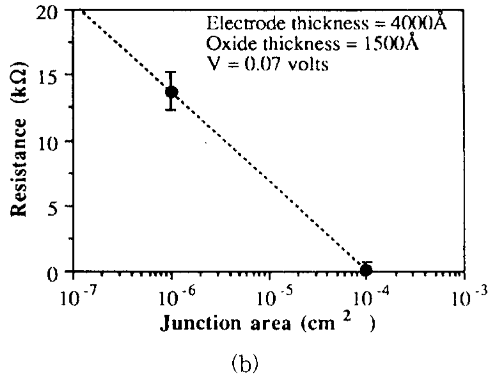
Fig. 4 shows the I_b-V characteristic obtained from G_b-V data in Fig. 3. The "-" symbol refers to the experimental data and the open circle symbol shows the theoretical data. Calculations of the theoretical data were performed until the test coefficient defined as [17]:

$$Test=\frac{\sum_i (I_{\exp}-I_{cal})^2}{\sum_i I_{\exp}^2} \qquad (1)$$

reaches a minimum. Good fits are obtained when $Test < 5\times10^{-3}$. The best fit to the experimental data ($Test = 4.5\times10^{-3}$) is obtained with the following parameters: barrier width (s) = 22Å, barrier height (φ_o) = 0.6 eV, and dielectric constant of the insulator (K) = 24. This observation supports the idea that tunneling occurs across a very thin interphase layer (22Å). Now we present the measured resistance R ≅ the tunneling interphase resistance R_b for $V<V_T$ to support above tunneling transport. Figs. 5 (a) and (b) show the resistance-oxide thickness (R-d) and resistance-junction area (R-A) characteristics of an as-prepared V|a-V_2O_5|V device measured at V = 0.07 volts, respectively. As shown in Fig. 5, the resistance near zero volt is independent of d and a function of 1/A, illustrating that there is a tunneling layer at the interphase. To confirm that the tunneling interphase resistance (R_b) ≈ measured resistance (R), the resistivities of a-V_2O_5 thin films were measured independently by the four-point probe technique [15] using a constant DC current source (I=0.2 mA) and a digital multimeter.



(a)

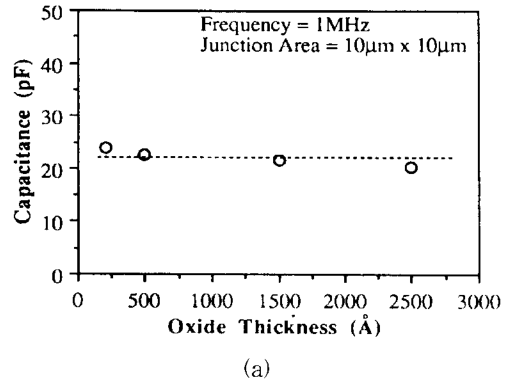


(b)

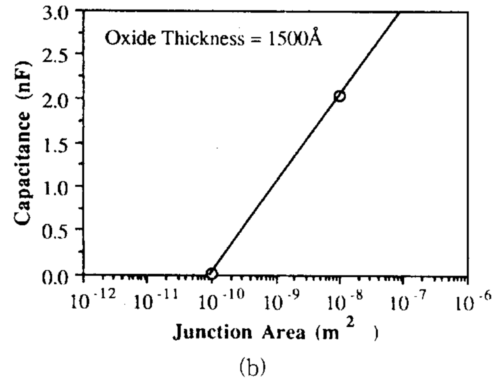
그림 5. 0 volt 근처에서의 저항이 d와 무관하며 1/A의 함수임을 나타내고 있는 V=0.07 volts에서 측정된 V|a-V_2O_5|V 소자의 (a) 저항-oxide 두께 (R-d), (b) 저항-접속면적(R-A)의 특성들. 각점들은 50 이상의 동일한 소자들의 저항값들을 평균하여 얻어졌다.

Fig. 5. (a) Resistance-oxide thickness (R-d) and (b) resistance-junction area (R-A) characteristics of an as-prepared V|a-V_2O_5|V device measured at V=0.07 volts, showing that the resistance near zero volt is independent of d and a function of 1/A. Each point was obtained averaging the resistance values of more than 50 identical devices.

The sheet resistance was measured with a rectangular-shaped a-V_2O_5 thin film (d=158 nm thick) on glass substrate of finite size (a=0.625", b=0.5625"). The measured average voltage was 6.69 mV. To eliminate edge effects [15], thickness (CF_t) and diameter (CF_d) correction factors were calculated using parameters b/s=14.0625 (s=probe spacing =0.04"), a/b=1.1 and were 1 and 4.36 [15], respectively. Using the relation R_s=(V/I)(CF_t)(CF_d), the calculated sheet resistance (R_s) was 146 Ω/square. The measured film thickness (d=158 nm) was used to obtain the sample resistivity (ρ=R_sd) from the sheet resistance. It was found that four-point probe resistivities of a-V_2O_5 were exceptionally low ($\approx 2.3\times10^{-3}$ Ωcm). For the device area = 10^{-6} cm^2, the resistances of a-V_2O_5 thin films were ~0.035 Ω, suggesting that the tunneling interphase resistance (R_b) ≈ measured resistance (R).



(a)



(b)

그림 6. C는 d에 무관하고 A의 함수임은 나타내고 있는 1MHz에서 측정된 V|a-V_2O_5|V 소자의 (a) 정전용량-oxide 두께 (C-d), (b) 정전용량-접속면적(C-A)의 특성들. 각점들은 50이상의 동일한 소자들의 정전용량값들을 평균하여 얻어졌다.

Fig. 6. (a) Capacitance-oxide thickness (C-d) and (b) capacitance-junction area (C-A) characteristics of an as-prepared V|a-V_2O_5|V device measured at 1MHz, showing that C is independent of d and a function of A. Each point was obtained averaging the capacitance values of more than 50 identical devices.

The capacitance-oxide thickness (C-d) characteristic (at 1MHz) of devices, with a junction area of ($10^{-10}\pm4\times10^{-12}$) m^2, is shown in Fig. 6 (a) where the independence of capacitance values on the a-V_2O_5 thickness is clearly observed. Each data point in Fig. 6 (a) was obtained by averaging the capacitance values of more than 50 identical devices. The value of the dielectric constant (ε_r) was computed from a plot of (A/C) vs d, making use of the equation [18]:

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} \quad (2)$$

where ε_r is the dielectric constant of the bulk oxide, A is the electrode area, and d is the oxide thickness. The estimated ε_r of 3.64×10^3 is not a realistic value since ε_r of a-V_2O_5 is 11.8 near 1MHz at 300 K[19]. The calculated interphase layer thickness using C = (22±0.013) pF, ε_r of semiconducting VO_2 = 24, and eq. (2) is 10Å. This result suggests that an interphase layer plays a dominant role in the capacitance measurements. This is similar to the results of Hebard et al.[18]. They have shown that an interphase layer makes a substantial contribution to the capacitance of thin-film Al|Al_2O_3|Al sandwich structures. The 10Å size is less than 76Å. Hajto et al.[5, 6] suggest that the dimensions of 1D channel should be less than 76Å to observe room temperature quantization. Fig. 6 (b) also shows the capacitance-junction area (C-A) characteristic (at 1MHz) of devices with a-V_2O_5 thickness of 1500Å, illustrating that the capacitance is a function of the junction area A. Here, we emphasize that the capacitance measurements were made both at dc and at ac with special care being taken to assure linearity by using voltage levels of 50mV or less, and the calibration was done using the known value of capacitors before the real capacitance measurements.

We can also rule out bulk phenomena using following the condition[3, 8]:

$$L < \mu \sqrt{\frac{m^* \cdot V}{e}} \quad (3)$$

where m^* is the effective mass, μ is the mobility, and L is the length of the ballistic channel. The channel length satisfying inequality (3) is bounded by requiring the ballistic carrier transit time to be less than the scattering time. It is unlikely that the channel is in the NM (non metal) film, since the mobility μ of a-V_2O_5 is less than 10^{-6} $m^2/V \cdot s$[17], and would require L<0.1nm for even a large effective mass of $m^* = 10^4 m_o$. In the absence of forming, the channel more likely lies in the L=1-10nm interphase of the as-deposited V|a-V_2O_5 contact, where ballistic carrier mobilities can be in the range 10^{-2}-10^{-3} $m^2/V \cdot s$. Based on above results we suggest that the threshold switching is an "interphase" phenomenon.

2. VO_2-like filament formation

Based on the result of Fig. 4 in section 1 we suggested that tunneling occurs across a very thin interphase layer (22Å) of dielectric constant of 24. Since the dielectric constant of a VO_2 thin film deposited by reactively sputtering vanadium in an atmosphere of argon and oxygen is 26 at 300 K[20] which is very close to 24, we suggest that the V|a-V_2O_5 interphase consists of VO_2-like layer.

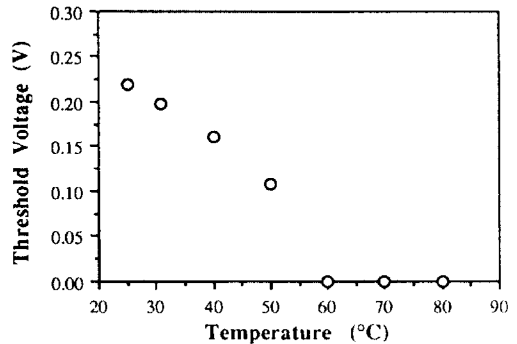


그림 7. 문턱전압(V_T)의 온도(T)에 대한 의존성. T가 증가함에따라 V_T는 감소하고 T≧60°C에 대하여 V_T=0

Fig. 7. The dependence of the threshold voltage (V_T) on temperature (T). V_T decreases as T increases and V_T=0 for T≧60°C.

To show that the 1DCQ is associated with the formation of conducting (metallic) VO_2-like filament in VO_2 interphase non-conducting layer, we demonstrate that the threshold phenomenon disappears near 60°C, which is close to the phase transition temperature for VO_2[21, 22]. Fig. 7 shows the dependence of the threshold voltage (V_T) on temperature (T), indicating that V_T

decreases as T increases and V_T = 0 for T≥60°C. Since V_T goes to zero near 60°C, it strongly suggests that there is a VO_2-like filament formation in the interphase, resulting in the 1DCQ. When T<60°C, metallic VO_2 filaments form in the interphase at $V \geq V_T$ and they form more easily as T increases, resulting in the decrease of the V_T. When T>60°C, however, the VO_2 filament in the interphase is always metallic at V≥0, resulting in V_T = 0. The VO_2-like filament formation was confirmed by showing that the length L of the ballistic channel in the interphase satisfies the inequality (3) "$L < \mu\sqrt{\frac{m^* \cdot V}{e}}$". Using σ_{mVO2} = conductivity of the metallic VO_2 = 370 $(\Omega cm)^{-1}$ [20], n = charge carrier density = 10^{20} cm^{-3}, $m^*=m_o$, and $V=V_T$=0.218 volts, we calculate $\mu(m^* \cdot V/e)^{1/2}$ $=(\sigma_{mVO2}/ne)(m^* \cdot V/e)^{1/2}$ ≈ 30Å. This 30Å value is greater than the L value (22Å), indicating that the length L of the ballistic channel satisfies the inequality "$L < \mu(m^* \cdot V/e)^{1/2}$". Since the ballistic carrier transit time is less than the scattering time, we suggest that data is compatible with 1DCQ phenomena.

Based on above results, we conclude that the 1DCQ is associated with the formation of conducting (metallic) VO_2-like filament in VO_2 interphase non-conducting layer.

3. Discussion of all possible LVTS switching mechanisms

To discuss all possible LVTS switching mechanisms, we examine all data related to threshold voltage. Fig. 8 shows that the mean threshold voltage corresponding to the first conductance step of more than 100 V|a-V_2O_5|V devices is determined to be V=218.6mV (standard deviation σ=24mV), illustrating that threshold voltage is highly characteristic. V_T is unusually low(218.6mV ~8kT/q where T=300 K) and has only a small (24mV ~kT/q where T=300 K) statistical variation device to device. It may be impossible to have this result if the formation of a ballistic point contact is driven by thermal excitations.

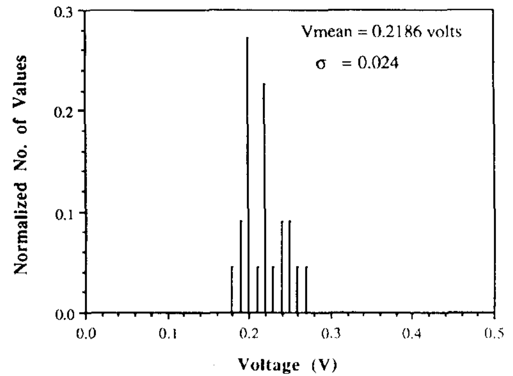
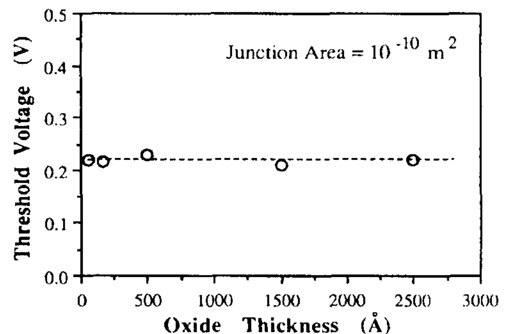


그림 8. 100개의 V|a-V_2O_5|V 소자들의 첫 번째 컨덕턴스 step에 대응하는 문턱 전압들의 중간값 (V_{mean}); V_{mean}=218.6mV, 표준편차=24mV

Fig. 8. The mean threshold voltage (V_{mean}) corresponding to the first conductance step of 100 V|a-V_2O_5|V devices; V_{mean}=218.6mV, standard deviation σ=24mV.

On the other hand, the threshold voltage is not a function of oxide thickness (Fig. 9 (a)), indicating that threshold switching is not due to high field effect. Each data point in Fig. 9 is an averaged value of 50 or more identical devices. Fig. 9 (b) shows that threshold voltage (V_T) is not a function of junction area. With amorphous oxide thickness (d) independence of R and device area (A) dependence of R (see Fig. 5), input power density (P_{in}) near threshold can be expressed as follows:



(a)

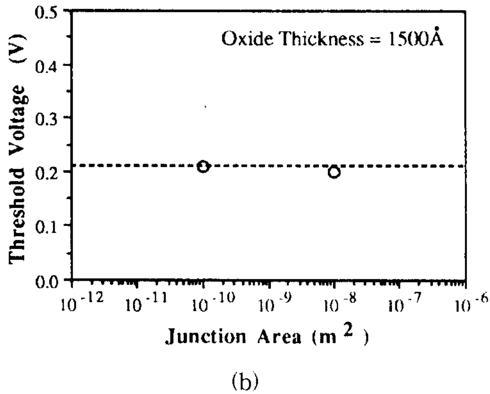


그림 9. V_T의 (a) a-V_2O_5 두께, (b) 접속면적들과의 함수관계. 각점들은 50이상의 동일한 소자들의 평균치이다.

Fig. 9. V_T as a function of (a) a-V_2O_5 thickness and (b) junction area. Each point is an averaged value of more than 50 identical devices.

$$P_{in}=\frac{V_T^2}{RAd}\neq f(A) \quad (4)$$

where f(A) means a function of A. Eg. (4) suggests that input power density (P_{in}) is not a function of A. Output power density (P_{out}) is not a function of A either. Therefore we can not rule out a possible interphase transition that could occur at a critical input power density.

However, Fig. 7 shows that V_T is observed to vanish as $(T-T_c)^n$ (n ~0.5) near T_c(critical temperature) ≈ 60°C. An analysis of the data suggests that the interphase transition at the voltage V_T, at which the LVTS was initiated, likely occurred by a critical event associated with an inelastic transfer of energy ~kT_c/q at the V|a-V_2O_5 interphase.

4. Equivalent Circuits

Based on the experimental results shown in previous Sections 1, 2, and 3, the equivalent circuit for $V \leq V_T$ (the region of OFF state in the LVTS) can be suggested as Fig. 10 (a) and experiment indicates that for $V \leq V_T$:

(1) the measured resistance R ≅ the interphase resistance R_b, (2) current flow through R_b is homogeneous, (3) V_T is the characteristic of interphase, (4) highly characteristic V_T suggests the electronic (not thermal) event, but the data do not rule out if the interphase transition occurred at critical electric field or critical input power density, and (5) in the OFF state, an interphase has the characteristics of semiconducting VO_2.

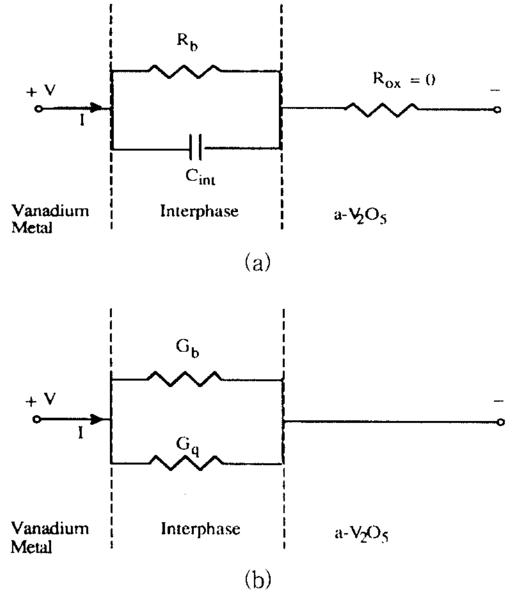


그림 10. (a) $V \leqq V_T$ 일 때, (b) $V > V_T$ 일때의 V|a-V_2O_5|V 소자에 대한 등가회로들. 여기서 $R_b >> R_{ox} \approx 0$, 그리고 G_b=1/R_b

Fig. 10. Equivalent circuits for a V|a-V_2O_5|V device (a) when $V \leqq V_T$ and (b) when $V > V_T$. Where $R_b >> R_{ox} \approx 0$ and G_b =1/R_b.

For $V>V_T$ (the region of ON state in the LVTS), the equivalent circuit is shown in Fig. 10 (b). The experimental results also indicate that for $V>V_T$:

(1) G (measured conductance) = G_b (interphase conductance) + G_q (quantized conductance), (2) current flow through G is inhomogeneous, (3) G_q results from the formation of 1D quantum point contact which contains metallic VO_2-like phase, (4) G_q is quantized as $(2e^2/h)(i + 1/2)$ where i is an integer or half integer, and (5) the nature of "ON" state is electronic (not thermal).

Therefore, above experimental result shows that in the V|a-V_2O_5|V devices the transitions

involve a new type of low voltage threshold switching from a spatially homogeneous OFF state to a spatially inhomogeneous ON state (a quantum ballistic point contact ON state). The temperature dependence of V_T, and fit of the material parameters (dielectric function, barrier energy, conductivity) to the data, showed that transport in the OFF and ON states occurred in an interphase with the characteristics of, respectively, semiconducting and metallic VO_2. The results also suggest that the LVTS is likely to be observed in interphases produced by contact reactions during the deposition of the devices and metastabilized in close proximity to a metal-nonmetal phase transition.

Ⅳ. Conclusions

In this paper the film structure-electrothermal property relationships associated with LVTS phenomena were isolated and investigated as follows:

(1) With electrical measurements to reveal that an interphase of device determines the I-V and capacitance-oxide thickness characteristics, and with unequivocal argument ruling out bulk phenomena, we concluded that the threshold switching is an "interphase" phenomenon. This was confirmed by measuring very low resistivity (ρ = 0.0023 Ωcm) of the bulk a-V_2O_5 with four-point probe measurement. The LVTS occurred in an ~22Å thick interphase of the V|a-V_2O_5 contacts.

(2) By showing that threshold phenomena disappear at ~60°C near the phase transition temperature for VO_2 and demonstrating that the length L of the ballistic channel satisfies the inequality "$L < \mu(m* \cdot V/e)^{1/2}$", we concluded that 1DCQ was associated with metallic VO_2-like 1D channel formation. We believe that this metallic VO_2-like channel formation is different from the conventional, irreversible formation of a joule-heating-induced filament of crystalline VO_2. Several possible experimental evidences for supporting this argument are that (i) the threshold voltage disappears at 60°C not the 68°C which is the exact phase transition temperature for crystalline VO_2, (ii) the formation of narrow channel is highly reversible, and (iii) the observation of 1DCQ.

(3) To discuss all possible interphase transition mechanisms, we showed that the as-deposited V|a-V_2O_5|V devices have a highly characteristic threshold voltage and demonstrated that the threshold voltage was not a function of amorphous oxide thickness or device junction area. These data suggest that the switching was reversible, however, were inconclusive to determine if the interphase transition occurred at a critical energy, critical field, or critical input power density.

Based on above experimental results, the equivalent circuits for $V \leq V_{LVT}$ (OFF state) and $V > V_{LVT}$ (ON state) were developed. At V_{LVT} there was a transition from an initially low conductance (OFF) state into a succession of quantized states of higher conductance (ON). The OFF state was spatially homogeneous and dominated by tunneling into the interphase with the characteristics of semiconducting VO_2. The ON state conductances were consistent with the quantized conductances of ballistic transport through a one dimensional, quantum point contact with the characteristic of metallic VO_2.

Several aspects of the observed 1DCQ phenomenon cannot be understood within the framework of the present theory, and room temperature 1DCQ is an extraordinary result. Furthermore, the data suggests that the transition was reversible, but were inconclusive to determine if the interphase transition occurred at a critical energy, critical electric field, or critical input power density (see Section 3). Therefore, additional research would be required to com-

pletely understand the physical mechanism of the LVTS in as-prepared V|a-V_2O_5|V thin film devices.

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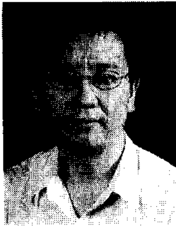

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