An Amorphous Silicon Local Interconnection (ASLI) CMOS with Self-Aligned Source/Drain and Its Electrical Characteristics

Yong-Sun Yoon, Kyu-Ha Baek, Jong-Moon Park, and Kee-Soo Nam

CONTENTS

ABSTRACT

A CMOS device which has an extended heavily-doped amorphous silicon source/drain layer on the field oxide and an amorphous silicon local interconnection (ASLI) layer in the self-aligned source/drain region has been studied. The ASLI layer has some important roles of the local interconnections from the extended source/drain to the bulk source/drain and the path of the dopant diffusion sources to the bulk. The junction depth and the area of the source/drain can be controlled easily by the ASLI layer thickness. The device in this paper not only has very small area of source/drain junctions, but has very shallow junction depths than those of the conventional ones. The electrical characteristics of this device are as good as those of the conventional CMOS device. An operating speed, however, is enhanced significantly compared with the conventional ones, because the junction capacitance of the source/drain is reduced remarkably due to the very small area of source/drain junctions. For a 71-stage unloaded CMOS ring oscillator, 128 ps/gate has been obtained at power supply voltage of 3.3 V. Utilizing this proposed structure, a buried channel PMOS device for the deep submicron regime, known to be difficult to implement, can be fabricated easily.

I. INTRODUCTION

CMOS device is the major part for integrated circuits over the past two decades with the high scalability of the device. There has been intensive research in scaling down CMOS devices in order to achieve high speed and packing density of CMOS circuits [1], [2]. As the device is scaled down, it is essential to implement a thin gate oxide, a heavily doped substrate, and a shallow source/drain junction. There have been numerous device structures reported in the literature to obtain the scaled down CMOS. An alteration of the structure in the gate was attempted to achieve the immunity of the short channel effect [3], [4]. In the case of source/drain structure, shallow junction formation is subject to CMOS fabrication technology. Several papers have reported the good results for shallow junction of the source/drain, such as elevated source/drain [5], [6], that of using rapid thermal process [7]-[9], and that of using solid phase diffusion from a PSG [10] and a BSG film [11]. However, there still exists an issue to reduce the source/drain junction capacitance caused by relatively large area of the source/drain in the conventional and the altered device structure, because the device scaling down results in the junction capacitance increasing. To reduce the junction capacitance in the source/drain, self-aligned counter doped well formation technique was attempted [12]. In recent years, the source/drain using amorphous silicon local interconnection (ASLI) layer has been suggested to achieve the shallow junction and small capacitance of the source/drain junction simultaneously [13].

In this paper, CMOS device using ASLI layer has been investigated by its electrical characteristics. To reduce the junction capacitance of the source/drain, the source/drain junction areas are significantly reduced by self-aligned source/drain scheme, and the very shallow source/drain junction depth is controlled by a doped amorphous silicon through the ASLI layer to the bulk. The ASLI layer has important roles in this device, and it is obtained very easily in the fabrication sequences. It makes the source/drain area in the bulk small significantly, and makes the source/drain area controllable very easily with its deposition thickness [13]. It is very useful for the shallow junction formation in both NMOS and PMOS source/drain region, simultaneously, because it is a path of the dopant diffusion sources from a doped amorphous silicon layer to the bulk. Shallow junction makes it possible to fabricate buried channel PMOS device in the deep submicron regime.

II. EXPERIMENTAL

The ASLI CMOS device has been fabricated with exchange of the sequences between the gate and the source/drain fabrication steps in the conventional 0.5 μm CMOS technology. The conventional LOCOS process was used for the isolation of

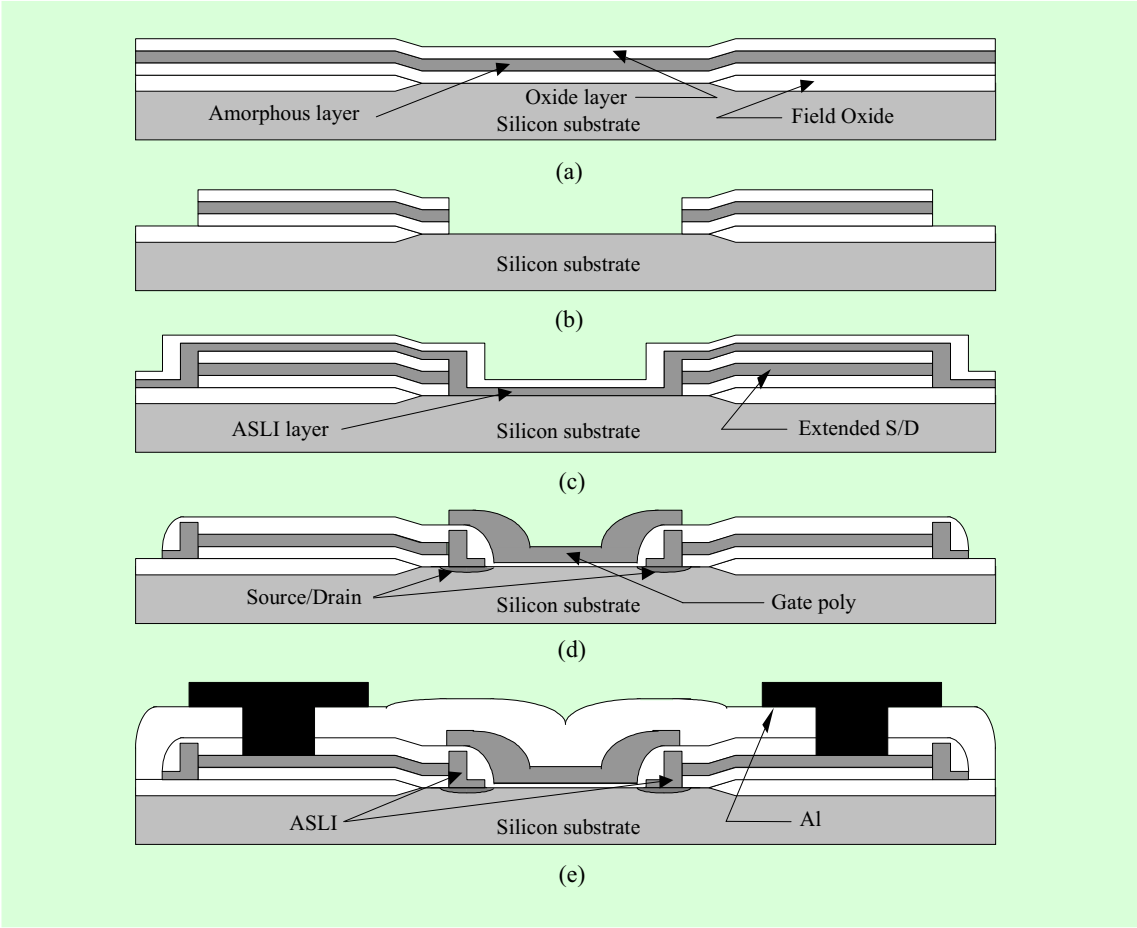

Fig. 15. Process steps for the CMOS device with self-aligned source/drain using ASLI layer: (a) thermal oxide/a-Si/oxide deposition; (b) self-aligned S/D lithography and oxide/a-Si/oxide layer etch; (c) ASLI/spacer oxide layer deposition; (d) oxide/ASLI layer etch, gate oxidation, gate poly-Si deposition and shallow source/drain junction formation; (e) contact open and metallization.

each NMOS and PMOS device. The process sequences until the end of LOCOS process were exactly same as those of the conventional CMOS process technology. The fabrication steps for the ASLI CMOS device are shown in Fig. 1. After the LOCOS process for a field oxidation, a thermal oxide in the thickness range of 1000 Å was grown and an amorphous silicon film was deposited successively in the thickness of 2000 Å. We have chosen the amorphous silicon rather than the polysilicon because the surface morphology of the amorphous silicon is known to be better than that of the polysilicon. In order to form the extended interconnection of the NMOS and PMOS source/drain, P and BF_2 implantations were carried out into the amorphous

silicon layer separately in the dose of 4×10^{15} cm^{-2}, and 3.7×10^{15} cm^{-2}, respectively. The implanted amorphous layers would also be dopant diffusion sources to form the small area of the source/drain and to form the shallow junctions of the source/drain in both NMOS and PMOS devices. An oxide layer deposition in the thickness range of 1000 Å was followed by the implantation processes as shown in Fig. 1(a). A photolithography with the source/drain photomask and the dry etch processes for the oxide/a-Si/oxide layer were carried out subsequently. The self-aligned source/drain was defined as shown in Fig. 1(b). A thermal oxidation at 850 °C, an implantation for threshold adjustments, and a wet etch process were performed sequentially. In order to form a local interconnection to the source/drain, the 1000 Å ASLI and an oxide layer in the thickness of 1000 Å, respectively, were deposited sequentially as shown in Fig. 1(c). The dry etch processes for the oxide and the ASLI layers were carried out successively. In these processes the local interconnections by the amorphous silicon layer and the side wall spacers by the oxide layer were formed. However, there would exist lots of damage by the implantation and the dry etch in the silicon surface. In order to remove the damage, a sacrificial oxide was grown and a wet etch process for the oxide was carried out successively. In these processes, almost all the damage would be removed. In addition, the self-aligned source/drain was partially formed by dopant diffusion through the ASLI to the bulk region during the oxidation process. In this oxidation step, the self-aligned source/drain was not formed completely because the diffusion path via ASLI layer was long enough to reach to the bulk. The complete self-aligned source/drain in this device would be formed completely in the next gate oxidation process. All the process sequences described above are different definitely from the conventional CMOS processes. In Fig. 1(d), the gate oxide was grown, the gate polysilicon was deposited and $POCl_3$ doping in the gate polysilicon at 875 °C was carried out successively. Polysilicon gate interconnection was formed by the conventional processes. Finally, the contact and the metallization processes were carried out in Fig. 1(e). From the gate oxidation to the end of metallization processes, all the process sequences are also the same as those of the conventional ones except only completion of the source/drain junction formation during gate oxidation step.

III. RESULTS AND DISCUSSIONS

We have fabricated CMOS device with self-aligned source/drain using amorphous silicon local interconnection layer, and have characterized its electrical properties. We have carried out process and device simulations by 2- dimensional simulator for both NMOS and PMOS devices. We have confirmed the suggested proper structure in the process simulations. The shallow junction

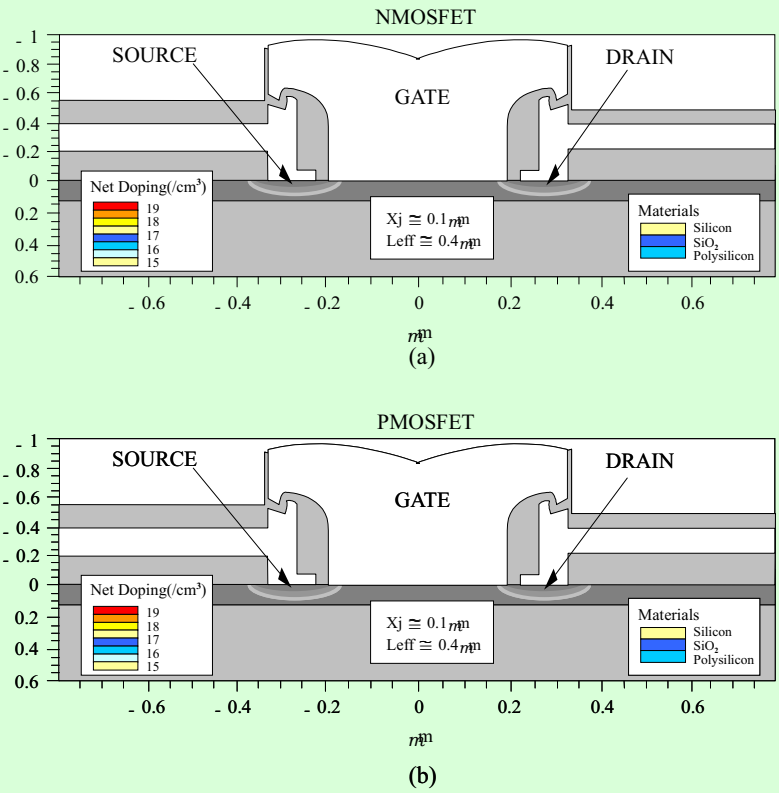

Fig. 16. Two-dimensional process simulation results: ASLI CMOS structures for (a) NMOS, (b) PMOS.

of the source/drain using not RTP but conventional furnace process could be formed easily in both NMOS and PMOS simultaneously, because the ASLI layer extends the dopants diffusion path of the source/drain to the bulk. The ASLI layer was long enough to control the junction depth of the source/drain in NMOS and PMOS. Small area of the source/drain in this structure could be also formed easily by the only ASLI layer thickness control.

1. Device structure

Figure 2 shows the process simulation results for both NMOS and PMOS devices. Simulations have been focused in the channel regions to determine the doping concentration and the junction depth of the source/drain. The junction depths in the simulation results are 0.08 μm for both NMOS and PMOS. These are remarkable results in the shallow junction formation in current CMOS technology [6], [7], [9], [11]. In addition, there are great advantages of

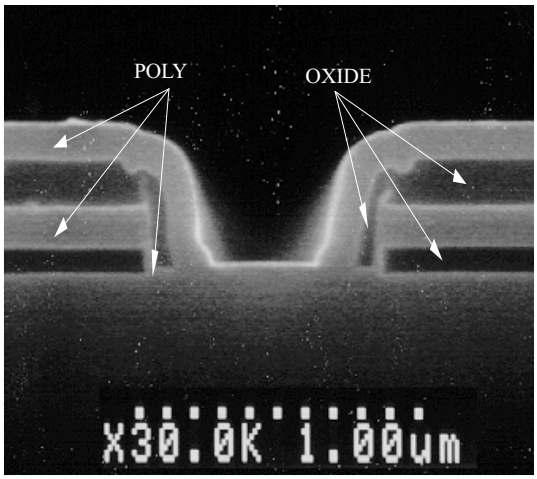

Fig. 17. A SEM photograph of self-align source/drain region with bottom oxide/a-Si/polysilicon layer in the thickness of 750/1000/1000 Å, respectively.

shallow junction depths of the source/drain in both NMOS and PMOS, especially for PMOS device compared with the conventional ones, because the high diffusivity of the boron in silicon makes it difficult to form the shallow junction in the conventional furnace process [11]. However, in this structure, it is very easy to form the shallow junction by the ASLI layer which is long enough for the dopants to reach to the bulk. Small area of the source/drain can be made easily also by ASLI layer thickness control. The area of the source/drain in this structure can be reduced at least 10 times compared with the conventional ones. This reduces the junction capacitance of the source/drain significantly.

Figure 3 shows a SEM photograph of the preliminary source/drain before complete fabrication of the ASLI CMOS device

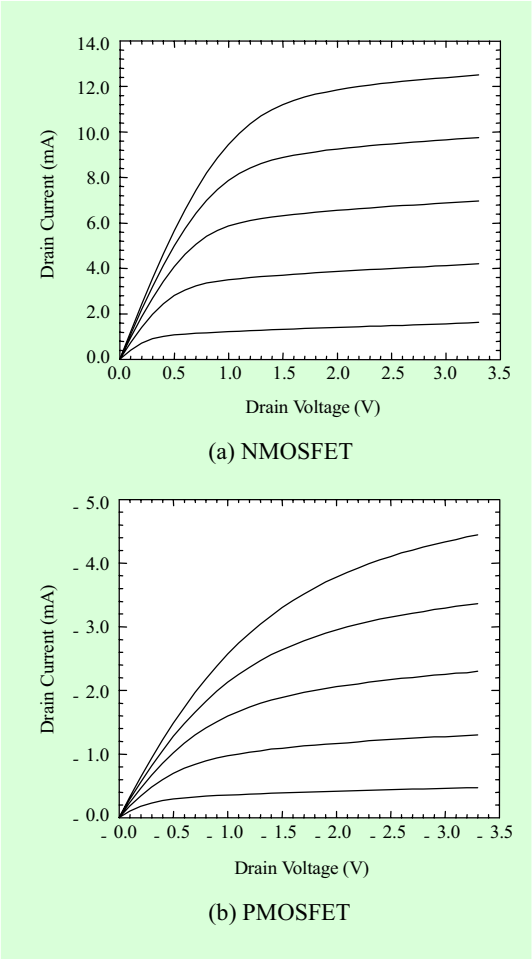

Fig. 18. Current-voltage characteristics of the ASLI CMOS for (a) NMOS, (b) PMOS.

structure. In this picture, the bottom oxide layer has a thickness range of 750 Å, the amorphous silicon layer of 1000 Å, and the top polysilicon layer thickness is 1000 Å. The top layer is a polysilicon layer, which was deposited intentionally in this case to clarify the contrast during SEM work. It is coincident with the CMOS structure in the source/drain as shown in Fig. 2.

Table 6. Electrical characteristics of the ASLI CMOS compared with the conventional CMOS.

	UNIT	Conventional CMOS		ASLI CMOS	
		NMOS	PMOS	NMOS	PMOS
Threshold Voltage	V	0.60	− 0.85	0.60 ± 0.01	−0.95 ± 0.01
Gate Oxide	Å	100	100	97	97
Subthreshold Slope	mV/dec	< 90	< 100	79.4 ± 0.04	−88.3 ± 1.26
Effective Channel Length	μm	0.45	0.45	0.46 ± 0.03	0.52 ± 0.04
Idsat(@3.3 V)	mA/μm	0.38	0.19	0.37 ± 0.02	0.14 ± 0.01
Breakdown Voltage(@Id = 10 nA)	V	> 8.0	< − 8.0	> 8.0	< − 8.0

2. Electrical Characteristics

Figure 4 shows the I-V characteristics of the ASLI CMOS device. Drain saturation currents in the channel width of 30 μm at $V_{DD} = 3.3$ V and $V_{GS} = 3.3$ V are 12.3 and 4.5 mA for NMOS and PMOS, respectively. These values are comparable in drain current characteristics with the conventional devices as shown in Table 1. Figure 5 shows the dependence of the threshold voltages on the effective channel lengths for NMOS and PMOS devices. The measurement conditions are drain voltage of 0.1 V and back bias voltage of 0 V for NMOS devices. For PMOS devices, the polarity of drain and back bias voltage is reversed. The threshold voltages for NMOS devices are rolled down near the effective channel length of 0.4 μm as shown in Fig. 5(a). These results are caused by short channel effect of the surface channel NMOS devices. For PMOS devices, however, the threshold voltage rolling down is suppressed at the same effective channel length and the threshold voltages are coincident within ± 0.05 V in all the range of the effective channel lengths as shown in Fig. 5(b). This suppression of rolling down shows a good characteristic compared with the conventional devices, and the characteristic is caused by shallow junctions of source/drain in the buried channel PMOS devices [14].

Figure 6 shows the subthreshold slopes with respect to the effective channel length for NMOS and PMOS devices. The subthreshold slope is one of the important characteristics of CMOS device and circuit. The average subthreshold slopes are 79.4, 88.3 mV/dec. for NMOS and PMOS, respectively. They are obtained at the drain voltage of 3.3 V with gate voltage variations of 0.05 volt steps. These are similar results

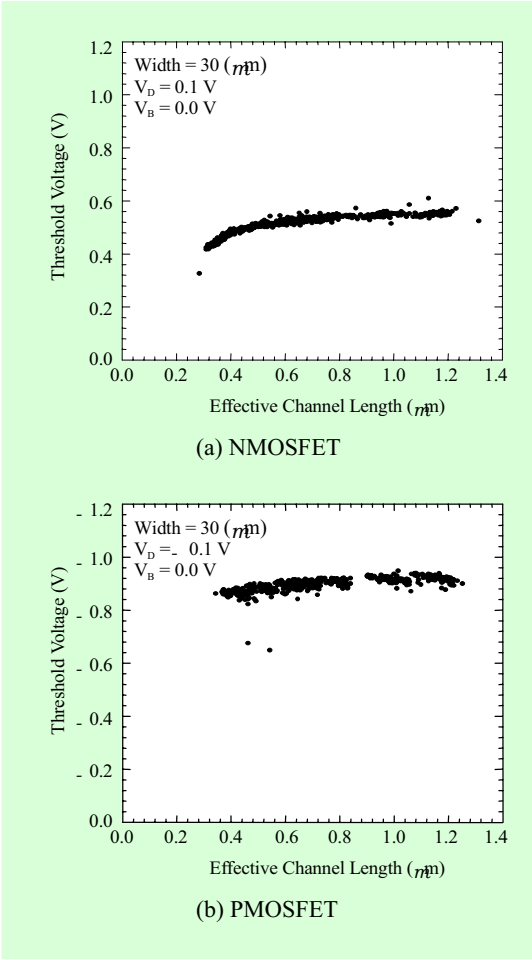

Fig. 19. The threshold voltage characteristics versus the effective channel length in the channel width of 30 μm: (a) for NMOSFET(V_D = 0.1, V_B = 0 V); (b) for PMOSFET(V_D = − 0.1, V_B = 0 V).

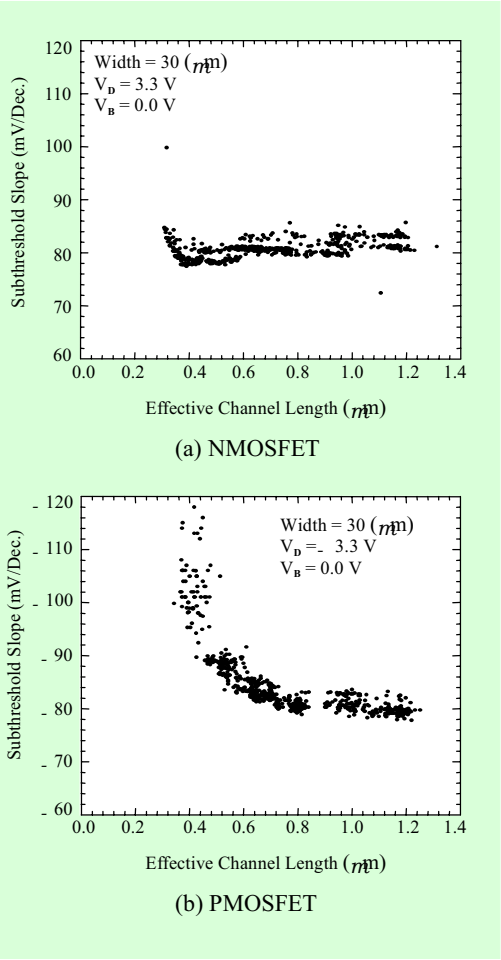

Fig. 20. The subthreshold slope characteristics versus the effective channel length in the channel width of 30 μm: (a) for NMOSFET, (b) for PMOSFET.

compared with the conventional CMOS devices for our case. For NMOS device subthreshold slope is almost constant in the effective channel length of 0.4 μm, however, it is increasing sharply near to the effective channel length of 0.35 μm. In the case of PMOS, however, it is increasing sharply near to the effective channel length of 0.5 μm. This is due to the increase of the bulk punchthrough effect in buried channel PMOS device [9].

Figure 7 shows the saturation drain current characteristics versus the effective channel length. The saturation drain current characteristic is reverse proportional to

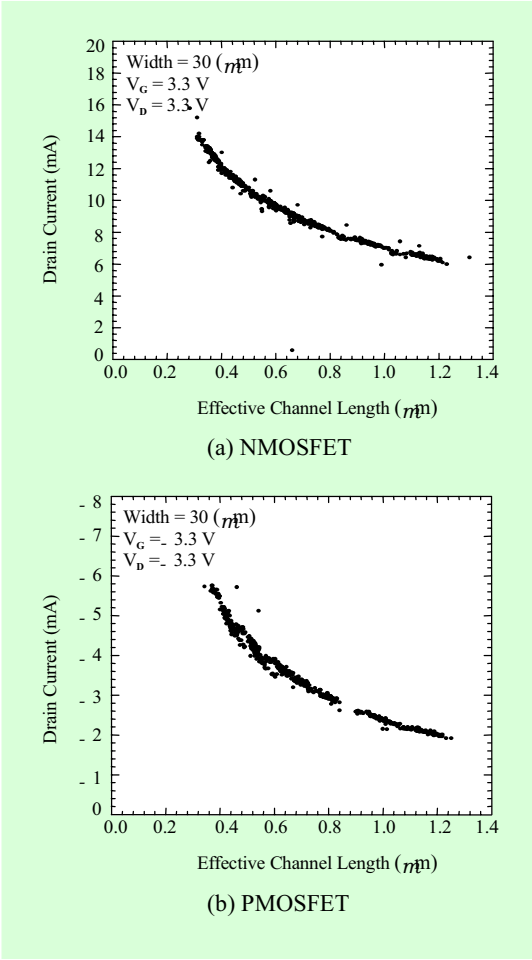

Fig. 21. The saturation drain currents versus the effective channel length in the channel width of 30 μm: (a) for NMOSFET, (b) for PMOSFET.

the effective channel lengths. The results are as good as this effect in both NMOS and PMOS devices. The measured saturation currents are 0.37, 0.14 mA/μm at the effective channel length of 0.45 μm for NMOS and PMOS device, respectively. The ratio of the saturation drain current between NMOS and PMOS device is 2.43 at drain and gate voltage of 3.3 volts. The all electrical characteristics described here are summarized in Table 1.

Figure 8 shows the CMOS ring oscillator characteristics of the new device. The gate delay of a 71-stage unloaded ring oscillator with the effective channel length of 0.45 μm is 128 ps/gate at power supply of 3.3 V. Figure 9 shows the CMOS ring oscillator characteristics of the new devices compared with the conventional ones in our cases. The gate delay with the effective channel length of 0.45 μm is represented by solid reverse triangle in Fig. 9. With an effective channel length of 0.65 μm, the gate delay of the new device is enhanced up to 35 %, compared to that of the conventional devices in the same effective channel length, which is represented by solid triangle in Fig. 9. These results are due to the remarkable reduction of the source/drain capacitance using ASLI layer, even if the resistance of the extended source/drain interconnection compared with conventional ones is increased. The structure of this device gives very shallow junction depths of less than 0.1 μm in both NMOS and PMOS devices, which are known to be difficult to implement in the conventional device technologies using ion implantation and furnace diffusion. With consideration of the shallow junctions and small capacitance of the source/drain, this structure is one of the most promising structures in deep submicron regime.

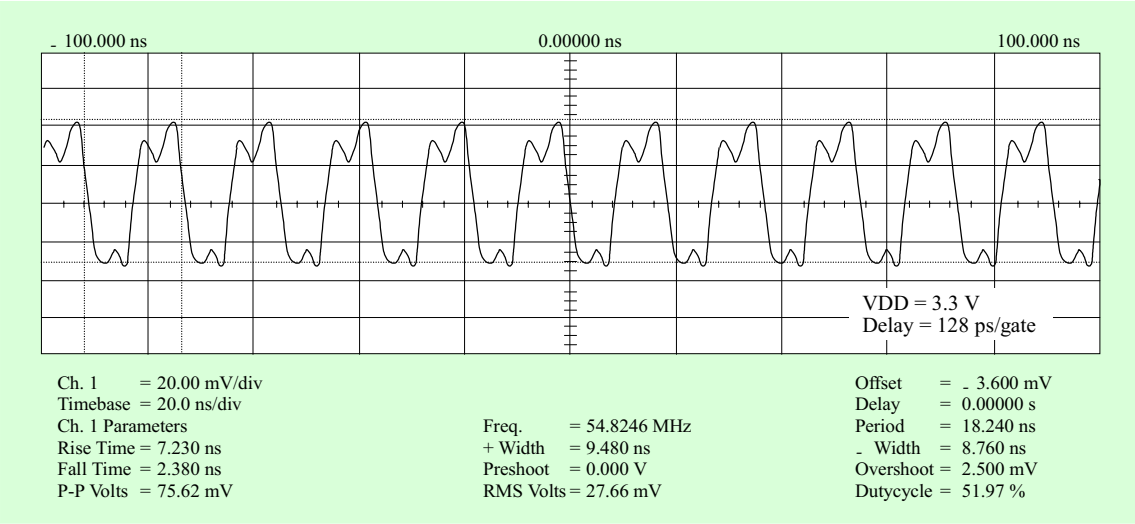

Fig. 22. 71-stage unloaded CMOS ring oscillator characteristic of the new devices. The gate delay of the new device is 128 ps/gate at power supply voltage of 3.3 V.

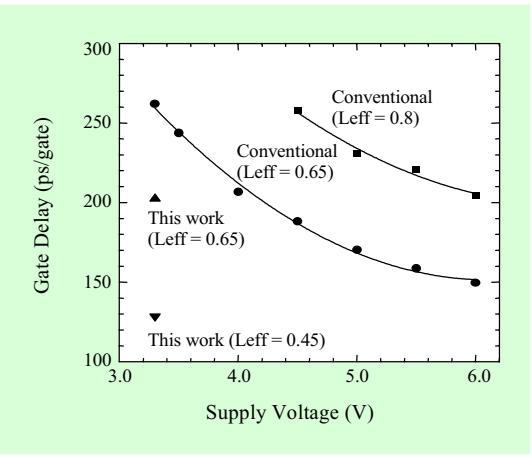

Fig. 23. 71-stage unloaded CMOS ring oscillator characteristics of the new devices and conventional ones. The solid circles and solid rectangles represent conventional ring oscillator characteristics with the effective channel length of 0.65, and 0.8 μm, respectively. The solid triangles and reverse triangles represent the new ones with the effective channel length of 0.65, and 0.45 μm, respectively.

IV. CONCLUSIONS

We have fabricated an ASLI CMOS device and investigated its electrical properties. The electrical properties are very close to the conventional CMOS devices, such as threshold voltages, saturation drain currents, subthreshold slopes, and breakdown voltage characteristics in both NMOS and PMOS devices. However, an operating speed characteristic is excellent compared with the conventional one due to the shallow junction and small area of source/drain in spite of the larger resistance of the extended source/drain interconnection. The gate delay of the 71 stage ring oscillator is 128 ps/gate. The ASLI layer makes it possible to control the junction depth of the NMOS and PMOS source/drain less than 0.1 μm in the conventional furnace process.

REFERENCES

[1] R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *J. Solid-State Circ.*, vol. SC-9, no. 5, pp. 256-268, 1974.

[2] W. H. Krautschneider, A. Kohlhase, and H. Terletzki, "Scaling down and reliability problems of gigabit CMOS circuits," *Microelectronics and Reliability*. vol. 37, pp. 19-37, 1977.

[3] S. Kimura, J. Tanaka, H. Noda, T. Toyabe, and S. Ihara, "Short channel effect suppressed sub-0.1-μm grooved-gate MOSFET's with W gate," *IEEE Electron Device Lett.*, vol. 42, pp. 94-100, Jan. 1995.

[4] P. H. Bricout, and E. Dubois, "Short-channel effect immunity and current capability of sub-0.1-micron MOSFET's using a recessed channel," *IEEE Trans. Electron Devices*, vol. 43, no. 8, pp. 1251-1285, Aug. 1996.

[5] S. Kimura, H. Noda, D. Hisamoto, and E. Takeda, "A 0.1 μm-gate elevated source and drain MOSFET fabricated by phase-shifted lithography," *Tech. Dig. IEEE Int'l Electron Devices Meeting*, pp. 950-952, 1991.

[6] H. Noda, F. Murai, and S. Kimura, "Threshold voltage controlled 0.1-μm MOSFET utilizing inversion layer as extreme shallow source/drain," *Tech. Dig. IEEE Int'l Electron Devices Meeting*, pp. 123-126, 1993.

[7] R. H. Yan, K. F. Lee, D. Y. Jeon, Y. O. Kim, B. G. Park, M. R. Pinto, C. S. Rafferty, D. M. Tennant, E. H. Westerwick, G. M. Chin, M. D. Morris, K. Early, P. Mulgrew, W. M. Mansfield, R. K. Watts, A. M. Vashchenkov, R.G. Swartz, and A. Ourmazd, "High performance 0.1-μm room temperature Si MOSFET's," *Symp. on VLSI Tech.*, pp. 86-87, 1992.

[8] R. A. Chapman, M. Rodder, M. M. Moslehi, L. Velo, J. W. Kuehne, and A. P. Lane, "The use of rapid thermal processing to improve performance of sub- half micron CMOS with and without salicide," *Symp. on VLSI Technology*, pp. 24 -28, 1993.

[9] A. Hori, H. Nakaoka, H. Umimoto, K. Yamashita, M. Takase, N. Shimizu, B. Mizuno, and S. Odanaka, "A 0.05 μm CMOS with ultra shallow source/drain junctions fabricated by 5 keV ion implantation and rapid thermal annealing," *Tech. Dig. IEEE Int'l Electron Device Meeting*, pp. 485 - 488, 1994.

[10] M. Ono, M. Saito, T. Yoshitomi, C. Fiegna, T. Ohguro, and H. Iwai, "Sub-50 nm gate length N-MOSFETS with 10 nm phosphorous source and drain junctions," *Tech. Dig. IEEE Int'l Electron Device Meeting*, pp. 119 - 122, 1993.

[11] M. Togo, T. Mogami, K. Uwasawa, and T. Kunio, "Novel deep sub-quarter micron PMOSFETs with ultra-shallow junctions utilizing boron diffusion from poly-Si/Oxide (BDSOX)," *Symp. on VLSI Tech.*, pp. 21 -22, 1994.

[12] H. Nakamura and T. Horiuchi, "A self-aligned counter-doped well process utilizing channel ion implantation," *IEEE Trans. Electron Devices*, vol. 43, no. 7, pp. 1099 - 1103, 1996.

[13] Y. S. Yoon, K. H. Baek, and K. S. Nam, "CMOS device with self-aligned source/drain using amorphous silicon local interconnection layer" *Electronics Lett.*, vol. 33, no. 5, pp. 389 - 390, 1997.

[14] M. Miyake, Y. Okazaki, and T. Kobayashi, "Characteristics of buried-channel pMOS devices with shallow counter-doped layers fabricated using channel preamorphization," *IEEE Trans. Electron Devices*, vol. 43, no. 3, pp. 444 - 449, 1996.

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