Development of the Base Station Transceiver Subsystem in the CDMA Mobile System

Dong-Wook Lee, Kisuk Yoo, Jin-Su Kim, Myoung Jin Kim, and Jae-Hong Park

CONTENTS

ABSTRACT

The base station transceiver subsystem (BTS) of the CDMA Mobile System is interfaced to mobile stations over the air and to the wired network through a packet switched interconnection network. The potential benefits of CDMA technology are achieved when the transmitter and the receiver are properly designed and implemented. The physical layer of the air interface at the base station is implemented with the CDMA ASICs and control circuits in the channel card of the BTS. We present the design perspectives and structural illustration of the BTS. Base station modem ASICs and their control to implement the CDMA receiver, baseband and RF signal processing blocks, and BTS controller are described. Elaborate power control is essential to ensure the high capacity which is one of advantages of the CDMA technology. The closed loop reverse link power control and the forward link power control operated in the BTS are described.

I. INTRODUCTION

The CDMA mobile system (CMS), a commercial prototype digital cellular system based on direct sequence/spread spectrum (DS/SS) CDMA technology, has been developed. The base station consists of base station transceiver subsystem (BTS), base station controller (BSC), and base station manager (BSM). BTS provides radio link to the mobile station (MS). In the forward link, BTS encodes and modulates the information data, then transmits the signal to the MS over the air. In the reverse link, it demodulates and decodes the received signal from the MS, then sends the recovered data to the wired network. The basic air interface follows TTA-62 [1], Korean standard on digital cellular, which is based on the IS-95, a North American digital cellular standard [2].

1. Design Requirements

General requirements for the design of CMS are summarized as follows:

i) Channel Structure
The forward and the reverse links employ convolutional coding, interleaving, pseudorandom-noise (PN) spreading, Walsh covering (or modulation), QPSK (or OQPSK) modulation as described in TTA-62 or IS-95.

ii) Services
As a basic service a variable rate voice service is accomplished using a dynamically variable data rate vocoder algorithm. The CDMA system must have the architecture which can support short message service, G3 fax or data services.

iii) Radio Link Capacity
The capacity must be greater than 10 times of AMPS capacity.

iv) Handoff
The system must support soft handoff when the mobile is in the boundary of two base station coverage, or sector coverage. The former is called (inter-cell) soft handoff, and the latter is called (intra-cell) softer handoff.

v) Sectored Cell
The base station should be able to be operable with up to 3 sectored cell configuration. The sectored cell can be implemented with direction antennas and is shown to give higher capacity.

vi) Power Control
The system must support the forward link and the reverse link power control.

vii) Redundancy
Failures of some modules may cause the entire shutdown of the base station. Critical modules must be duplicated, and the system should be able to detect failures.

viii) Expandability and Maintenance
The system should be able to support up to 10 frequency assignments (FAs).

2. Design Philosophy

The following aspects are considered for

the design of BTS.

i) Base Station Synchronization

Synchronization in CDMA system is very important in the sense that any chip interval discrepancy causes fatal effect to the operation of the entire system. To search a mobile station in the acquisition mode or in the handoff state, the base station must know the absolute time. Both base stations involved in the soft handoff must be synchronized with each other. For this reason every BTS is equipped with GPS receiver and clock generation unit.

ii) Frame Staggering

The system is given a delay budget to make a natural conversation possible. Since we design the base station with packet switched network and there are finite number of trunks between BTS and BSC, queuing delay is inevitable. To increase the trunk utilization with given delay budget, frame staggering is used. To support this functionality, BTS and BSC must be able to handle the staggered frame.

iii) Soft and Softer Handoffs

For the inter-cell soft handoff, the digital speech is transferred from the vocoder of the mobile to both base stations and from there to the BSC where the frame of better quality is selected prior to vocoding. On the other hand, in the intra-cell softer handoff case, combining occurs in the BTS because the CDMA ASICs may process signals from two sectors.

iv) Fault Management

The system is able to detect device fault and to report the status to the BSM. If a failure of duplicate device is detected, the standby module undertakes the role of the fault device. Faults are categorized into groups depending on severity, and alarm goes off for the critical faults.

v) Receiver Sensitivity

Sensitivity is a measure of how weak a signal can be and still be received satisfactorily. It is determined by information data rate, total interference, and required E_b/N_o. A total interference is a fuction of thermal noise, other user interference, and other cell interference. And the required E_b/N_o in the demodulator depends upon the channel condition. Even if the information data rate is fixed, a receiver sensitivity is decided by the required E_b/N_o in the consideration of total interference.

vi) High Power Amplifiers (HPA) Output Stability

A CDMA system is a noise limited system that should control the output power in the sense of reducing the output power by the minimum required level. Since the HPA is a non-linear system whose power gain is decreased by increasing, the input power, its power gain must be constant to maintain the required cell coverage. To satisfy this requirement, the input power of the HPA should be controlled by some techniques. We provide transmit power tracking loop around the HPA with a power detector having a temperature characteristic.

vii) Data Logging for Performance Evaluation

To evaluate the performance of the CDMA system, certain modules of BTS and BSC can log data for post-processing. Performance measures are frame error rate (FER), power control error variance, statistics of transmit and receive power, handoff statistics, etc. To measure the necessary statistics, finger energy, power control threshold, transmit digital gain, common air interface (CAI) message, and other data are logged.

3. Overall Architecture of BTS

The BTS is composed of RF unit, digital unit, BTS interconnection network (BIN), and BTS control processor (BCP). The RF unit converts the received UHF signal to IF signal which is down-converted to the baseband. The received baseband signal is converted into digital signal and demodulated in the digital unit. PN despreading, Viterbi decoding, demodulating and rake combining operations are performed in the channel card of the digital unit. For the forward link, digital unit encodes and modulates the information signal, then the signal is up-converted to the IF band. It is then sent to RF unit for up-conversion to UHF frequency band and transmitted to the mobile station. The BCP controls the operation of the BTS such as call processing and device initialization. It is responsible for the management of resources in the BTS such as frequency assignment, code channel, frame offset, and power allocation. The BIN is a packet router between BTS and BSC. Control and traffic packets are passed to the destination through the BIN. Figure 1 shows the block diagram of the BTS.

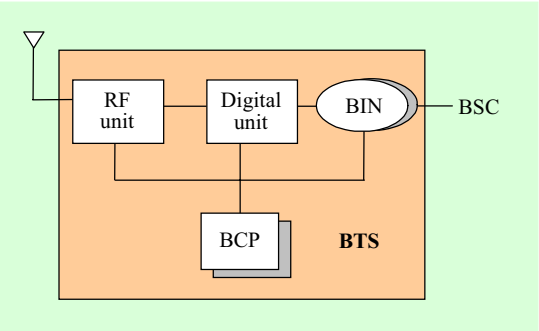

Fig. 1. Block diagram of the BTS.

II. CDMA MODEM ASIC AND RECEIVER DESIGN

1. Base Station Receiver

A. Base Station Demodulator Structure

On the reverse link, the information data is convolutionally encoded, block interleaved, modulated by the 64-ary orthogonal modulation, direct-sequence spread, and OQPSK modulated for transmission. At the base station, the demodulation is performed by finger in the CDMA channel card. The I and Q data is despread using two PN sequences, then accumulated over the Walsh chip period (which is equivalent to 4 PN chips). The I and Q fast Hadamard transform (FHT) is computed on the accumulated I and Q data by correlating the data with 64 possible Walsh sequences. The Walsh symbol that has the largest correlation

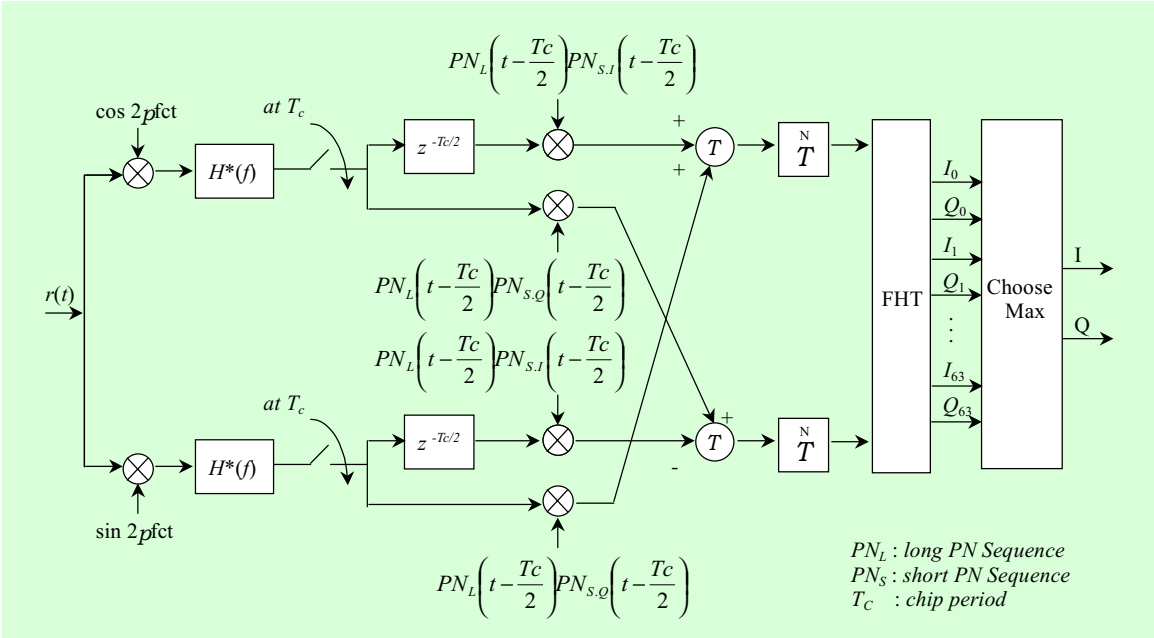

Fig. 2. Block diagram of the base station demodulator.

result is selected as the demodulated Walsh symbol. Before demodulation, the base station must acquire the mobile station through preamble searching. The DS/SS CDMA system works only when the chip timing of the receiver is synchronized to that of the transmitted signal. The code synchronization consists of two steps: code acquisition and code tracking which are performed by searcher and by finger, respectively. Figure 2 shows the block diagram of the base station demodulator.

B. Code Acquisition and Tracking

The purposes of the reverse link code synchronization are to acquire the access preamble in the access channel, to acquire traffic preamble, and to find the multipath profile in the traffic channel and access channel. From the code acquisition by the searcher, new mobile station or new potential paths for demodulation are acquired with coarse resolution such as a half chip resolution. Fine timing alignment such as one eighth chip resolution is obtained from the code tracking in the process of demodulation. The path diversity is obtained by implementing rake receiver with multiple demodulators. The searching results and finger information such as lock status, current path being locked and symbol energy are used to determine whether a finger is assigned to a new path or not.

In the base station, the uncertainty region for code acquisition is dependent on the cell size. In the current implementation the maximum cell size is limited to 50 km

and the demodulator cannot process signal delayed more than 384 PN chips (equivalently, 1.5 reverse link Walsh symbols). Therefore the number of tests that the base station performs for the code acquisition is 768 (384×2, with half PN chip resolution). With 8 searcher configuration as in the current implementation, each searcher needs to perform 96 (768/8) tests. Assuming that the integration period for performing each test is 512 PN chips, it takes 40 ms (96×512 PN chips) to test all the hypotheses. In the hypothesis testing for the code acquisition, sophisticated setting of decision threshold is required to obtain reasonably low false alarm probability. In the traffic mode, after detecting the mobile station's preamble, the base station begins to transmit traffic packet. After receiving valid frames from the base station, the mobile station stops transmitting preamble and begins to transmit traffic data. If the decision threshold is set too low, the base station easily takes noise for signal, it then cannot get back to the mobile station preamble detection state, and as a result, the call will be dropped. To satisfy this threshold setting requirement, the base station CDMA modem uses the maximum-likelihood search technique for initial code acquisition with single fixed dwell time detector [6].

The 1.2288 MHz of PN chip rate makes it possible to realize simple delay-lock loop with completely digital technique. The digital technique removes the arm balancing problem in the delay-lock loop, which may occur when it is implemented with analog technique. Every 1.25 ms (power control group), PN code phase is updated by the code tracking loop. In the CDMA system, the mobile station transmits data in burst mode. Therefore, in certain power control groups, no data are transmitted. This can cause error in the code tracking loop. For this reason, the code tracking loop is updated with the new error metric only if signal is present during the power control group. In addition, the code tracking loop can be set in the way it is updated if the combined Walsh symbol is the same as the demodulated Walsh symbol in the finger.

C. Rake Receiver

The rake receiver is implemented by combining Walsh symbols from multiple fingers for demodulation. The Walsh symbol that has the biggest combined correlation results is selected as the demodulated Walsh symbol. For symbol combining, all the correlation results of the received signal with possible 64 Walsh symbols are required; however, this increases computational complexity. In the implementation of CDMA rake receiver with base station ASICs by Qualcomm, Inc. [3], 4 fingers give the channel element processor only the correlation results with the winning Walsh symbol. In the channel element processor, the winning symbol whose correlation result is greater than a threshold is converted to 6 bit data. Before combining the symbol, the processor gives weights properly to the

correlation results. The 6 bit data and the weight corresponding to each bit are converted to 6 tuple vector. Then, the processor sums the symbol vector and are input to the serial Viterbi decoder for soft decision decoding. If all the winning symbols having magnitudes greater than a threshold are the same, then the performance of this method is the same as that of soft symbol combining system.

2. Base Station Modem ASICs

The base station CDMA modem is implemented in the base station channel card which is primarily responsible for processing calls within the base station. In the test system and the commercial system currently being developed, the base station channel card, which is responsible for transmitting and receiving signal to and from mobile stations over the air, has been implemented with two kinds of CDMA ASIC provided by Qualcomm, Inc. The first generation CDMA modem is comprised of CDMA ASIC set which consists of four base station demodulators, a base station modulator and a serial Viterbi decoder. In 1994, Qualcomm, Inc. introduced the second generation base station CDMA ASIC which is called cell site modem chip (CSM) where the first generation six chip set is integrated. This CSM makes the structure of CDMA modem and its control scheme simple. As a result, it becomes possible for one microprocessor to control several CDMA modems operating in a different channel application mode and in future system the size of digital shelf will be greatly reduced.

A. First Generation CDMA ASIC

The first generation CDMA modem is composed of 6 ASICs of 3 kinds, that is, four demodulators, a modulator, and a serial Viterbi decoder. The demodulator consists of a processing block, front end interface, microprocessor interface, and clock generator. The processing block is comprised of one demodulating finger and two searchers. The finger is used for data demodulation and code tracking, and the two searchers are used to continuously scan for other strong multipath signals. The front end interface selects one of six incoming data streams to feed to the finger or to the searchers. The input to the finger and searchers are independent. The microprocessor interface delivers processed data to the i960 for further digital signal processing such as rake combining and finger assignment to a new path. The clock generator receives the external clock signal, then generates and distributes the internal clock signal required by the demodulator. More detailed operation of demodulator is described in [1].

The incoming signal through each antenna is down-converted to baseband and sampled to produce a sequence of digital data that is at 8 times the PN chip rate (this is called system clock, 19.6608 MHz) and is in offset two's complement format.

For a three-sectored base station, data from different sectors are fed to the demodulator via 24 data lines. These data lines are divided into three groups of eight lines. Each group represents data from a specific sector and is split into channel I and Q. The data from two antennas of the same sector are time multiplexed onto these data lines. The synchronous input data lines to the demodulator have transition streams at the falling edge of the system clock and are demuliplexed for two antennas. The front end interface also controls the source for the finger and the two searchers according to the control of the i960CA. Since the current version of demodulator has some bugs in lock detector and code tracking loop operation, those are performed by software loaded on the i960CA. Furthermore, since each demodulator gives the i960CA only the magnitude for the winning symbol, the i960CA cannot perform soft symbol combining.

The modulator performs convolutional encoding to the forward link information data, interleaving, pulse shaping, Walsh covering to orthogonalize the forward channels, and symbol spreading. It also performs deinterleaving to the received data and feeding the deinterleaved data to serial Viterbi decoder for the processing of reverse link data. The modulator has two transmit sections. For each section, the transmitted symbols are covered with different Walsh sequence and spread by different pilot PN sequence with different gain. This structure enables softer handoff within a cell, i.e. within a channel card. Since each section can transmit pilot channel signal only, a modulator can transmit pilot signal together with sync channel data or paging channel data. More detailed operation of modulator is described in [3].

The Viterbi decoder uses the serial Viterbi decoding (SVD) algorithm to decode a synchronized and quantized code symbol stream. This chip is used in both base station and mobile station with properly setting the configuration. It includes an input buffer that allows data to be received via a serial input. It provides an interrupt signal for the microprocessor and an output buffer for the decoded data in order to isolate the microprocessor from system frame timing. The SVD also produces status information such as symbol error count, CRC check result, and the quality bit for the best state metric. The SVD is not given the code symbol rate when operating in some channel mode. It tries four possible rates (full, half, quarter, and eighth rates) and computes the processing status data mentioned above for each rate to assist the microprocessor to determine what the most probable data rate is. It may also serve as an indicator to decide whether or not the decoded frame is valid. The decoded output data are re-encoded and compared with the input code symbol to determine the symbol error count. The decoded data for the four possible data rates are stored in the output buffer, and after determining the most probable data rate, microprocessor can read

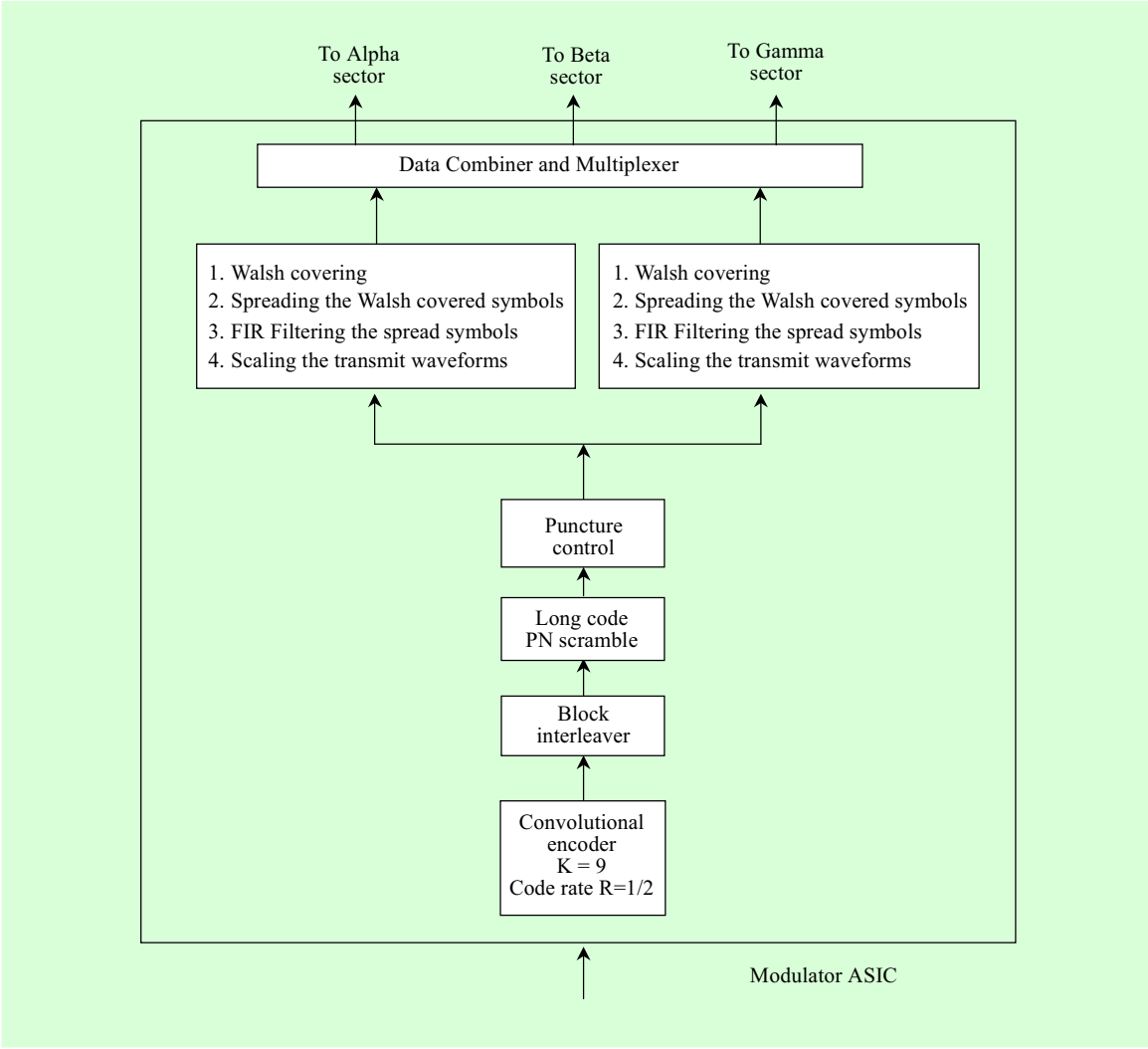

Fig. 3. Operations in the ASIC for the forward link.

the decoded data for that data rate by writing the predefined output buffer address for the most probable data rate into a register. More detailed information on the serial Viterbi decoder is in [3].

Data flows and operations in the CDMA ASICs for the forward link and reverse link are shown in Fig. 3 and Fig. 4, respectively.

B. Second Generation CDMA ASIC

In 1994, Qualcomm, Inc. introduced a new CDMA ASIC called CSM. This single chip can replace the previously described six first generation CDMA ASICs. Since it supports most of low level physical layer tasks such as lock detection, symbol-based demodulation, offset-based searching, and

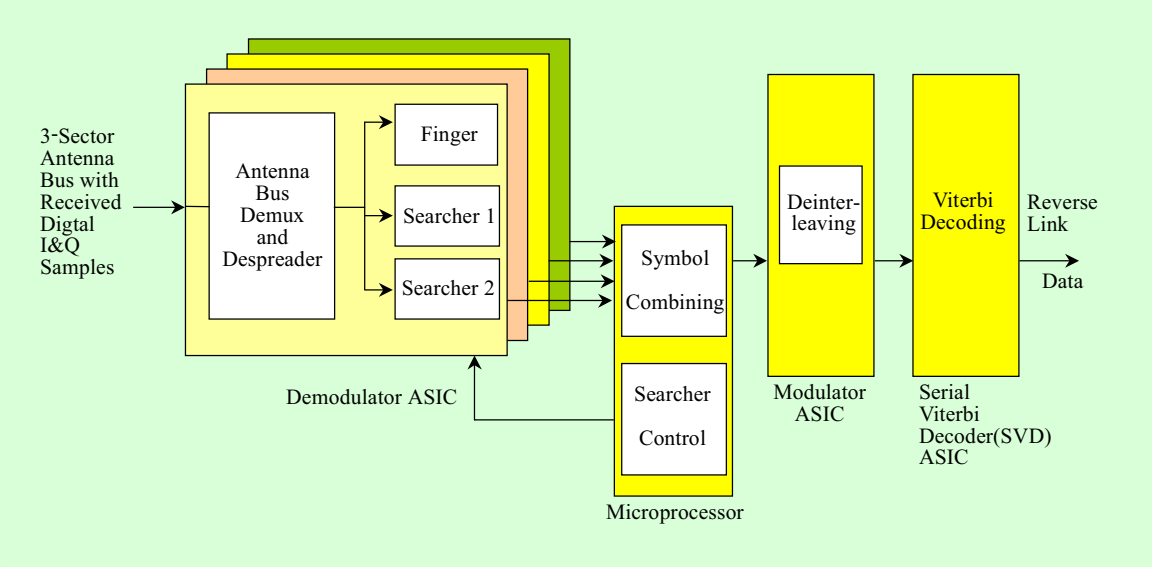

Fig. 4. Operations in the ASIC for the reverse link.

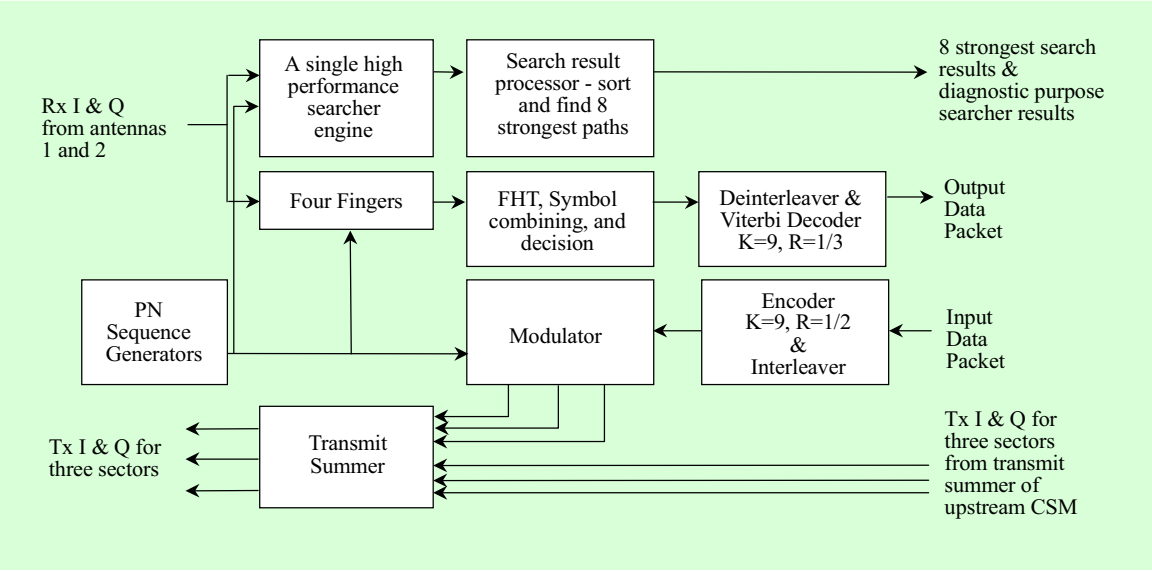

Fig. 5. High level block diagram of CSM [4].

sorting the searching results, a microprocessor can control several CDMA modems simultaneously. And since symbol combining is done in a chip, soft combining can be performed on the optimal basis. It can perform three-way softer handoff since one

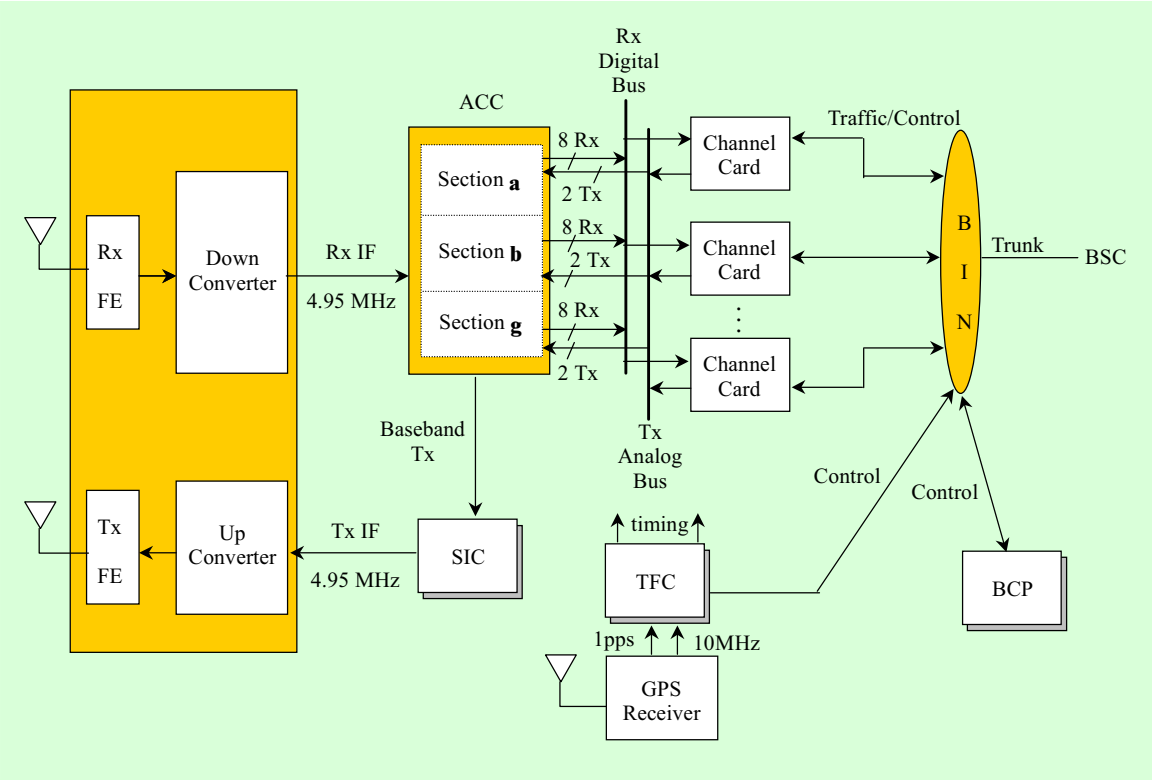

Fig. 6. Architecture of the BTS.

transmit section is added to the modulator section. Figure 5 is a block diagram of CSM. For more details, refer to [4].

III. SYSTEM ARCHITECTURE AND OPERATIONS

1. Architecture of BTS

The BTS is composed of RF unit, digital unit, BIN, and BCP. The architecture of the BTS and their interconnection are shown in Fig. 6. The analog common card (ACC) receives three timing signals: system clock (19.6608 MHz), a pulse every other second (EVEN_SEC clock), and a 10 MHz reference to be used for synthesizing the 4.95 MHz in reverse link QPSK demodulation. The ACC distributes system clock and EVEN_SEC to the rest of the digital shelf. In the forward link, the ACC combines the incoming baseband signals from the channel cards within a digital shelf. These signals start from the output of the modulator ASIC, then they are passed through a digital combiner. The I and Q outputs are converted to analog through a set of digital-to-analog converters and filters. The single ended analog

signals are converted into differential before going to backplane. The ACC receives these summed signal differentially and transmits them to the sector interface card (SIC).

In the reverse link, signals from the two antennas pass through the RF unit and enter the ACC. The signal is passed through a passive low pass filter and an AGC loop, then converted to digital signal. The output of four analog-to-digital converters (ADCs), which are 4-bit each at 9.8304 MHz, is passed through a MUX with an output of 8 bits at 19.6608 MHz.

The main function of the SIC is to combine the baseband forward link signals and to upconvert them to IF frequency. In the forward link, the SIC receives the combined baseband transmit signals from the ACCs, combines and amplifies them by a nominal gain about 0 dBm. This signal is then passed through a low pass filter (LPF) with bandwidth of 630 kHz. After these signals are passed through two mixers with the IF frequency (4.950 MHz, 0 and 90 degrees), they are combined and filtered via a bandpass filter.

The time and frequency reference card (TFC) receives one pulse per second (1 PPS) and the 10 MHz reference clock from the GPS receiver and generates the 19.6608 MHz system clock (SYS_CLK) synchronized to the 10 MHz clock by PLL, buffered 10 MHz reference clock, and the one pulse per two second (EVEN_SEC) time reference signal synchronized to 1 PPS signal. The TFC distributes these three timing signals to other devices in the BTS digital shelf. The TFC transmits and receives control messages to and from the BCP through the BIN, and it initializes the SIC and keeps monitoring the status of the SIC for the fault detection purpose. Two TFC boards are placed in the digital shelf to provide the redundancy. One of the TFC boards acts in the active mode and the other board stays in the standby mode. On detection of failure in the active TFC, the output is cut off and the control is handed over to the standby TFC.

The BCP controls and monitors the overall operations of the BTS, performs BTS hardware and software configuration, and manages resource allocation. In the power-up state, the BCP initializes the subordinate BTS devices, downloads executable codes and configuration data to the BTS devices according to the cell configuration data file. When a call is attempted, the BCP allocates resources such as frequency assignment, code channel, frame offset, and transmit power in the way to maximize the successful call completion rate and the resource availability. It also dynamically changes pilot power and cell RF total transmit power to maintain the traffic load balance between cells. The BCP monitors the operations of the BTS devices and reports the status to the BSM in case faults are detected. It is also duplicated to prevent catastrophic shutdown of the cell.

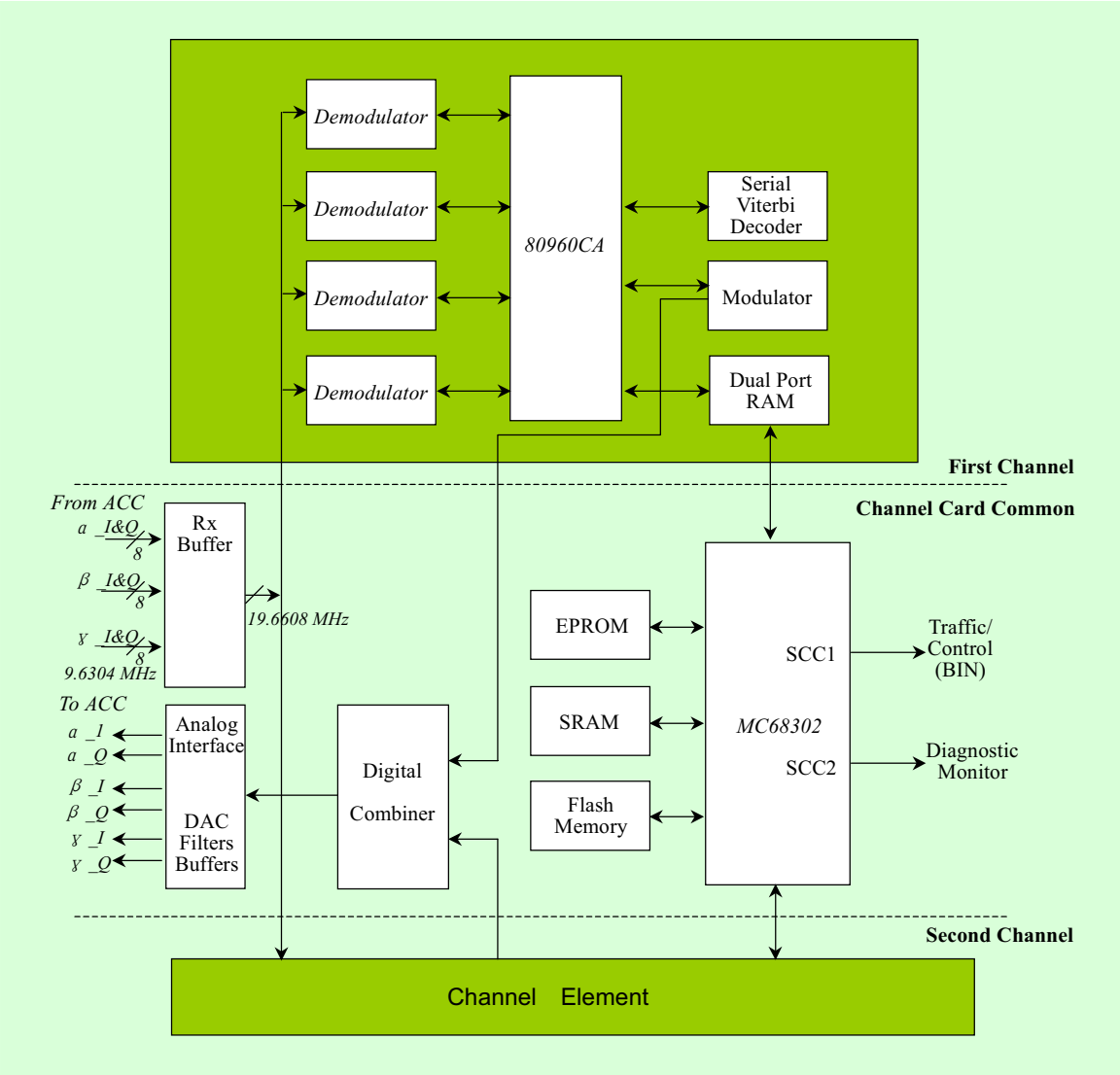

Fig. 7. Channel card using base station ASIC chip set.

2. Channel Card

The channel card consists of channel elements, channel card controller, and interfaces to packet switched network. Each channel element can carry out required CDMA signal processing operations for the forward channels and the reverse channels. The channel card is designed to be operated on the same hardware regardless of channel types. The channel element functions as a transmitter for the pilot channel, the sync channel, the paging channel, and the traffic channel on the forward link and as

a receiver for the access channel and the traffic channel on the reverse link by running different software on the same hardware. In the BTS initialization process, the BCP downloads the channel element software and configuration parameters which determine the personality of the channel element. Most of CDMA signal processing operations are carried out in the ASICs. We have implemented two versions of channel cards using two kinds of CDMA ASICs supplied by Qualcomm, Inc.

Figure 7 shows the block diagram of channel card using Qualcomm's first generation chip set. The channel card consists of two channel elements and a common section. Each channel element consists of 4 demodulators, one modulator, one serial Viterbi decoder, and a channel element processor. The common section consists of a channel card controller, a digital combiner, and digital-to-analog converters (DACs). The channel card controller routes traffic and control data between channel elements and base station network elements such as transcoding and selection block (TSB), BCP, logging devices and diagnostic monitor. On the forward link, the channel element receives traffic and control data packets from TSB, disassembles the packets, and separates out the control information. It then packetizes the traffic data and synchronizes it to the over-the-air timing. The modulator ASIC convolutionally encodes, interleaves, scrambles the coded symbols, and covers the data with the orthogonal Walsh sequence, then spreads it with I/Q PN sequences. The I/Q digital waveforms from two channel elements are combined and converted into baseband analog waveforms. The analog baseband signals from channel cards are combined and upconverted to the IF frequency band in the ACC and SIC.

On the reverse link, the channel element processor assigns a sector and an antenna to each demodulator ASIC for demodulation. The received digital data is input to the channel card from ACC through a 24-bit bus running at 19.6608 MHz which is 16 times the chip rate. This provides four-bit I and Q samples from six antennas at a 9.8304 MHz rate per antenna. The channel element processor combines the demodulated symbols from all the demodulator ASICs to take advantage of time and spatial diversity. The combined data is deinterleaved and decoded in the modulator ASIC and serial Viterbi decoder, respectively. The decoded voice data are then packetized and sent to TSB through the packet switched interconnection network.

The channel card using CSM ASIC, Qualcomm's second generation base station ASIC, is shown in Fig. 8. Six first generation base station ASIC chips, which are 4 demodulators, one modulator, and one serial Viterbi decoder, are integrated into a single CSM chip. In addition to integration density, most of low level physical layer processing such as lock detection, symbol-based demodulation, offset-based searching, and sorting the searching results, which is

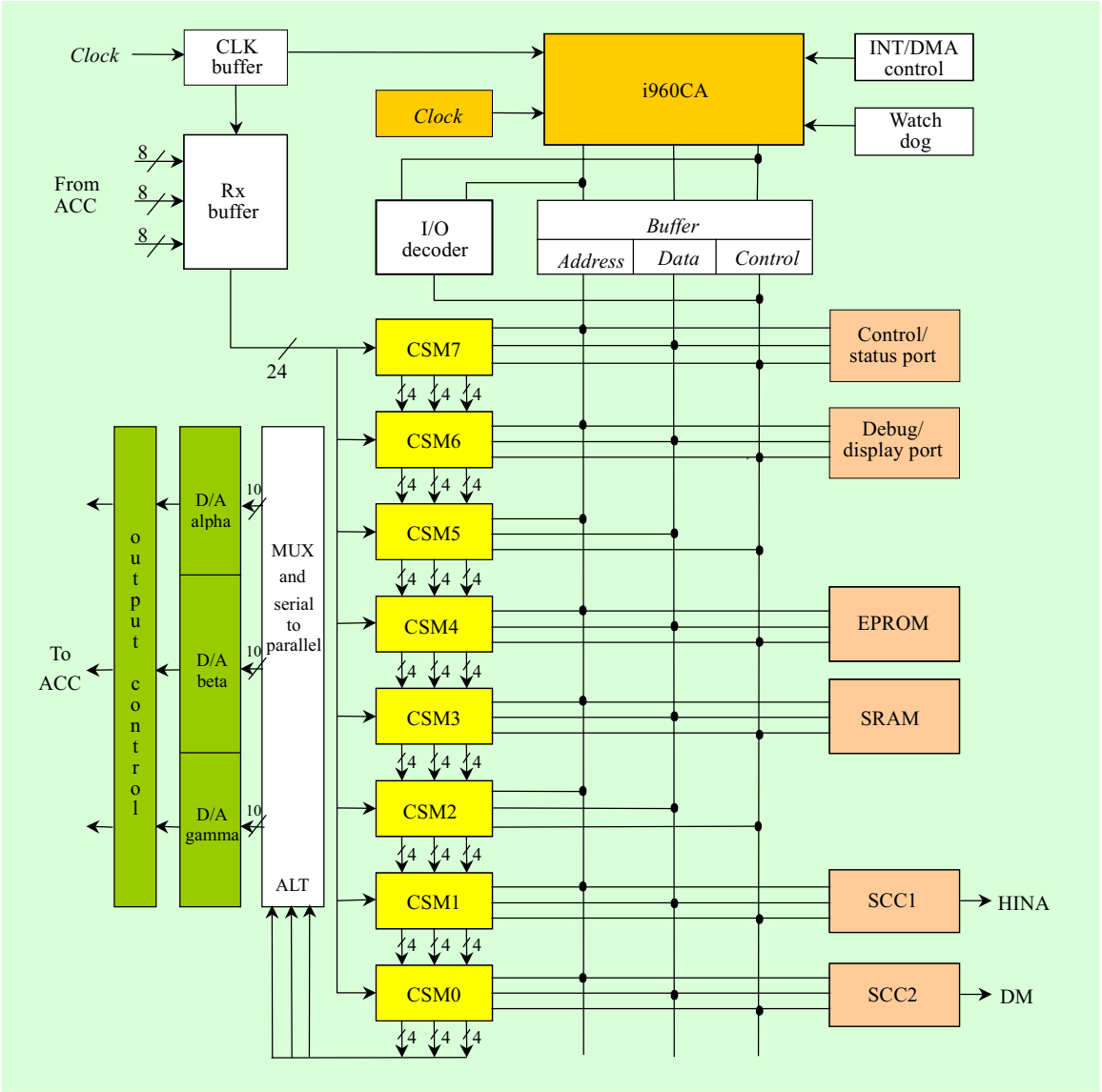

Fig. 8. Channel card using CSM ASICs.

carried out by the channel element processor for the first generation chip set, is performed inside the CSM chip. This makes channel card architecture of many CSM chips and a single control processor. Because of less computational and I/O burden, the control processor can control many CDMA modems simultaneously. In the CSM, the symbol combiner is implemented inside the chip. This makes it possible for each finger to give the symbol combiner all the correlation results of the received signal

with 64 possible Walsh symbols. The channel element processor gives the CSM only a threshold by which the CSM determines which finger should be enabled for combining. The symbol combiner combines the correlation results for Walsh symbol output from each enabled finger. The Walsh symbol that has the biggest combined correlation value is selected as a demodulated Walsh symbol. The channel card is designed to support 8 channel elements. The ASICs are controlled by a single processor. It has been shown that the Intel i960 processor has enough computing power to support more than 16 channel elements.

Figure 9 shows the picture of the implemented CDMA channel card using the first generation ASIC sets and the second generation ASICs.

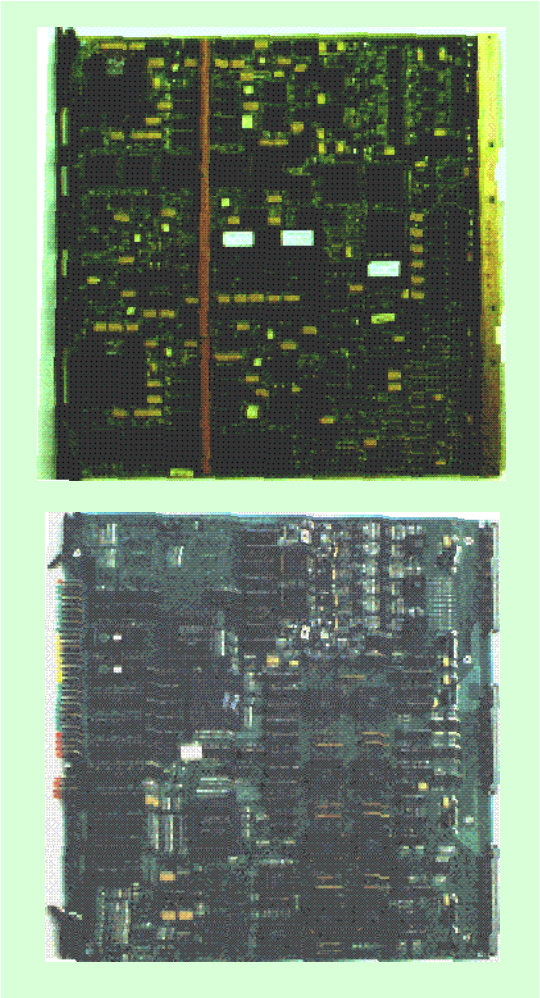

Fig. 9. The picture of the implemented CDMA channel cards.

3. Power Control in the BTS

CDMA is an interference-limited system in the sense that the system capacity is closely related to the amount of interference the system receives. Large capacity is one of advantages that CDMA system offers. However, the maximum capacity is achieved when the perfect power control is performed. This is because the amount of interference is determined by the received signal level from each user. The system capacity is maximized if the transmit power of each mobile station is controlled in the way that the cell received power is minimum as long as the base station can correctly demodulate the receiver signals. The purpose of the reverse link power control is to cope with the "near-end far-end problem". When some mobile stations are close to the base station they have stronger signals than mobile stations far from the base station and may cause unnecessary interference on the reverse link unless they are controlled. A combination of open loop and closed loop power control is used on the reverse link to command the mobile station

to adjust the transmit power. The mobile station measures the received power as a part of the open loop power control. In the closed loop power control mode, the base station measures the received power and makes decision whether it commands the mobile unit to increase or to decrease the transmit power. The objective of the forward loop power control is to keep the SNR at the mobile station almost constant. Mobile stations located near cell boundary will require more power than mobiles close to the center of the cell because mobiles far from the base station have more transmission loss and more interference from adjacent cells; this is known as the "corner problem". The reverse link and the forward link power control in the landside network is performed in the BTS and BSC. The operations for the power control performed in the BTS are described below.

A. Reverse Link Power Control

The mobile station measures the received signal power to estimate the path loss from the base station to the mobile unit. Mobile-received signal strength as a mobile drives away from the base station is typically represented by long-term fading (log-normal fading) and short-term fading (Rayleigh fading). The measured mobile-received power is used to estimate the path loss and to adapt to a sudden degradation or improvement in the channel. Prompt adjustment to this sudden change in the channel is important because slow response to the channel improvement will cause increase of received signal power at the base station, hence additional interference to all the other signals. The estimate of reverse link path loss is used to adjust transmit power at the mobile station. If the received signal level is high, the mobile station adjusts the power level downwards. Strong received signal indicates that the mobile is located near the base station or the path between mobile and base station is unusually good. In this case mobile needs less power to make the signal received at the base station keep a nominal SNR. This open loop power control mechanism determines the transmit reverse link power based on the received signal strength in the forward link. However, the CDMA system uses the frequency division duplex (FDD), in other words, the forward link and the reverse link have different frequency bands. This implies that the instantaneous path loss on the forward link is different from that on the reverse link. The necessity of closed loop power control comes from this independent fast fading. To account for this uncorrelated fading on the forward and the reverse links, the mobile station transmit power is also controlled by a command from the base station. At the base station, each demodulator measures the received signal strength and estimates E_b/N_o based on the measurements. If the measured E_b/N_o is greater than the desired value, $(E_b/N_o)_{\text{set point}}$, the base station sends the command to the mobile to adjust the transmit power downwards.

The channel element receives the threshold value, $(E_b/N_o)_{\text{set point}}$, from the TSB every 20 ms. This threshold value is used to send the power control command to the mobile station. The channel element computes the received E_b/N_o from the measured energy of the locked fingers every power control group (1.25 ms), and then it compares the measured E_b/N_o with $(E_b/N_o)_{\text{set point}}$. Power control commands are sent to the mobile station through the power control subchannel. The power control bit is not coded when it is sent to the mobile. The command bit punctures the coded symbols in the randomized position. This power control bit puncturing is performed in the modulator ASIC.

The reverse link power control algorithm in the network consists of an outer loop and an inner loop. The inner loop algorithm intends to maintain the desired reverse link signal to noise ratio, which is performed in the channel card of the BTS. The outer loop algorithm adjusts the desired reverse link signal to noise ratio based on the performance of the reverse link. In other words, the outer loop power control is to change $(E_b/N_o)_{\text{set point}}$ in order to maintain certain performance like FER. The TSB measures the FER from the traffic packets received from the BTS and compares it with the desired FER. It decreases the $(E_b/N_o)_{\text{set point}}$ if the measured FER is less than the desired FER, and then increases the $(E_b/N_o)_{\text{set point}}$ if the rate of the bad frames is getting larger.

B. Forward Loop Power Control

Assisted by the mobile station, the base station adjusts the amount of power allocated to each traffic channel so that the SNR at each mobile is almost constant. To each channel element, 7-bit of digital gain is assigned, and the transmit power is proportional to the square of the digital gain. As in the reverse link power control mechanism, the forward loop power control may consist of an open loop control and a closed loop control. In the open loop control, the base station estimates the forward link transmission loss based on the measurements of received signal strength from the mobile in the access procedure, then the base station assigns the initial digital gain for each traffic channel element. In the closed loop control, the base station adjusts the digital gain dynamically in cooperation with the mobile. Typically the base station continuously lower the digital gain until it receives any complaint from the mobile. The mobile station monitors the frame quality of the forward traffic channel. When the base station transmits signal with too low power, the FER at the mobile increases. The number of bad frame count is reported to the base station periodically and also at a moment when the count of bad frame exceeds certain threshold. If the base station recognizes that the forward FER (or equivalently the number of bad frames) exceeds some level, it increases the transmit power by assigning larger digital gain.

IV. BASE STATION TRANSCEIVER SUBSYSTEM

1. Reverse Path Units

A. Rx Front End Unit

The Rx Front End Unit (RxFU) provides a signal path for reverse link between the Rx antenna and the distribution shelf unit (DISU). Main functions of the RxFU are reverse signal filtering and sampling. It is basically designed for 4 frequency assignments (FAs) and is expandable to support up to 10 FAs. It has two blocks per sector for space diversity. With 3-sector system configuration, totally 6 blocks are used for one RxFU. Each block of RxFU shown in Fig. 10 is composed of directional coupler, Rx bandpass filter, LNA, attenuator, and 1:2 splitter.

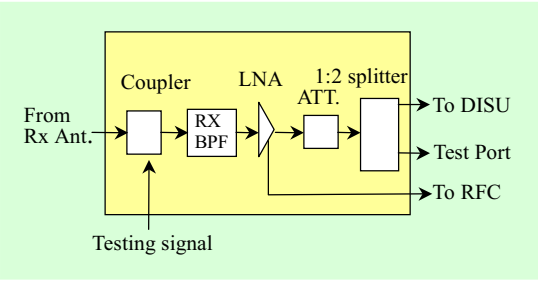

Fig. 10. One block structure of the RxFU.

The directional coupler is used for injecting test signal on the receive path. The level of coupling of the test signal must match Tx front end unit (TxFU) in order to properly simulate equal forward and reverse signal path loss. The Rx filter provides the rejection of signals which are out of cellular (25 MHz) band or allocated service band. It is typically a cavity type having low insertion loss and specially good selectivity. The LNA is a low noise and high dynamic range amplifier for amplification of the received signal. A balanced type configuration is desirable because of the soft failure mode. The attenuator is used for gain matching to desired level, and the 1:2 splitter provides test port for RxFU block on system operation without disturbance. The control signal from the LNA is interfaced with the RFC and used for monitoring whether the LNA is fault or not.

The levels of each device in the RxFU are determined to match signal input level condition (Gain=12∼16dB, NF<3.2dB) to down-converter unit following the DISU. In the DISU, the divider is used for signal distribution to each down-converter unit (max. 5 EA including redundancy). The dividing loss in the DISU should be considered in the design of the RxFU.

B. Receiver Card

The receiver card provides the signal path from the RxFU to the DISU. It performs the following functions:

- Down-conversion from UHF to an IF of 4.95 MHz,
- Cell blossoming, wilting, and breathing through controllable noise figure degradation under the control of RFC,
- Received signal strength indicator (RSSI).

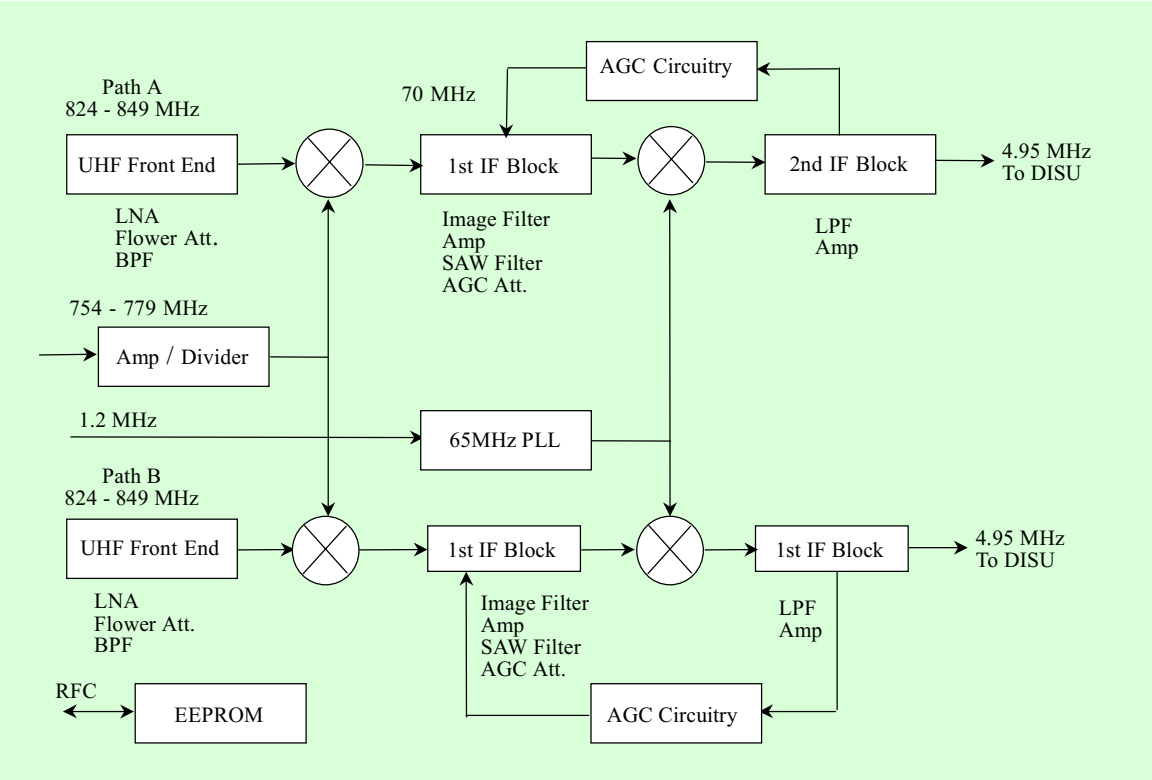

Fig. 11. Block diagram of the receiver card.

The receiver card shown in Fig. 11 has a double conversion configuration. The 824 to 849 MHz UHF is first mixed down to 70 MHz among which desired CDMA channel is selected by SAW filter in the first IF block, then to 4.95 MHz. Two diversity receivers (Rcvr 0 and Rcvr 1) are incorporated in one receiver card. This kind of receiver is a component of the spatial (path) diversity feature of CDMA. Both receivers share a common UHF local oscillator (LO) (754 to 779 MHz) that is generated on the up-converter card and a common 65 MHz LO.

The first LNA on the receiver card is a low noise and high third order intercept point (IP3) amplifier. Flower attenuators give the interface between the RFC control and the variable attenuators, which perform cell blossoming, wilting, and breathing functions. The UHF is down-converted to the first IF of 70 MHz. The mixer has a high intercept point. The mixer output is duplexed to maintain broadband termination for mixer spurs and is then sent to the first 70 MHz IF amplifier (high IP3 and gain). SAW1 along with SAW2 located on the first IF block, provide the selectivity needed to meet the 750 kHz desensitization

specification. The rest of the 70 MHz IF chain consists of a sequence of gain blocks and AGC. AGC blocks consist of PIN diode and π-pad attenuators. AGC detector in the AGC circuitry consists of Schottky diode to sample the 4.95 MHz. Loop filtering is performed by an op-amp integrator. Loop gain variation is minimized by a linearizer. The absolute signal strength is derived from the AGC. The 4.95 MHz chain consists of a duplexer followed by a moderate gain amplifier. The final amplifier is fairly robust to maintain signal integrity at an output level of -3 dBm.

2. Transmit Path Units

A. Transmit Front-end Unit

The Transmit Front-end Unit (TxFU) provides a signal path for forward link between the HPAU and the Tx antenna. And the main functions of the TxFU are forward signal filtering and sampling. One TxFU for 3-sectors is configured three block, and each block structure shown in Fig. 12 is composed of Tx bandpass filter and directional coupler. The Tx bandpass filter provides the rejection of out-of-cellular band and passes the service band signals, which is designed with cavity types for low insertion loss and good selectivity. If more suppression on band edge is required, additional notch filter can be used. The directional coupler is used for sampling test signal to BTU on the transmit path. The level of coupling of the test signal must match the RxFU in order to properly simulate equal forward and reverse signal path loss.

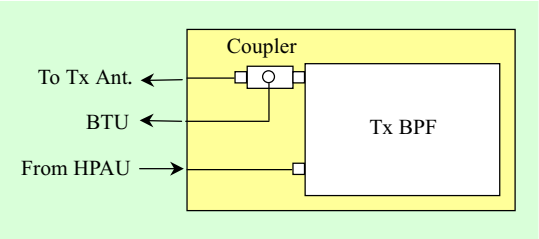

Fig. 12. One block structure of the TxFU.

B. Upconverter Card

The upconverter card provides the frequency upconversion as shown in Fig. 13. The upconverter card receives the 4.95 MHz IF signal from the SIC and upconverts the signal to UHF. The upconverter card filters the signal to reduce spurious energy less than $\pm$820 kHz from the channel center. It also provides gain adjustment to the transmit power tracking loop (TPTL) and cell blossoming, wilting, and breathing functions initiated by RFC.

The 4.95 MHz input signal is started with 4 dB attenuator to meet the 1.4:1 input VSWR specification and to reduce the signal to the required level to the mixer. The lowpass filter is a non-tuned LC filter that reduces the noise bandwidth and harmonics of the input signal. The 3 dB point of this filter is normally 7.75 MHz. The lowpass filter is followed by a resistive pad for impedance matching to the mixer. The two variable attenuators in the 114.99 MHz IF section are used to give the upconverter

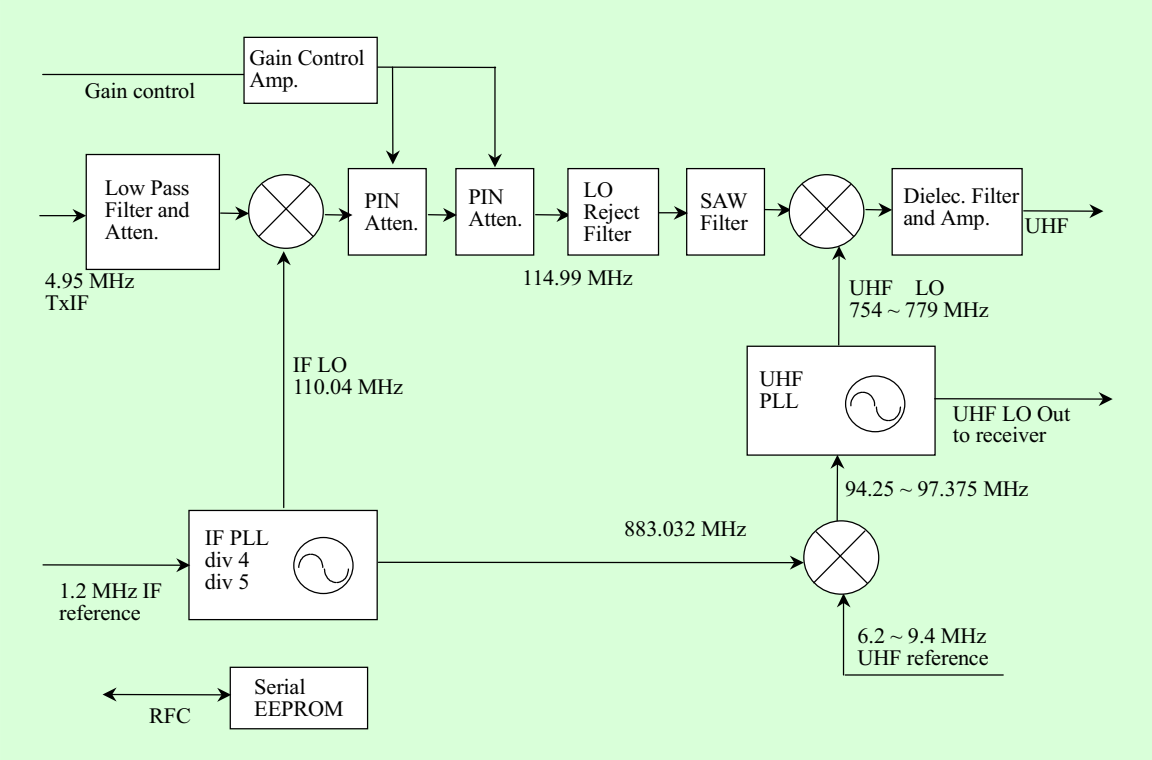

Fig. 13. Block diagram of the frequency upconverter.

variable gain control to correct for process gain variations of the entire forward link.

In addition, the pin attenuators provide attenuation for cell blossoming, breathing, and wilting. Both attenuators are controlled by a single analog voltage that originates from RFC. The transmit signal frequency, 869 MHz to 894 MHz, is obtained by mixing the IF signal with UHF LO. At UHF, the dielectric bandpass filter yields 60 dB of attenuation at the transmit LO frequencies, 754 MHz to 779 MHz. The transmit LO frequencies are also provided for the receiver card. A 1.2 MHz, pseudo ECL, balanced differential input is received from the RFC. This signal is used as a reference for a 440.16 MHz PLL. The output of the PLL is split. One half is divided by four to yield the 110.04 MHz IF LO. The other half is divided by five to yield 88.032 MHz. This is mixed with the UHF LO reference from the RFC. This signal, 94.25 MHz - 97.375 MHz is used as the reference for the PLL that produces the final 754 MHz to 779 MHz UHF LO. The UHF LO reference, generated on the RFC, varies from 6.2 MHz to 9.4 MHz. DDS synthesizer on the RFC can tune the upconverter to any frequency with 0.126 Hz resolution between 868.95 MHz and 893.97 MHz. The

serial EEPROM holds linearization information for the PIN diode attenuators for the upconverter card.

C. High Power Amplification Unit

The High Power Amplification Unit (HPAU) provides a signal path for forward link between the DISU and the TxFE. Main functions of the HPAU are amplification of signal for transmitting, combining two RF channels, and forward power detection for transmit power tracking loop (TPTL).

One HPAU as shown in Fig. 14 supports one sector, and is designed for 2 FAs. It is composed of two class AB HPAs, one 2:1 channel combiner, and two power detector. Each HPA provides amplification of the transmit signal and the suppression of distortion caused by intermodulation product. The HPA is controlled by the RFC to change status enable/disable, and is monitored if it is in the right operation. Each power detector receives the coupling signal from each HPA output, converts to dc voltage, and transmit to the RFC for the operation of TPTL. Also, the power detector has dc voltage level data representing the HPA output signal level in EEPROM. On initialization of BTS, the data in EEPROM is read by the RFC and used as reference data for TPTL operation. The channel combiner provides two channel combining and is configured by the isolator, channel bandpass filter, and the combiner. The isolator protects HPA from returning signal (f_1) caused by mismatch and spilling over other channel (f_2).

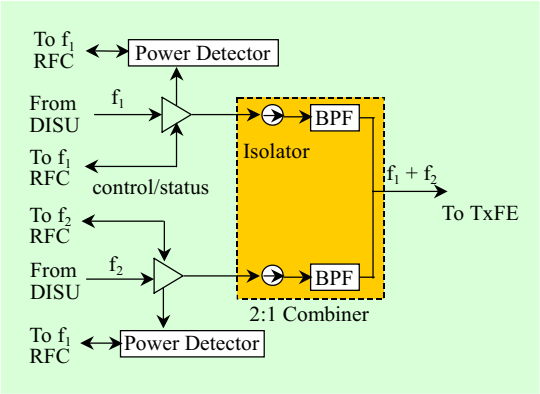

Fig. 14. A structure of the HPAU.

V. CONCLUSIONS

Design concept and the implemented system structure of the CMS are described. Most of physical layer operations between CDMA base station and mobile station air interface are performed in the CDMA ASICs and their control logic circuits. To be a commercial system the base station needs to be highly integrated and the critical modules ought to be duplicated. As a commercial prototype system, eight channel elements have been implemented in a single channel card. It is noticed that higher density channel card such as 16 or 32 channel elements per card can be realized with CSM modem ASICs and sophisticated control software. The specifications of the RF unit is chosen through the system link budget based on macro-cell coverage. To make the system reliable, the system is designed to have redundancy. It is the BCP that configures the BTS devices and controls the

overall operations of the BTS. The call control algorithm and the resource management algorithm with configuration parameters play a significant role in the optimal cell planning. These algorithms and the operating parameters of the BCP are being verified and improved through the field test with the help of the performance evaluation tools.

REFERENCES

[1] TTA, *TTA - 62: Common Air Interface for Digital Cellular in the 800 MHz Band*, Korea: Telecommunications Technology Association, 1994.

[2] S. Kim, P. Song, J. Kim, and H. Lee, "Investigation of CDMA air interface and protocols," in this issue, pp. 303-315.

[3] Qualcomm, Inc., *CDMA Base Station ASIC User Manual*, DL80-7251-2-X3, Jan. 1993.

[4] Qualcomm, Inc., *CDMA Cell Site Modem ASIC*, 80-12125 X4, 1994.

[5] Dong-Wook Lee, Jin-Su Kim, Young-Gyun Cheong, and Myoung Jin Kim, "A method for controlling multi-purposed channel card in CDMA cellular telephone system," applied for Korea patent, 1995.

[6] M. K. Simon, J. K. Omura, R. A. Scholtz and B. K. Levitt, *Spread Spectrum Communications Vol. III*, Computer Science Press, Chap.1-2, 1985.

[7] Lee and Messerschmitt, *Digital Communication*. KAP, 1988.

[8] Stephen J. Erst, *Receiving System Design*. Artech House, 1984.

[9] William Gosling, *Radio Receiver*, Peter Perregrinus, Ltd., 1986.

[10] Guillermo Gonzalez, *Microwave Transistor Amplifiers Analysis and Design*. Prentice Hall, 1984.

[11] William C.Y. Lee, *Mobile Communications Engineering*. McGraw-Hill, 1982.

[12] Robert C. Dixon, *Spread Spectrum Systems*. John Wiley & Sons, Inc., 1984.

Dong-Wook Lee
See *ETRI Journal*, vol. 19. no. 1, p. 11, Apr. 1997.

Kisuk Yoo received the B.S. and M.S. degree from Korea University, Seoul, Korea in 1980, 1982, respectively, all in electronics engineering. He received the Ph.D. degree in electrical engineering from the Florida Institute of Technology, Melbourne, Florida, U.S.A. in 1993. Since he joined ETRI in 1993 as a Senior Member of Research Staff, he has been working for Radio Technology Section in Mobile Telecommunication Division of ETRI. His research interests are robust control system, especially RF signal control, and RF components.

Jin-Su Kim
See *ETRI Journal*, vol. 19. no. 1, p. 11, Apr. 1997.

Myoung Jin Kim was born in October 1958, in Seoul, Korea. He received the B.S. and M.S. degrees in control and instrumentation engineering from Seoul National University, Seoul, Korea, in 1982 and 1984 respectively, and the Ph.D. degree in electrical engineering from the University of Minnesota, Minneapolis, Minnesota, in 1992. During 1984-1996, he worked at ETRI, Taejon, Korea, where he was involved in research and development projects for CDMA digital cellular system and PCS. Since 1996,

he has been an assistant professor at the Department of Information and Communications Engineering at Hankuk University of Foreign Studies (HUFS), Yongin, Korea. His research interests are code division multiple access, wireless communications, and theory and application of multi-scale techniques and wavelets.

Jae-Hong Park He received his BS, MS, and Ph.D degrees in electrical engineering from Seoul National University in 1978, 1980, and 1995, respectively. He developed electronic warfare system in Agency for Defence Development from 1979 to 1985. Since joining ETRI in 1985, he had developed satellite sommunication and broadcasting systems for Koreasat until 1994. Currently he is in charge of Radio Technology Section of Mobile Telecommunication Division and involved in CDMA cellular system development and PCS development. His major interests are modulation, channel coding, and radio communication systems.