An Improved Base Station Modulator Design for a CDMA Mobile System

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CONTENTS

ABSTRACT

We propose a new method to eliminate completely the redundant elements in a CDMA (code division multiple access) mobile system. First, we define multilevel logic operation (MLO), which is a new concept to deal with the multilevel logic signals. We prove that the conventional binary logic concept is a subset of the MLO concept. The multilevel logic signal can be directly controlled by using this MLO in place of the binary operation. We applied the MLO to the CDMA base station modulator (BSM) in order to reduce the hardware complexity. In the case of a 3-sectorized cell, this method helps reduce the complexity down the level of below 1% of the conventional CDMA BSM for spreading and filtering, and to 50% for Walsh covering.

I. INTRODUCTION

Spread spectrum techniques have been used since the mid-1950s in various practical applications such as military antijam communications, guidance systems, and experimental antimultipath systems. Spread spectrum is a technique that uses a wide *radio frequency* (RF) bandwidth in transmitting a signal - substantially wider than its information bandwidth - to achieve a certain operational advantage. Two fundamental spectrum spreading techniques are *direct sequence* (DS) *pseudonoise* (PN) modulation and frequency/time hopping. DS may be generated by phase-modulating an RF frequency with a fast pseudorandom sequence which was multiplied by a binary data sequence. Its effective bandwidth becomes approximately equal to the sequence bit rate. Frequency/time hopping is generated by shifting (or hopping) the RF carrier/time slot to different frequencies/times in a pseudorandom way. Hybrid combinations of these techniques are also frequently used.

While *direct sequence/code division multiple access* (DS/CDMA), the technique of interest in this paper, uses up a wide bandwidth, its bandwidth inefficiency may be compensated by its interference reduction capability. This technique can give the desired signal a power advantage over many types of interference, including intentional interference and makes it attractive for mobile radio networks (e.g., radio telephony, packet radio, and amateur radio), timing and positioning systems, and some applications in satellites. A specific form of the technique known as DS/CDMA was selected as the EIA/TIA IS-95 standard for commercial digital cellular systems [1].

In this paper, we will describe a design technique for what is known as the *base station modulator* (BSM) of a DS/CDMA mobile system. We first look at the basic theory of DS/CDMA and examine the conventional application of this theory to digital cellular communications systems. We will also define *multilevel logic operations* (MLOs) that are extension of the conventional binary logic operations. We then apply MLO to the design of BSM, which results in reduction of complexity.

II. DS/CDMA MOBILE SYSTEMS

1. Background Principles for DS/CDMA

In DS/CDMA [2]-[4], each user is given a code that is approximately orthogonal to (i.e., has low cross-correlation with) other user's codes. That is,

$$\frac{1}{T}\int_0^T p_i(t)\, p_j(t)\, dt \cong \begin{cases} 1, & i = j \\ 0, & i \neq j \end{cases}, \qquad (1)$$

where $p_i(t)$ is the spreading sequence waveform of i-th user. However, because CDMA systems are typically asynchronous (i.e., the transition times of the data symbols of the different users do not have to coincide), it

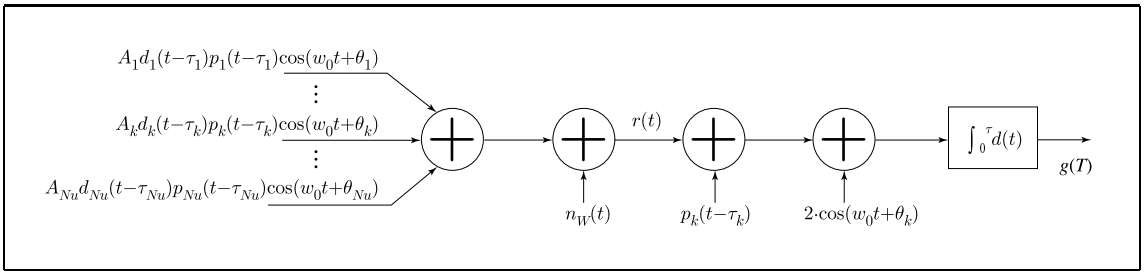

Fig. 1. DS/CDMA System.

is important to use the codes with very low cross-correlation between the user's codes for good acquisition of the user's signals. Hence the key features in DS/CDMA systems are both the cross-correlation and the partial-correlation functions, and the design and optimization of code sets with good partial-correlation properties can be found in many references, such as [5], [6], and [7].

A typical DS/CDMA system is shown in Fig. 1. In this figure, the received signal $r(t)$ is given by

$$r(t) = \sum_{i=1}^{N_u} A_i d_i(t-\tau_i)\, p_i(t-\tau_i)\cos(\omega_0 t+\theta_i) + n_w(t), \tag{2}$$

where

N_u = total number of users,

$d_i(t)$ = message of i-th user (± 1),

$p_i(t)$ = spreading sequence waveform of i-th user,

A_i = amplitude of i-th carrier,

θ_i = random phase of i-th carrier uniformly distributed in [0, 2π],

τ_i = random time delay of i-th user uniformly distributed in [0, T],

T = symbol duration,

$n_w(t)$ = additive white Gaussian noise.

Assuming that the receiver is correctly synchronized to the k-th signal, we can set both τ_k and θ_k to zero without loss of generality. The output $g(T)$ of the integrate-and-dump process can be represented by

$$g(T) = A_k + \frac{1}{T}\sum_{i=1,\, i\neq k}^{N_u} A_i \int_0^T d_i(t-\tau_i)\, p_i(t-\tau_i) \cdot p_k(t)\cos\theta_i\, dt + \frac{2}{T}\int_0^T n_w(t)\, p_k(t) \cdot \cos\omega_0 t\, dt, \tag{3}$$

where double-frequency terms have been ignored.

Notice that the second term on the *right hand side* (RHS) of (3) is a sum of N_u-1 terms of the form

$$A_i \cos(\theta_i) \int_0^T d_i(t-\tau_i)\, p_i(t-\tau_i)\, p_k(t)\, dt.$$

Since the i-th signal is not, in general, synchronized with the k-th signal, $d_i(t-\tau_i)$ will change its signs somewhere in the interval [0, T] for 50 percent of the time. As a result, the above integral becomes the sum of two partial correlations of $p_i(t)$ and $p_k(t)$, rather than one

total cross-correlation. Therefore, (3) can be rewritten as

$$g(T) = A_k d_k(t-\tau_k) + \sum_{i=1,\, i\neq k}^{N_u} A_i d_i(t-\tau_i)\,(\rho_{ik}(\tau_i) + \widehat{\rho_{ik}}(\tau_i))\cos(\theta_i) + n(T), \quad (4)$$

where

$$\rho_{ik}(\tau_i) = \frac{1}{T}\int_0^{\tau_i} p_i(t-\tau_i)\,p_k(t)\,dt,$$

$$\widehat{\rho_{ik}}(\tau_i) = \frac{1}{T}\int_{\tau_i}^{T} p_i(t-\tau_i)\,p_k(t)\,dt,$$

$$n(T) = \frac{2}{T}\int_0^{T} n_w(t)\,p_k(t)\cos\omega_0 t\,dt.$$

Notice that $\rho_{ik}(\tau_i) + \widehat{\rho_{ik}}(\tau_i)$ is the total cross-correlation between the *i*-th and *k*-th spreading sequences. Therefore, the completely orthogonal codes allow any user's message demodulated uniquely.

2. Conventional Structure of BSM in CDMA System Based on IS-95

Fig. 2 shows a conventional block diagram of the 3-sectorized BSM [8] which has been developed by Qualcomm Inc. in compliance with IS-95 [1]. In this figure, input to the convolutional encoder is digital voice data generated by the *Qualcomm code excited linear prediction* (QCELP) variable rate vocoder. The QCELP vocoder provides 4 different data rate - 9.6kbps, 4.8kbps, 2.4kbps, or 1.2kbps - including 8 tail bits for convolutional encoding. Due to 1/2 coding rate, the output symbol rate of the convolutional encoder becomes twice the input bit rate, resulting in 19.2ksps, 9.8ksps, 4.8ksps, or 2.4ksps, respectively. These variable rate symbols are repeated 0, 1, 3, or 7 times according to rate by the symbol repetition block so that the output symbol rate becomes a 19.2ksps fixed rate. The redundancy by symbol repetition is compensated for by controlling its transmission power such that the average energy per bit maintains. Then the repeated symbols are interleaved by the block interleaver to increase the immunity against the burst error that frequently occurs in mobile radio environments. These interleaved symbols are scrambled with the long code PN sequence that is generated by a 42-bit shift register. The scrambled symbols are pseudorandomly punctured with a cycle of 800 Hz by the decimated long code PN sequence and substituted for a power-control bit supplied via a microprocessor interface. This power-control bit is used to control the mobile transmission power. Each symbol outputted from the puncture control block is then covered with a distinct Walsh sequence that is selected via the microprocessor interface. With the use of 64-ary Walsh symbols, the output Walsh chip rate becomes 1.2288 Mcps and one Walsh code is assigned to only one user. Forward channels from the base station to the mobile station are differentiated and identified by the Walsh code. Two forward-channel transmit symbol streams are thus formed, which correspond to the two transmit sections in the Fig. 2. These two forward-transmit channels are required to support the softer handoff that is defined as a handoff occuring between two sectors with-

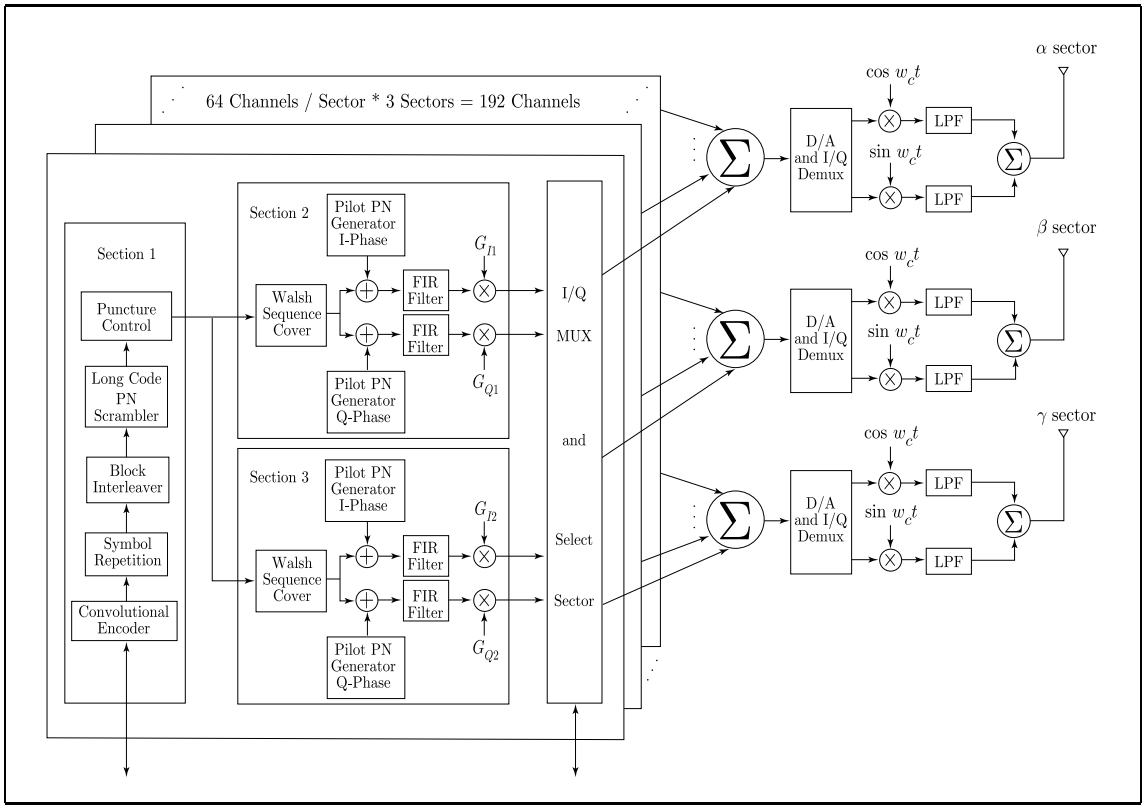

Fig. 2. Conventional CDMA Base Station Modulator Structure.

out temporarily disconnecting the call. The Walsh covering guarantees orthogonality between various users in the same CDMA radio channel. After a Walsh covering, the symbols are QPSK-spreaded via two (*in-phase* (I) and *quadrature-phase* (Q)) PN sequences. One sequence is used to form the I channel, and the other the Q channel. Shifted versions of the two basic sequences, that are common to all forward channels,are used to differentiate sectors/cells. After spreading, the chip signals are low-pass filtered by 48-tab *finite impulse response* (FIR) filters. The filtering limits the bandwidth of the transmitted signals, as required, to limit interference with adjacent CDMA radio channels. The filters smooth the transitions between symbols with different bit rates. After filtering, the transmit waveforms are scaled to provide power control in the forward channel and a scaling factor is supplied via the microprocessor interface. The BSM provides output to three base station sectors. Each output may be programmed via the microprocessor interface to provide multiplexed I and Q from either of the two transmit sections. The outputs may also be programmed to pro-

vide a sum of two transmit sections as multiplexed I and Q.

There are 192 multiplexed I and Q signals in a 3-sectorized cell. These 64 multiplexed I and Q signals per each sector are combined digitally via the digital combiner and converted to analog signals. These analog signals are then demultiplexed and modulated with the carrier frequency. The modulated I and Q signals are filtered through the *low pass filter* (LPF) and summed prior to be transmitted.

III. MULTILEVEL LOGIC OPERATIONS (MLOs)

Binary logic is used to describe the manipulation and processing of binary information. It is done by logic circuits called gates. Gates are blocks of hardware that produce signals of binary "1" or "0" when input logic requirements are satisfied.

Generally, the binary logic operator has two binary inputs and one binary output that can be represented as

$$z = O(x,\ y), \quad x,\ y,\ z \in GF(2), \tag{5}$$

where O(x, y) means binary logic operation with two binary logic input x and y, and $GF(2)$ is a Galois field of two elements. If we assume that this operator is symmetric for its two inputs, that is, $O(x,\ y) = O(y,\ x)$, the number of different binary operators is 2^3 including two trivial operators that always output a logic "0" (reset operator) or a logic "1" (set operator) without regard to its inputs. Thus six kinds of binary logic operator can be defined - AND, OR, XOR (exclusive OR), NAND, NOR, XNOR (exclusive NOR) gates. These gates can be classified into two groups. Output of the one group that consists of AND, OR, XOR gates is opposite from that of the other group that consists of NAND, NOR, XNOR gates, respectively. Thus, we can also define the NOT operator that negates the logic value of its input variable. As a result, four kinds of binary logic operator are sufficient to design all binary logic circuits, except in trivial cases.

However, in many digital circuits these operators are often accompanied by some arithmetic operators such as arithmetic adder and arithmetic multiplier. In this case, the output of this circuit is no longer binary; it becomes multiple-valued. This multiple-valued logic, in which the number of discrete logic is not confined to two, has been the subject of much research over many years. The multiple-valued logic is manipulated by using Max, Min, or Unary operators [9]. We call this multiple-valued logic a multilevel logic in this paper. Implementation of these multilevel logic operators is usually complex and costly because 1) each multilevel logic unit must be represented by more than one bit, where the number of bits depends on the level of the logic, and 2) the multilevel logic circuit consumes a lot of power due to its increased data rate. A solution to this problem is to come up with a binary logic circuit that is equivalent to

the given MLO and yet easy to implement.

To define MLOs, we will extend the conventional binary logic operations into the MLOs, which has one $(A+1)$-ary input and one $(B+1)$-ary input. $A+1$ and $B+1$ are radixes of input logics of MLO. By intuition, we define the MLO whose two inputs have multilevel logic values as follows [10]:

$$\begin{aligned} &AND(x,\ y)=xy,\\ &OR(x,\ y)=xA+yB-xy,\\ &EXOR(x,\ y)=xA+yB-2xy,\ \text{and}\\ &NOT(x)=\bar{x}, \end{aligned} \tag{6}$$

where $x\in GF(B+1)$, $y\in GF(A+1)$, $AND(\ )$, $OR(\ )$, $EXOR(\ )$, and $NOT(\ )$ denote the multilevel logic AND, OR, exclusive-OR, and NOT operation, respectively, and $\bar{x}$ denotes the (radix-1)′s complement of x, that is, $\bar{x}=B-x$.

These definitions satisfy binary logic operations as well. That is, if we let A and B be 1 in the above equations, then the MLO defined in (6) becomes binary operation. Therefore, this MLO is an extension of binary logic operation. We now show an important theorem :

Theorem : Let $x_i,\ y_i\in\{0,\ 1\}$. Then,

$$\sum_{i=0}^{k-1}(x_i\oplus y_i)=\frac{1}{k}EXOR\left(\sum_{i=0}^{k-1}x_i,\ \sum_{i=0}^{k-1}y_i\right),$$

$$\text{if}\quad k\sum_{i=0}^{k-1}x_iy_i=\sum_{i=0}^{k-1}x_i\sum_{j=0}^{k-1}y_j. \tag{7}$$

Proof : The proof of the theorem is straightforward. Let $x_i,\ y_i\in\{0,\ 1\}$. Using the above definition, RHS of (7) is given as the following.

$$\frac{1}{k}EXOR\left(\sum_{i=0}^{k-1}x_i,\ \sum_{i=0}^{k-1}y_i\right)$$

$$=\frac{1}{k}\left(k\sum_{i=0}^{k-1}x_i+k\sum_{i=0}^{k-1}y_i-2\sum_{i=0}^{k-1}x_i\sum_{j=0}^{k-1}y_j\right)$$

$$=\sum_{i=0}^{k-1}(x_i+y_i-2x_iy_i),$$

$$\text{if}\quad k\sum_{i=0}^{k-1}x_iy_i=\sum_{i=0}^{k-1}x_i\sum_{j=0}^{k-1}y_j$$

$$=\sum_{i=0}^{k-1}(x_i\oplus y_i),\ \text{by definition. Q.E.D.}$$

Assuming that x_i is a constant binary logic value c, then (7) becomes

$$\sum_{i=0}^{k-1}(c\oplus y_i)=EXOR\left(c,\ \sum_{i=0}^{k-1}y_i\right). \tag{8}$$

The result is very useful in a digital circuit design.

To show the design efficiency of the defined MLO, consider the simplified BPSK modulation circuit from the base station modulator for a DS/CDMA mobile system [1]. Assume that this modulation circuit has k user's binary information signals and one modulating binary signal as shown in Fig. 3(a). This circuit produces a sum of each user's signals that are BPSK modulated, bandlimitted, and amplified digitally.

Let P_I be a binary modulating signal in BPSK, V_i, $i=0,\ 1,\ \ldots,\ k-1$ denote the binary information signal of i-th user, and G_i, $i=0,\ 1,\ \ldots,\ k-1$ denote the gain factor for i-th user. Then, the output S in Fig. 3(a) is given by

$$S=\sum_{i=0}^{k-1}G_i\ FIR\{(P_I\oplus V_i)\}, \tag{9}$$

where $FIR\{\ \}$ denotes FIR filtering used to limit the bandwidth of transmitting signals,

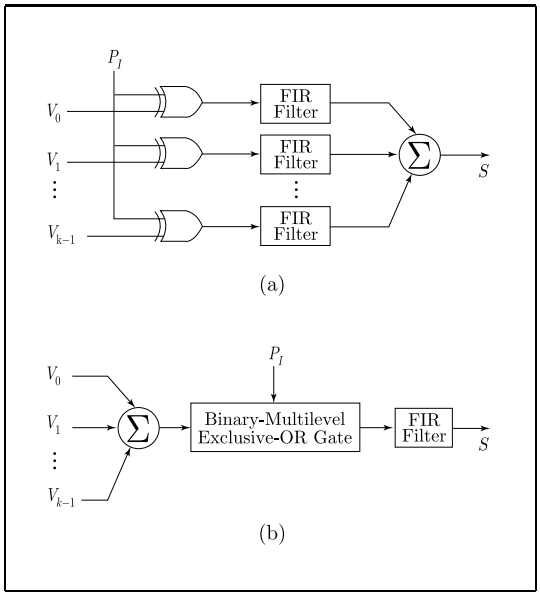

Fig. 3. An example to design a digital circuit using the MLO. (a) An example of BPSK modulation circuit, (b) Modified circuit of (a) using the binary-multilevel exclusive-OR operation.

and $\oplus$ denotes modulo-2 addition that is implemented with the binary exclusive-OR gate. Using equation (8) and the linearity of each operation in (9), we may rewrite (9) as

$$S = \sum_{i=0}^{k-1} G_i \; FIR\{P_I + V_i - 2P_I V_i\}$$
$$= FIR\left\{EXOR\left(P_I, \sum_{i=0}^{k-1} G_i V_i\right)\right\}, \quad (10)$$

where $EXOR(\ )$, whose first argument has binary logic value and the second argument has a multilevel logic value because of the arithmetic addition, denotes binary-multilevel exclusive-OR logic operation that is given by letting any one of its two input logic units in (6) be binary. This binary-multilevel exclusive-OR logic operator can be easily implemented as shown in Fig. 4. The design complexity of this operator is dominantly dependent on the subtractor and is not so high than that of a binary gate. In this figure, the (radix-1)'s complement means the multlevel NOT operator defined in (6). The switch can be implemented by the 2-to-1 multiplexer, indicated on the upper line, when the binary input P_I is the logic "1" and the lower line when P_I is the logic "0".

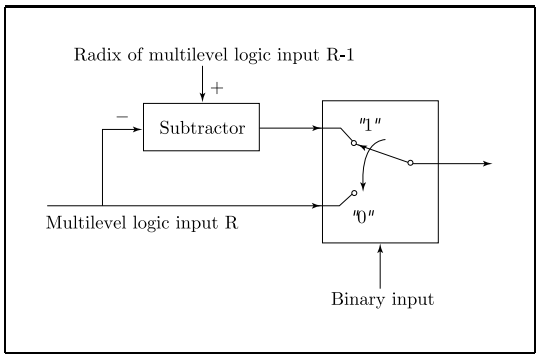

Fig. 4. Binary-multilevel exclusive-OR logic operator.

By using this binary-multilevel exclusive-OR operator, we can modify the circuit shown in Fig. 3(a) into that shown in Fig. 3(b) because (9) and (10) are equivalent, producing the same results. For example, assume that $k = 3$, $V_1 = (100110101)$, $V_2 = (011001010)$, $V_3 = (110101100)$, $P_I = (010110010)$. Then both circuits of Fig. 3 output the same result (211122221).

Notice that Fig. 3(a) contains k FIR filters, k binary exclusive-OR operators, k multipliers, and one arithmetic adder as opposed to Fig. 3(b) that contains only one FIR filter, one multilevel exclusive-OR operator, k

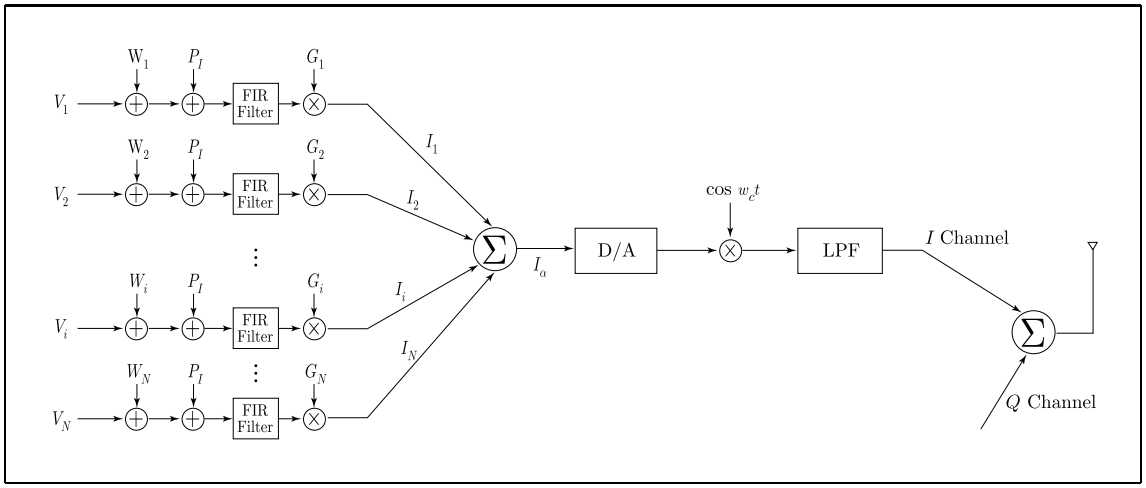

Fig. 5. Channel signal flow in a sector of the conventional BSM.

multipliers, and one arithmetic adder. Also while individual inputs to the arithmetic adder in Fig. 3(a) are to be represented by multiple bits to maintain the resolution given by the FIR filter coefficients, those in Fig. 3(b) require just one bit resolution because the circuit of Fig. 3(b) employs binary logics. As an example, if each FIR filter of Fig. 3(a) outputs 8-bit filtered data, Fig. 3(a) requires k 8-bit additions whereas the arithmetic adder in Fig. 3(b) requires only k 1-bit additions, thus substantially simplifying its operation. It is easier and simpler to use Fig. 3(b) than Fig. 3(a) because Fig. 3(b) requires less components and lower speed processing.

Fig. 3 is a simple example showing improvement of design efficiency achieved by using a binary-multilevel exclusive-OR operation that is a special case of multilevel exclusive-OR of MLOs. We may get similar results for many other applications involving AND, OR, NOT operation.

The MLOs we defined are not commutative because one of two input logic of each operator may not be equal to the other. Commutativity holds only when two input logics are identical, i.e., $A = B$ in (6).

IV. DESIGN OF BSM USING THE MLO CONCEPT

The purpose of this paper is the elimination of redundancy which may reside in the conventional DS/CDMS BSM system. As an example of redundancy elimination trial, location of FIR filter in Fig. 2 can be considered. Simply applying linear system theory to the Fig. 2, it is possible to replace all FIR filters in Fig. 2 with two filters after the digital combiner for each sector. And also, the section 2 in the

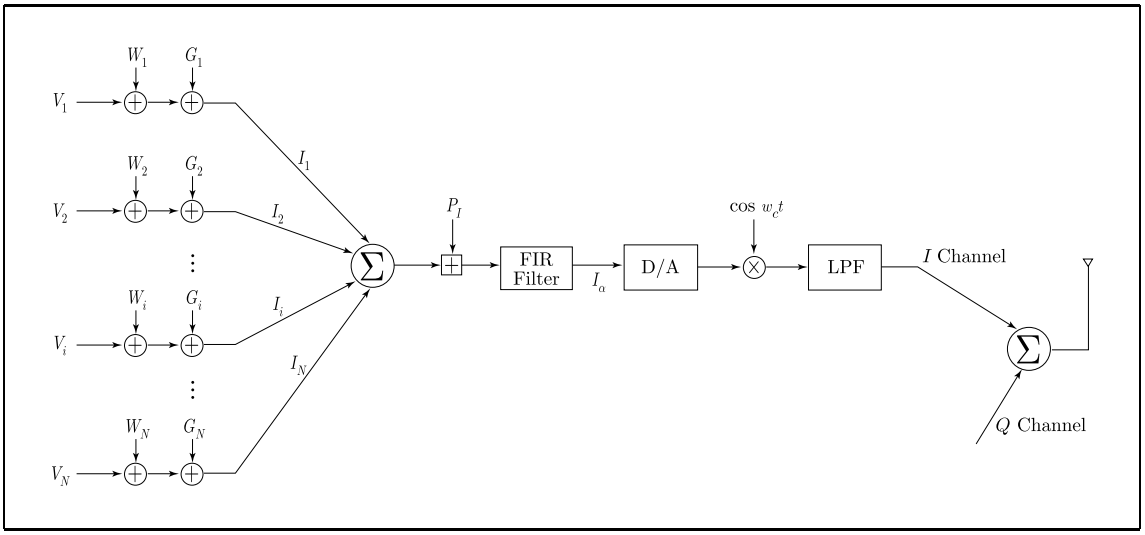

Fig. 6. Channel signal flow in the modified structure.

Fig. 2 is duplicated for the purpose of support the inter-sector softer handoff [1]. This duplicated section is needed only when inter-sector softer handoff is operating. Therefore, when a user is not in the handoff region, the duplicated section in Fig. 2 is redundant. This redundancy can be eliminated by using MLO.

To apply the MLO concept to the conventional BSM design, we review the structure of the 3-sectorized BSM shown in Fig. 2. The I-channel data flow of the alpha sector is taken and shown in Fig. 5. The output of digital combiner (i.e., the summation sign) I_α may be written

$$I_\alpha = \sum_{i=1}^{N} G_i \, FIR\{(V_i \oplus W_i) \oplus P_I\}, \qquad (11)$$

where G_i denotes the gain factor of the signal to i-th user, V_i denotes the power-punctured signal to be transmitted to i-th user, P_I denotes I-channel PN spreading sequence, W_i denotes the Walsh code assigned to i-th user, N is the total number of users in the alpha sector, and $FIR\{\ \}$ means FIR filtering. Similarly, the output of the digital combiner in the Q-channel Q_α, is given by

$$Q_\alpha = \sum_{i=1}^{N} G_i \, FIR\{(V_i \oplus W_i) \oplus P_Q\}, \qquad (12)$$

where P_Q is the Q-channel PN spreading sequence.

Using the above theorem and the linearity of the operators, we can rewrite (11) and (12) as

$$I_\alpha = FIR\left\{EXOR\left(P_I, \sum_{i=1}^{N} G_i(V_i \oplus W_i)\right)\right\},$$
$$Q_\alpha = FIR\left\{EXOR\left(P_Q, \sum_{i=1}^{N} G_i(V_i \oplus W_i)\right)\right\}. \qquad (13)$$

The expression of I_α in (13) may simply be implemented by the circuit shown in Fig. 6.

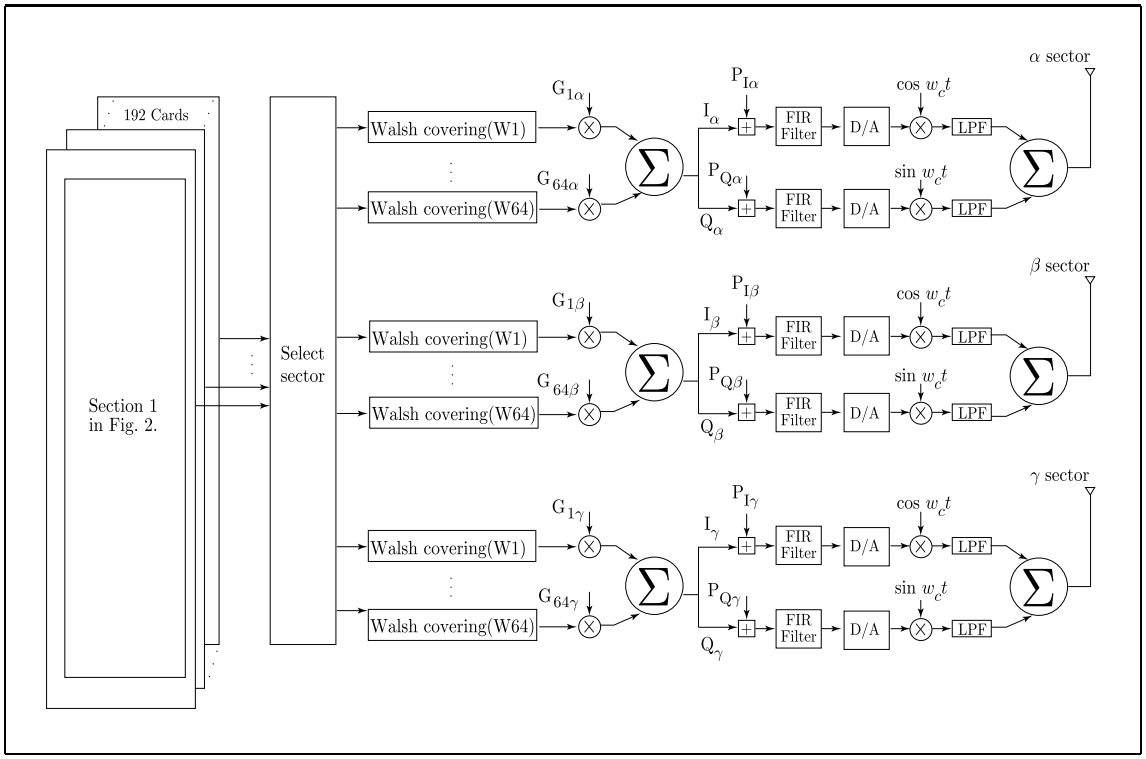

Fig. 7. Modified structure for CDMA BSM.

Apparently, the logic circuit in Fig. 6 contains smaller number of FIR filters and spreaders and thus is simpler than that in Fig. 5.

Using the circuit transforms of Fig. 5 to Fig. 6, we may now convert the conventional BSM structure of Fig. 2 to a simpler structure of BSM. The result is shown in Fig. 7. It has only 6 FIR filters, 6 spreaders, and 3N Walsh covers, while the conventional BSM structure has 12N FIR filters, 12N spreaders, and 6N Walsh covers. As an example, when a 64-ary Walsh cover is used (i.e., $N = 64$), the circuit of Fig. 7 has 6 FIR filters, 6 spreaders, and 192 Walsh covers, whereas the conventional BSM has 768 FIR filters, 768 spreaders, and 384 Walsh covers. The complexity of the new structure is reduced to less than 1 % of the conventional CDMA BSM for both the spreader and FIR filter, and 50 % for Walsh covering. The new structure also involves relatively low-speed digital combining.

Because the input logic of FIR filter in Fig. 2 is confined to binary and that in Fig. 7 is multilevel logic, it is more simple to implement FIR filter in Fig. 2 than in Fig. 7. But since the input of FIR filter in Fig. 7 is not real value but integer value, it can be imple-

mented by using shift register and adder instead of multiplier. Hence, it can be stated that hardware complexity increment by a FIR filter element is not so much.

V. CONCLUSIONS

In this paper, we defined MLOs and showed that multilevel logic exclusive-OR operation can be formed by extending binary exclusive-OR operation. Further, by applying it to the conventional CDMA BSM, we achieved significant reduction of hardware complexity of the conventional CDMA BSM as well as low digital circuit speed. The concept of MLO may be applied to those logic circuits that require heavy digital computations such as the areas of neural network.

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