A Low Distortion and Low Dissipation Power Amplifier with Gate Bias Control Circuit for Digital/Analog Dual-Mode Cellular Phones

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ABSTRACT

A power amplifier operating at 3.3 V has been developed for CDMA/AMPS dual-mode cellular phones. It consists of linear GaAs power MESFET's, a new gate bias control circuit, and an output matching circuit which prevents the drain terminal of the second MESFET from generating the harmonics. The relationship between the intermodulation distortion and the spectral regrowth of the power amplifier has been investigated with gate bias by using the two-tone test method and the adjacent channel leakage power ratio (ACPR) method of CDMA signals. The dissipation power of the power amplifier with a gate bias control circuit is minimized to below 1000 mW in the range of the low power levels while satisfying the ACPR of less than −26 dBc for CDMA mode. The ACPR of the power amplifier is measured to be −33 dBc at a high output power of 26 dBm.

I. INTRODUCTION

Digital mobile communication systems are developed to realize communication capabilities beyond the analog systems with greater spectral efficiency. During the transition from analog system to digital one, a mobile station should be able to place and receive calls in any cellular system, and vice versa. A digital modulation technique using QPSK signals for CDMA systems requires a more linear power amplifier than that required by the analog systems because spectral regrowth not only gives rise to interfering signals in other channels but also creates in-band interference that causes errors in the symbol vectors. The efficiency of the amplifier is very important for long time operation because most of power in a cellular phone is consumed in a power amplifier. Therefore, it is necessary to develop a power amplifier with high linearity and high efficiency for the dual-mode cellular phone [1]-[5].

For the CDMA mobile transmitter defined in the standard [6], the effective radiated power at the maximum output power should be within 23 dBm (lower limit) and 30 dBm (upper limit). Spurious emission level due to spectral regrowth in the mobile station should be less than -42 dBc/30 kHz for frequency offset greater than 885 kHz and -54 dBc/30 kHz for frequency offset greater than 1.98 MHz. There are two alternatives for power amplifier designers to satisfy such specifications. One method is using class A amplifiers operating at a reduced power level (backed off) far below saturation in order to keep distortion at an acceptable level. The drawback of this method is that the efficiency is low, so as to decrease talk time, and the thermal dissipation is high, so as to degrade the performance of the phone. The other way is using linearizers such as feedfoward [7], feedback [8]-[9], and predistortion [10], which make nonlinear power amplifiers linear. However, these are not suitable for low-cost and small-size power amplifiers in the mobile station.

Power dissipation and spectral regrowth are related to the output power levels of a power amplifier. In the range of low output power levels, signal distortion is low so that the specification of linearity can be satisfied, but efficiency is so low that high thermal dissipation is created and it results in reducing life time of a phone. However, in the range of high output power levels, the efficiency is high so that there are no problems in thermal dissipation, but the signal distortion gets worse that the specification of linearity can not be met. Therefore, it is very important to set the bias point using proper bias circuits. It is possible to improve both the efficiency and the IMD regardless of the output power levels if gate voltages corresponding to the power levels are controlled by a proper bias circuit. Bias control was proposed by Saleh *et al.*[11] and Simo [12], but never rigorously demonstrated for CDMA signals.

Characterization of spectral regrowth for the test of power amplifiers is often

replaced with intermodulation distortion (IMD). The most common way to specify the distortion is two-tone test method characterized by two closely spaced carriers. Since the amplitude and frequency distributions are markedly different from those of digitally modulated signals [13], the standard two-tone test can give misleading information about the amplifier's overall performance. Therefore, it is necessary to investigate the relationship between spectral regrowth of CDMA signals and the IMD of two-tone test.

In this work, we have developed a power amplifier operating at a supply voltage as low as 3.3 V for the CDMA/AMPS dual-mode cellular phone, which satisfies the linearity and the efficiency for CDMA mode, and simultaneously satisfies the output power and efficiency for AMPS mode. The relationship between the IMD and the spectral regrowth of the power amplifier has been investigated with the gate bias by using the two-tone test method and the adjacent channel leakage power ratio (ACPR) method of CDMA signals. This paper also describes a new method for designing high efficiency and linear power amplifier by dynamic control of the gate bias on the second MESFET using the input power level.

II. POWER AMPLIFIER DESIGN

In order to obtain good linearity for CDMA together with high output power (Pout) and high power-added efficiency

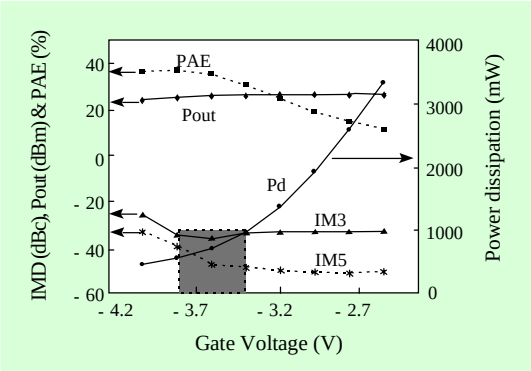

Fig. 1. The simulated results of total output power (Pout), power-added efficiency (PAE), third-order intermodulation distortion (IM3), fifth-order intermodulation distortion (IM5), and dissipation power (Pd) as a function of the gate bias (Vgs) on MESFET's.

(PAE) for AMPS mode in the 3.3 V operating power amplifier, it is important to develop highly efficient and linear power MESFET's with a supply voltage of 3.3 V. There are several sources causing intermodulation such as transfer characteristics and output impedance matching of power MESFET's. Most of the distortion arises from the nonlinear dependence of the drain current on gate bias [13]. A constant transconductance with gate bias can be obtained by a vertically stepped doping profile in the channel of the MESFET rather than a uniform doping profile [14]. In this work, a low-high doped channel structure grown by molecular beam epitaxy (MBE) was used in the fabricating power MESFET's to obtain the constant transconductance. Details on the fabrication and the performance of the MESFET's were described in elsewhere [15]-[17].

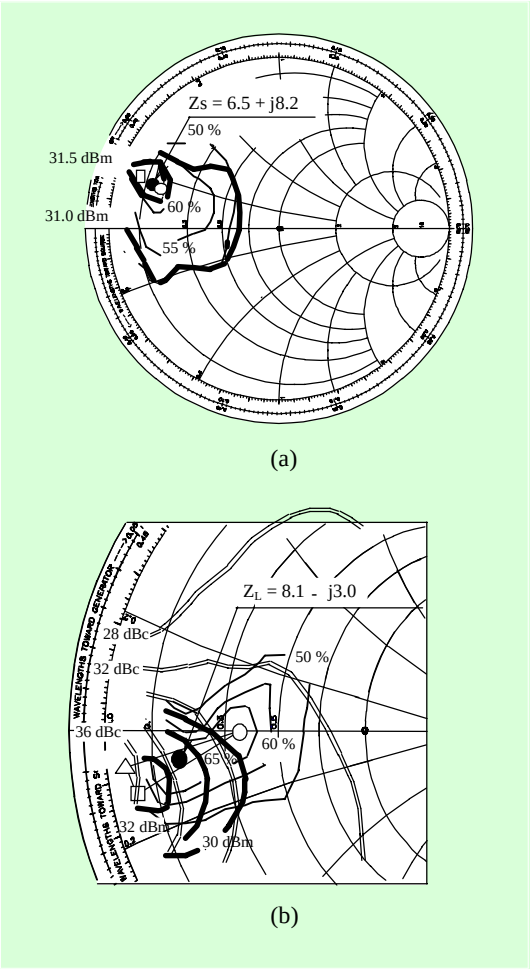

Fig. 2. The contours of output power, PAE, and IM3 of the 2nd stage MESFET (▬ : output power, — : PAE , ═ : IM3 at an output power of 26 dBm, □ : maximum output power, ○ : maximum PAE, △ : minimum IM3). (a) Source-pull contours. The optimum source (Zs) was determined by optimizing between the maximum output power and the maximum PAE. (b) Load-pull contours. The optimum load (Z_L) was determined by considering the maximum output power, the maximum, and the minimum IM3.

One of the important issues in designing a power amplifier for dual-mode applications is the selection of a gate bias point (Vgs) on a MESFET. The gate bias point has a large effect on the efficiency and the level of the intermodulation products. In order to determine the bias point, harmonic balance simulator was used to simulate the performance of a two-stage power amplifier in terms of total Pout, PAE, third-order intermodulation distortion (IM3), fifth-order intermodulation distortion (IM5), and dissipation power (Pd) as a function of Vgs on the power MESFET. The EEFET3 model provided by HP-EESOF was used for large signal simulation of the power MESFET. The harmonic terminations using short circuits were used in the output matching circuit composed of ideal components. The input and output matching circuits were re-tuned for each Vgs. Fig. 1 shows the simulated results of total Pout, PAE, IM3, IM5, and Pd as a function of Vgs. It was simulated at a drain voltage of 3.3 V, an input power of 2 dBm per each tone for average output power of 26 dBm, and the 442.5 kHz spacing of two tones. The simulated results show a weak sweet spot around the Vgs of −3.6 V, where the IM3 reduce to a level of −35 dBc. In addition to the IM3, the Pd related to the PAE is a key parameter to determine the gate bias point because the Pd causes the performance degradation of a phone. The dissipation power of around 1000 mW is evaluated to be appropriate, which is the value when the power amplifier is operating at a saturation output power of 31.5 dBm for maximum efficiency. As a

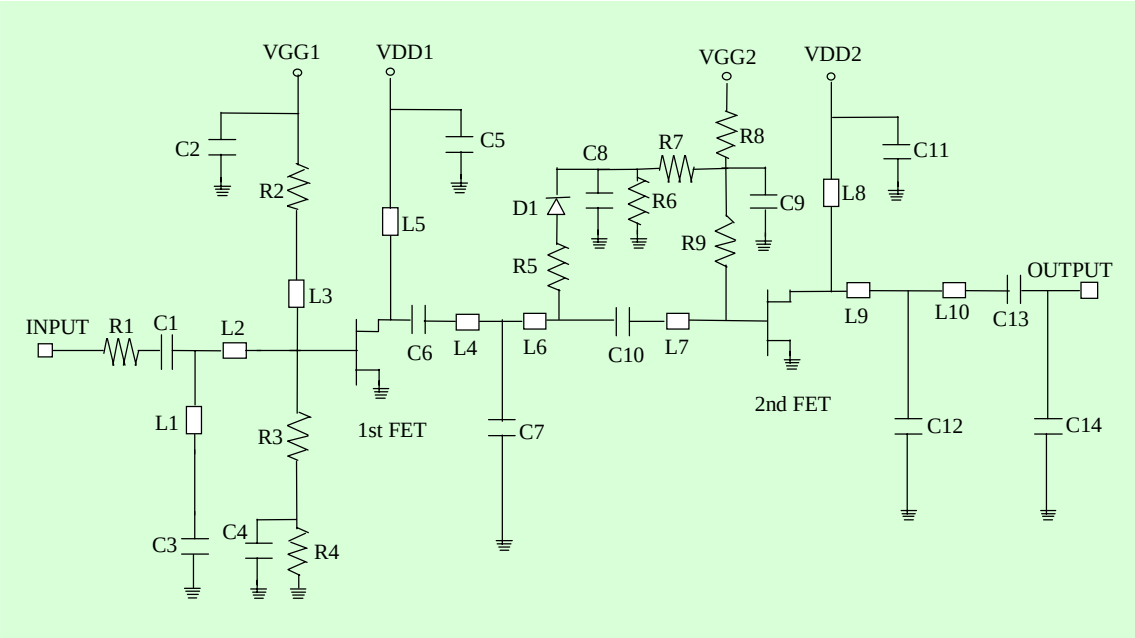

Fig. 3. Circuit diagram of the power amplifier for dual-mode cellular phones. A new gate bias circuit in the intersatge was designed to control the gate bias of the second stage MESFET with input powers.

result, the optimum gate voltage range is indicated by dotted box area in Fig. 1.

For the design of matching circuits after the gate bias selection, load and source impedances for both the output power and PAE were measured for the first stage and the second stage MESFET by the load-pull method using an input and an output tuner. Fig. 2 shows the contours of output power, PAE, and the IM3 at an output power of 26 dBm for the second stage MESFET. Source impedance was determined to be 6.5 + j8.2 Ω, optimizing between the maximum output power and the maximum PAE impedances. The optimum load impedance was 8.1 − j3.0 Ω, considering the maximum output power (32.1 dBm), the maximum PAE (68 %), and the minimum IM3 (−37 dBc). An output power of 31.7 dBm, a PAE of 66 %, and IM3 of −33 dBc were achieved at the optimum impedances.

The circuit diagram of the power amplifier for the dual-mode cellular phone is shown in Fig. 3. It consists of two stages to obtain a small-signal gain of more than 30 dB. The total gate widths of the first stage MESFET and the second stage MESFET are 3.2 mm and 16 mm, respectively. The matching circuits were designed to be matched to the optimum load and the optimum source impedances using a linear simulator. In the design of input circuits, the impedance matching to the input of the MESFET, stability, and losses were considered. A lowpass input circuit with series and shunt resistor for stabilization was

designed. A new gate bias circuit in the intersatge was designed to control the gate bias of the second stage MESFET with input powers. Average input powers to the second stage MESFET are detected by a series of resistor (R5) and diode (D1) and then charged in the capacitor (C8). The detector time constant is 10 ns. The voltage difference between the charged voltage and negative supply voltage (VGG2) is divided by R7, R8 and applied to the gate of the second stage MESFET. In the design of the second stage output circuit, the impedance matching to the output of the MESFET at a fundamental frequency, harmonic terminations at the second and the third harmonic frequencies, RF losses due to large impedance transform, and DC losses due to voltage drop by high current in the drain bias circuit were carefully considered. Fig. 4 shows the simulated and the measured impedance contours of the output matching circuit at the drain terminal of the second MESFET as a function of frequency. The designed output circuit is matched at a fundamental frequency and it has low impedances at the second and the third harmonic frequencies. This method resulted in improving both efficiency and linearity by preventing the drain terminal of the second MESFET from generating the harmonics. We designed the output circuit with simply minimized elements and high Q components for reducing RF losses. In order to reduce DC losses, the length and width of the drain bias line were designed to be shorter than quarter-wavelength and to be wide width of 300 μm. Fig. 5 shows a top view photograph of the dual-mode power amplifier with a size of 11.9 $\times$ 21.0 mm^2. The matching and bias circuits consist of microstrip transmission lines, chip capacitors and resistors (1005-type). Glass-based epoxy (FR-4) is used as a substrate to reduce total cost of the power amplifier.

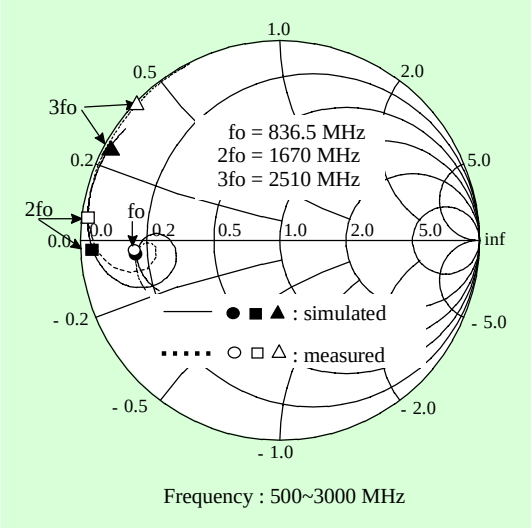

Fig. 4. The simulated and measured impedance contours of an output circuit at the drain terminal of the second MESFET as a function of frequency. Solid line shows the simulation result; Dashed line shows the measured result.

III. EXPERIMENTAL RESULTS

Fig. 6 shows the Pout, gain, and PAE of the power amplifier with a single tone for AMPS mode. It was measured with a gate bias control circuit at a drain voltage of 3.3 V and a center frequency of 836.5 MHz

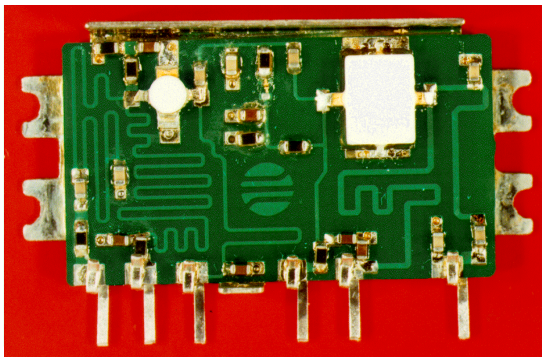

Fig. 5. Top view photograph of the dual-mode power amplifier with a size of 11.9 × 21.0 mm^2.

as a function of input power. The output power of more than 31.5 dBm and PAE of more than 60 % at a saturation point are satisfying the specifications which are the output power of 31 dBm and the PAE of 55 % required for AMPS mode. The measured performance of the amplifier with a gate bias control circuit for AMPS mode is comparable to that of a amplifier with single gate bias point [2]-[4].

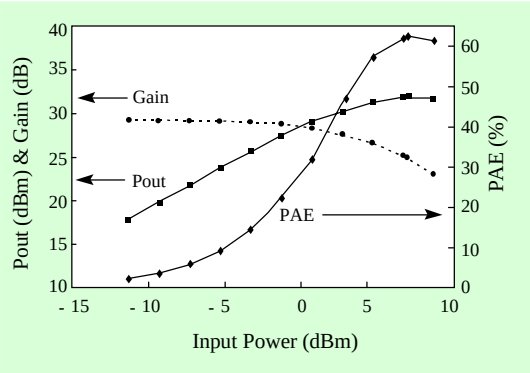

Fig. 6. Pout, gain, and PAE characteristics of the power amplifier with single tone measured at supply vol- tage of 3.3 V and a frequency of 836.5 MHz as a function of input powers.

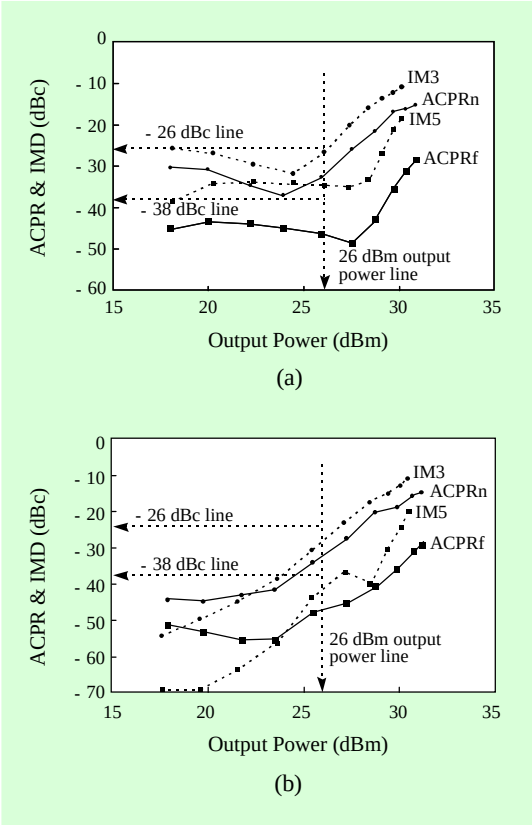

Fig. 7. Intermodulation distortions (IMD's) and adjacent channel leakage power ratios (ACPR's) of the power amplifier as a function of output power at gate bias of (a) VGG2 = −3.8 V and (b) VGG2 = −3.3 V.

The relationship between the IMD and the spectral regrowth of the power amplifier without a series of the R5, D1 as shown in Fig. 3 was investigated with the gate voltage (VGG2) on the second stage MESFET by using the two-tone test method and the ACPR method of QPSK signals using CDMA source (HP 8921A and HP 83203B). The IM3 and the IM5 were measured with a spacing of 442.5 kHz for the two-tone test method. The differences be-

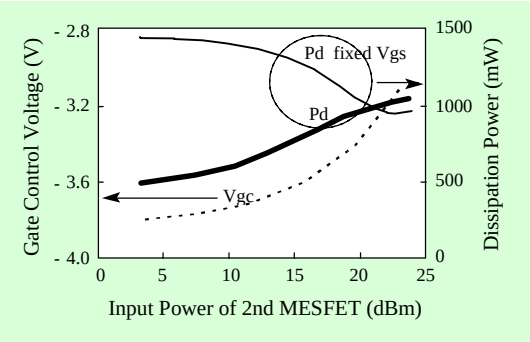

Fig. 8. Gate control voltage and dissipation power as a function of input power of the second stage MESFET. The Pd_fixed Vgs line means the dissipation power without gate bias control circuit at a fixed Vgs.

tween a level of center frequency (836.5 MHz) and a level of frequency offset of 885 kHz (ACPRn), and between a level of center frequency and a level of frequency offset of 1.98 MHz (ACPRf) were measured with a bandwidth of 1.23 MHz for the ACPR test. Fig. 7 shows the ACPR's and IMD's of the power amplifier at gate voltages of −3.8 V (lower limit) and −3.3 V (upper limit) as a function of output powers. The guide lines of −26 dBc and −38 dBc respectively correspond to −42 dBc/30 kHz for frequency offset of 885 kHz and −54 dBc/30kHz for frequency offset of 1.98 MHz required by the standard [6]. The IM3 and the IM5 at a low gate voltage of −3.8 V for an output of 26 dBm are higher than the ACPRn and the ACPRf by amount of more than 4 dB and more than 10 dB, respectively as shown in Fig. 7(a). This indicates that it is unreasonable to replace the spectral regrowth with IMD for lower gate bias vol- tage. The ACPRn of −3.8 V gate voltage is narrowly satisfying the specification of −26 dBc. As shown in Fig. 7(b) for a high gate voltage of −3.3 V, the IMD's are still higher than the ACPR's though the discrepancy between the IMD's and ACPR's are much close each other.

In the higher output power levels in Fig. 7, it is shown that the ACPRn and ACPRf in the slope aspect correlate to the IM3 and IM5, respectively. In the lower power levels, the behaviors of ACPR and IMD are attributed to variations of optimum impedances depending on operating points. The matching circuit can not provide gain slope compensation since the optimum impedances were determined by tradeoff between efficiency, power and IM3 at a bias point of 10 % Idss. The IMD of the two-tone test can be a tight specification for designing a digital power amplifier because IMD's are higher than ACPR's for high output levels regardless of gate voltage.

In order to improve both the efficiency for low power levels and the linearity for high output power levels, we designed a new gate bias circuit using a diode which dynamically controls the gate voltage on the second stage MESFET with the average input powers of the second stage. The input signals before the input circuit of the second stage MESFET are detected by a series of the D1, R5 and then charged in the C8 in Fig. 3. The voltage difference between the charged voltage and the VGG2 of −5 V is divided by a shunt of R7, R8 and then applied to the gate of the second stage MESFET in accordance to the

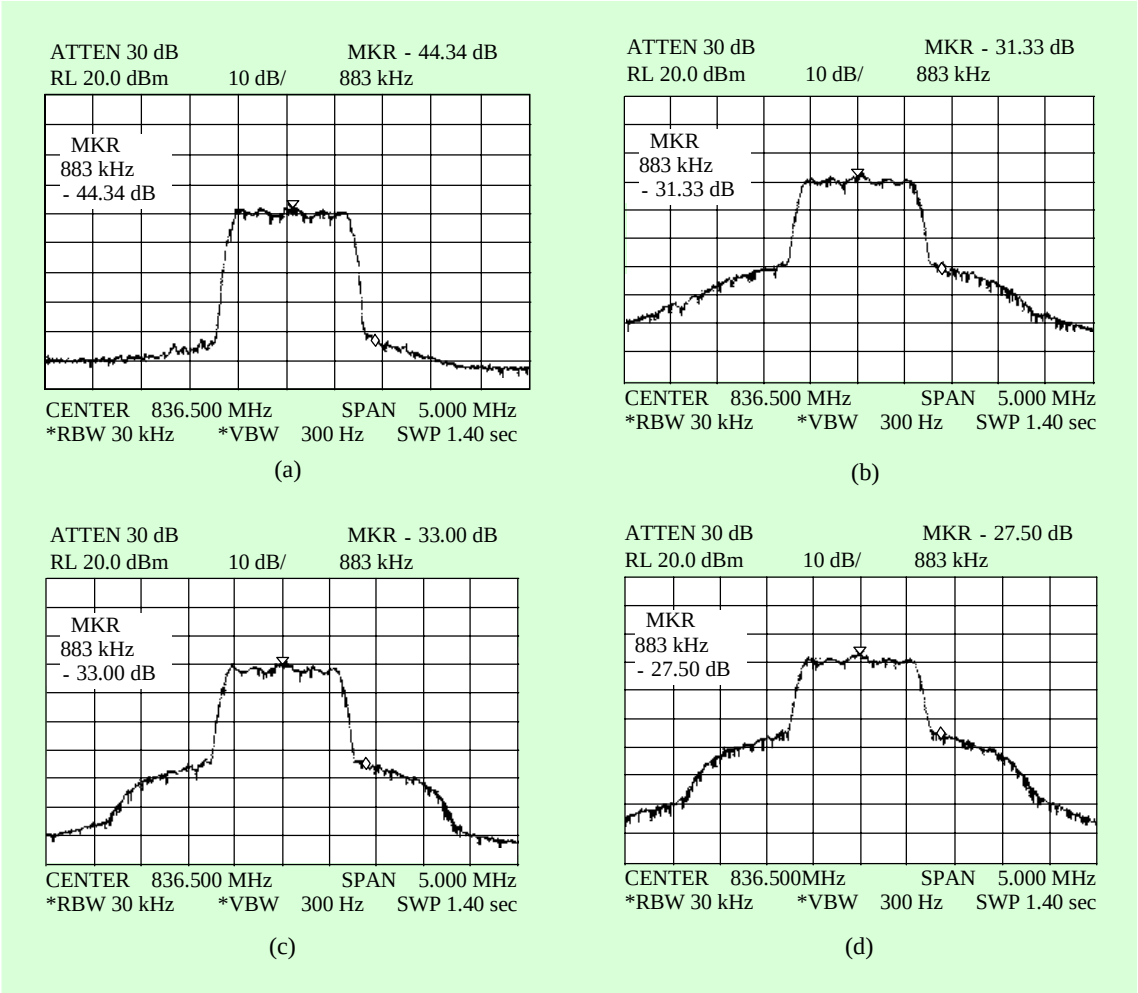

Fig. 9. Spectra of (a) the CDMA source from the equipment, (b) the CDMA signal passed the amplifier without gate bias control at a channel power of 26 dBm, (c) the CDMA signal passed the amplifier with gate bias control at a channel power of 26 dBm, and (d) the CDMA signal passed the amplifier with gate bias control at a channel power of 28 dBm.

input power levels in the second stage. As shown in Fig. 8, the gate control voltage of the second stage MESFET increases to obtain good linearity at high input power levels and decreases to minimize the dissipation power of below 1000 mW at low input power levels while maintaining ACPRn of below than −26 dBc. The dissipation power of the power amplifier using gate bias control is remarkably reduced for the low output powers compared with the amplifier using constant gate bias.

Fig. 9 shows the spectra of (a) the CDMA source from the equipment, (b) the

CDMA signal passed the amplifier without a gate bias control circuit at a channel power of 26 dBm, (c) the CDMA signal passed the amplifier with a gate bias control circuit at a channel power of 26 dBm, and (d) the CDMA signal passed the amplifier with gate bias control circuit at a channel power of 28 dBm. The ACPRn's are dominant spectral regrowth, which are −31.3 dBc in Fig. 9(b), −33 dBc in Fig. 9(c), and −27.5 dBc in Fig. 9(d), respectively. At this time, the efficiencies were measured to be (b) 30.8 %, (c) 27 %, and (d) 31 %. The spectral regrowth at an output power of 26 dBm is suppressed by amount of 1.6 dB using the gate bias control circuit though the efficiency is sacrificed to somewhat. It is demonstrated in Fig. 9(d) that the channel power can be realized up to 28 dBm by using the gate bias control circuit while satisfying the specifications of CDMA mode.

In the range of low output power levels, the dissipation power is reduced by lowering gate bias of the amplifier as long as the ACPR's are satisfying the specifications. In the range of the high output power levels, the ACPR's are improved by raising the gate bias even though the dissipation power increases a little. Therefore, we can improve the efficiency for lower power levels and the linearity for higher power levels by the dynamic control of the gate vol- tage of the power amplifier. These results are evaluated to be good enough because the efficiency is the most important parameter for the low output power levels while the ACPR's are the most important parameters for the high output power levels.

IV. CONCLUSIONS

A power amplifier operating at a supply voltage as low as 3.3 V has been developed for CDMA/AMPS dual-mode cellular phones. It consists of linear GaAs power MESFET's, a gate bias control circuit, and an output matching circuit which prevents the drain terminal of the second MESFET from generating the harmonics. The relationship between the IMD and the spectral regrowth of the power amplifier has been investigated with gate bias by using the two-tone test method and the ACPR method of CDMA signals. The IMD's of the two-tone test are higher than the ACPR's of the ACPR test so that the IMD's of the two-tone test can be safe guide lines for designing a digital power amplifier. By using a gate bias control circuit, the dissipation power was minimized to below 1000 mW for the lower power levels while satisfying the specifications of the CDMA mode. The ACPRn was improved to be −33 dBc for an output power of 26 dBm. As a result, the efficiency in the range of low output power levels and the linearity in the range of high output power levels can be improved by the control of the gate bias of the power amplifier.

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