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Variations of Interface Potential Barrier Height and Leakage Current of (Ba, Sr)TiO_3 Thin Films Deposited by Sputtering Process

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Variations of the leakage current behaviors and interface potential barrier height (Φ_B) of rf-sputter deposited (Ba, Sr)TiO_3 (BST) thin films with thicknesses ranging from 20 nm to 150 nm are investigated as a function of the thickness and bias voltages The top and bottom electrodes are dc-sputter-deopsited Pt films. Φ_B critically depends on the BST film deposition temperature, postannealing atmosphere and time after the annealing. The postannealing under N_2 atmosphere results in a high interface potential barrier height and low leakage current. Maintaining the BST capacitor in air for a long time reduces the Φ_B from about 2.4 eV to 1.6 eV due to the oxidation. Φ_B is not so dependent on the film thickness in this experimental range. The leakage conduction mechanism is very dependent on the BST film thickness; the 20 nm thick film shows tunneling current, 30 and 40 nm thick films show Schottky emission current.

Key words : (Ba, Sr)TiO_3, Pt, Barrier height, Leakage current, Tunneling, Schottky conduction

I. Introduction

(Ba, Sr)TiO_3 (BST) thin film attracts great interest as a new dielectric material in capacitors for the next generation ultralarge scale intergrated dyamic random access memories (ULSI DRAMs), such as 1 giga bit or 4 giga bit density DRAMs not only from research institutes but also from semiconductor industries because of its high dielectric constant, low dielectric loss and low leakage current level.[1-3] It is understood that the adoption of BST film can greatly reduce the storage node height of the future ULSI DRAMs due to its large dielectric constant, which largely facilitate the photolithographic process of the DRAM fabrication. DRAM capacitors have used SiO_2/Si_3N_4 (ON) bi-layered thin films as the dielectric material and doped-polycrystalline silicon as the electrodes. However, the new dielectric material requires other electrode material than the doped poly-Si which is very resistant to oxidation or conductive after oxidation, otherwise the capacitance of the capacitor can not be high enough because of formation of the interfacial oxide film which has small dielectric constant. The most promising electrode material is platinum (Pt)[3-5] or conducive oxides, such as RuO_2[2] and IrO_2,[6,7] even though a proper etching technology is under development yet for the Pt case,[8] and high leakage current is obtained for the conductive oxide case.[2]

It seems that more attention should be paid to the interfaces between the BST thin film and Pt electrodes when the BST film thickness is smaller than 100 nm to understand the leakage current mechanism and to improve the leakage characteristics of the capacitor, because when the insulating oxide film thickness is very small the characteristics of charge transport across the interfaces with electrodes become more dominant.

As elucidated by T. Mihara and H. Watanabe,[9] the real leakage current flow through metal-ferroelectric-metal (MFM) or metal-high dielectric insulator-metal (MIM) capacitors can reasonably be classified as the Schottky emission current or Poole-Frenkel emission current when the applied electric field strength is larger than about 0.5 MV/cm. The leakage current of the capacitors in an applied electric field strength less than 0.5 MV/cm, which is about the normal operating electric field strength range of DRAM cells, is attributed to the relaxation or absorption current.[5] The relaxation current occurs during the charging process of the capacitor, which is not a real leakage current flowing from one electrode to the other. The relaxation current is linearly proportional to the bias voltage but the real leakage current, which is the emission current, increases very rapidly with increasing bias voltage. Therefore, suppression of the emission current not to occur in the normal operation voltage range of the devices is very important for the stable operation of the devices.

The authors showed that the electronic emission mechanism of Pt/$SrTiO_3$/Pt capacitor tends to change from the Schottly emission to Poole-Frenkel emission with decreasing the $SrTiO_3$ film thickness.[10] And capacitors having BST as the dielectric material are also fabricated and their excellent dielectric properties are already reported elsewhere.[11,12]

In this paper, the leakage current behavior of the capacitor by the electronic emission process is mainly studied

when the BST film thickness ranges from 20 nm to 150 nm. The electrical barrier properies of the top and bottom electrode interfaces are studied along with the variations of the film thickness.

II. Experimental Procedures

Planar Pt/BST/Pt capacitors were fabricated by sequential deposition of dc-sputtered Pt, rf-sputtered BST and dc-sputtered Pt thin films on thermally oxidized, 6"-diameter (100) Si wafers. Bottom Pt electrodes were deposited at 400°C and Ar sputtering gas pressure of 6mTorr, which is one of the experimentally determined hillock-free deposition conditions of the Pt thin films. BST thin films were deposited at temperatures ranging from 450°C to 600°C, and with thicknesses ranging from 20 nm to 150 nm under a sputtering gas, which was composed of 80% Ar and 20% O_2, with pressure of 10 mTorr. A sintered target of 50/50 [Ba]/[Sr] was used. A small sputtering power was used to minimize the surface damage of the BST film during the top electrode deposition. The wafers were not intentionally heated during the top electrode deposition. Capacitors with area of $8\times10^{-4}cm^2$ were defined by a dry etching technique unilizing a photo resist mask. The capacitors were annealed at 750°C in flowing oxygen and nitrogen atmospheres after the top electrode fabrication.

Capacitance and leakage current density were measured using a HP-4284 LCR meter at 10 kHz and a HP-4145B semiconductor parameter analyzer, respectively. The leakage current density was measured at temperatures ranging from room temperature (RT) to 165°C. A staircase shaped dc-bias voltage, with 0.05 V high and 1 sec long at each voltage step, was applied to the top electrode while the bottom electrode was grounded.

III. Results

Figure 1 shows the variations of logarithm of leakage current density (Log(J)) of the BST thin films which are 40 nm thick and deposited at 570°C and postannealed at 750°C for 30 min under (a) O_2 and (b) N_2 atmospheres as a function of square root of the applied electric field strength ($\sqrt{E}$) at the measuring temperatures ranging from 55°C to 115°C.

J can be divided into two different types according to the applied field strength; one is the low field strength region where J is nearly independant of the E and the other is the high field strength region where the Log(J) increases linearly with $\sqrt{E}$. J in the low E region is known to be the polarization or relaxation current, which is not a true leakge current by the movements of conducting electrons from one electroode to other, whereas the J in the high E region is the true leakage current. The linear relationship between the Log(J) and $\sqrt{E}$ strongly implies that the conduction of the current is controlled by the field enhanced Schottky type electron emission at the interface between the BST and Pt or the Poole-Frenkel type electron emission within the BST film. The authors have reported that the conduction mechanism of the Pt/$SrTiO_3$/Pt capacitor is strongly dependent on the dieclectric thin film thickness.[10] In this Pt/BST/Pt capacitor case, the conduction mechanism can safely be assumed to be the Schottky type electron emission from the reasons discussed in the followings.

The transition point of E at which the conduction mechanism changes from the polarization to the emission decreases with increasing measuring temperature due to the increased emission current and almost constant polarization current. The emission current densities are also strongly dependent on the postannealing atmospheres as clearly seen from figure 1 (a) and (b). J of the film annealed under N_2 atmosphere is much smaller than that of the film annealed under O_2 atmosphere. We have already reported that the annealing under N_2 atmosphere is much more effective to reduce the emission leakage current than O_2 atmosphere.[11] The variations in

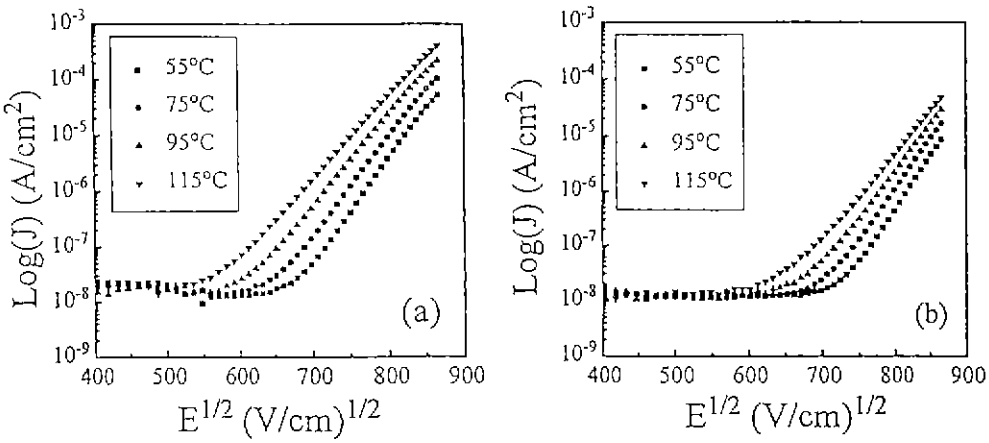

Fig. 1. Variations of log(J) of the 40 nm thick BST thin films deposited at 570°C and postannealed at 750°C for 30 min under (a) O_2 and (b) N_2 atmospheres as a function of $\sqrt{E}$ at the measuring temperatures ranging from 55°C to 115°c.

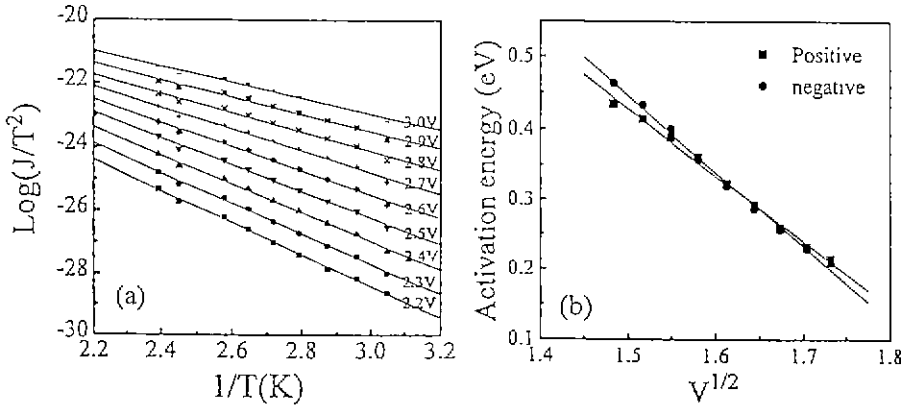

Fig. 2. (a) Variations of $\log(J/T^2)$ with 1/T, where the J was measured at voltages ranging from +2.2V to +3.0V, (b) activation energy vs. $\sqrt{E}$ plot obtained from Fig. 2 (a).

the emission current density with the E and temperature, and variation of the interfacial Schottky potential barrier height are studied in detail by plotting the measured emission current density in a way shown in figure 2.

The variations of $\mathrm{Log}(J/T^2)$ with 1/T, where the J was measured at voltages ranging from +2.2V to +3.0V with 0.1V interval, are shown in figure 2 (a). The sample capacitor comprises 40 nm thick BST film with Pt electrodes and was annealed at 750°C for 30 min under N_2 atmosphere. As will be discussed later, the elapsed time after taking out the sample from the annealing atmosphere greatly affects the measured potential barrier height. Here, the measurement was performed within 12 hours after taking out the sample. The least squared linear fittings of the data at each measuring voltage fit very nicely to the experimental data and the reliability values of the fittings are more than 0.995.

The slopes of each graphs correspond to the activation energies for the electron emission at the bottom electrode interface as shown ineq. (1).[13]

$$\mathrm{Ln}(J/T^2) = (-q\Phi_B + \sqrt{(qE/4\pi\varepsilon_0\varepsilon_r)})/kT + \mathrm{Ln}(A^*) \quad (1)$$

where ε_0, ε_r, and A^* stand for the permitivities of vacuum, BST film and effective Richardson's constant, respectively. The slopes of each graph in figure 3 (a) correspond to $(-q\Phi_B+\sqrt{(qE/4\pi\varepsilon_0\varepsilon_r)})/k$. Therefore, the interfacial potential barrier height Φ_B can be obtained by plotting the activation energies obtained at different E vs. $\sqrt{E}$ and extrapolating the graph to E=0, figure 2 (b) shows the activation energy vs. $\sqrt{E}$ plot obtained from figure 2 (a) which reveals a nicely linear behavior. Φ_B of the top electrode interface can also be obtained by applying negative voltages to the top electrode in a way similar to figure 2 (a).

The Φ_B's of the top and bottom electrode interfaces of the Pt/BST/Pt capacitor, where the BST film was deposited at 570°C and postannealed at 750°C under O_2 and N_2 atmospheres. are obtained by the method just described. The Φ_B strongly depends on the annealing atmosphere and varies with the time after the annealing as shown in figure 3. In figure 3 the x-axis corresponds to the time elapsed during which the sample was in air at room temperature after the sample was taken out from the annealing furnace.

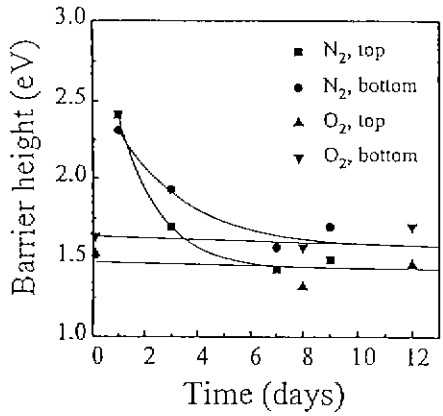

Fig. 3. Variations of the Φ_B with time after the postannealing. The samples were annealed under N_2 and O_2 atmospheres.

There are several things to be noticed in figure 3. First of all, the Φ_B is higher when the capacitor is annealed under N_2 atmosphere than that of O_2 for a certain period of time after the annealing, which corresponds well to the results shown in figure 1 (a) and (b). However, Φ_B's of the bottom electrode of the samples annealed under N_2 and O_2 eventually merge to a certain constant value after a long time, which is about 9 days, because the Φ_B's of the sample annealed under N_2 decreases with time but the Φ_B's of the sample annealed under O_2 atmosphere are almost irrespective of the time. The constant values of the Φ_B are about 1.6 eV and 1.5 eV for bottom and top electrode interfaces, respectively, whereas the Φ_B's within a day after the annealing under N_2 atmosphere are 2.3 eV 2.4 eV. When the sample was annealed again under N_2 at-

mosphere after the Φ_B decreased to the saturation value, the Φ_B almost recovers its initial value although the data is not included in figure 3.

The second point to be notified is that the relative variations of Φ_B's under positive and negative bias conditions which correspond to the Φ_B's of the bottom and top electrode interfaces, respectively. The sample annealed under O_2 atmosphere shows a constantly larger value of Φ_B at bottom electrode interface than that of the top interface but the sample annealed under N_2 atmosphere shows larger Φ_B at the top electrode interface than that of the bottom electrode interface just after the annealing. However, the Φ_B of the top electrode interface decreases faster than that of the bottom electrode interface with time so that only after about 1 day the bottom electrode interface shows a larger Φ_B than that of the electrode interface.

The interfacial potential barrier heights of the films deposited at 490°C with different thicknesses are measured and the results are shown in figure 4 Here, Φ_B's of the 30 and 40 nm thick films are calculated for the whole trmperature range and those of the 70 and 150 nm thick films are calculated at temperatures ranging from 100°C to 160°C.

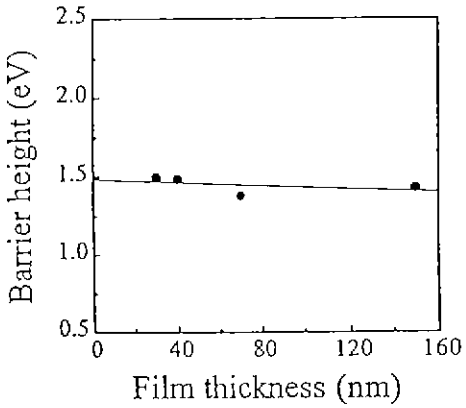

Fig. 4. The variation of the Φ_B with the BST film thickness.

However, Φ_B's of the bottom electrode interface of the thicker films can not be estimated because of the easy breakdown under the positive bias conditions so that only the Φ_B's of the top electrode interfaces are plotted in figure 4.

It is interesting to notice that Φ_B's are almost independent of the film thickness, which is about 1.45 eV in this experiment. The Φ_B's are measured at about 12 hours after the annealing except for the 70 nm thick film in which the Φ_B was measured after 3 days so that the Φ_B of that film is estimated to be a little bit lower than what it should be. Another point to be noticed from figure 4 is that absolute value of the Φ_B's are much smaller than that of the film deposited at 570°C shown in figure 3. The reason for the variation of the Φ_B with the deposition temperature is under study now.

The 20 nm thick film shows a different leakage current behavior not only in the high field region but also in the low field region from those of the thicker films. We assumed that the tunneling current starts to appear at this film thickness and plotted the variation of J with E according to the formula of electron tunneling through the thin insulator.[13] J increases rather slowly in the low voltage region and much rapidly in the high voltage region where the absolute transition voltage is about 1.3 V irrespective of the bias polarity.

Figure 5 (a) shows the variation of the Log(J) with E which shows the true tunneling in the low field region, and figure 5 (b) shows that of the $Log(J/E^2)$ vs. 1/E in the high field region, which corresponds to the Fowler-Nordheim tunneling.[13] Both of the graphs show a good linearity supporting the tunneling model of the 20nm thick film. Furthermore, the transition voltage from the true tunneling to Fowler-Nordheim tunneling is slightly smaller than the interfacial potential barrier height estimated from the thicker films, which seem to be very reasonable. Scott et al.[11] have shown the same variation of the leakage conduction mechanism with E.

However, it can not be unequivocally stated that the 20 nm thick film shows the tunneling current behavior in

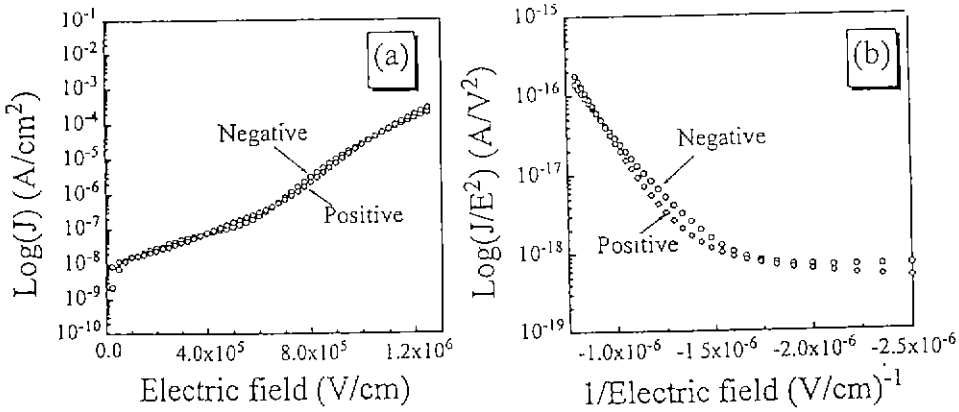

Fig. 5. Variations of (a) log(J) with E and (b) $log(J/E^2)$ vs. 1/E of the 20 nm thick film

the high E region only from the Fowler-Nordheim tunneling plot shown in figure 5 (b) because the 30 nm thick film also show a very linear behavior in its Log(J/E^2) vs. 1/E plot in the high field region as shown in figure 6. Therefore, we measured the variation of J as a function of the applied voltage at temperatures ranging from 40°C to 130°C of the 20nm thick film as shown in figure 7 (a). J increases very slowly with temperature in the low voltage region and shows a maximum increases rate at about 1.75 V as shown in figure 7 (b), which is a typical characteristics of the tunneling conduction.

Now we assumed that the 20 nm thick film also shows the Schottky emission behavior in a voltage region from 1.5 V to 2.5 V and estimated the activation energies at each voltages and Φ_B. The 20 nm thick film shows a much smaller and constant activation energy of about 0.14 eV, irrespective of the applied voltage. This is a completely different behavior from those of the BST films thicker than 30 nm. Therefore, the leakage current mechanism of the 20 nm thick film is not the field enhanced thermally activated process over the interfacial poterntial barrier, which is the Schottky emission, but the Fowler-Nordherim tunneling.

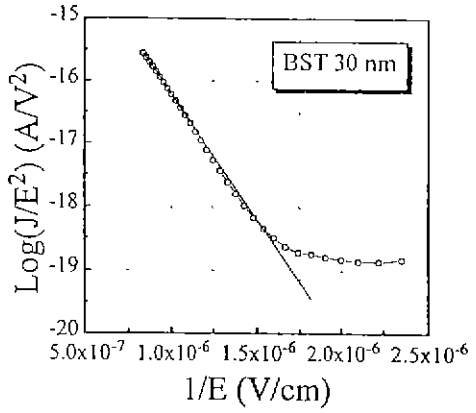

Fig. 6. Fowler-Nordheim plot of J of the 30 nm thick BST film.

Finally, thicknesses of the interfacial carrier depletion layers (t_d) are estimated from the variation of apparent dielectric constant of the BST film with the total film thickness (t_t). It is well known that the conducting electrons in the insulating thin film transfer to the metal with large work function Φ_m when the metal-insulator contact is made to equilibrate the Fermi levels of the two material.[13] The carrier depletion layer is formed by this movements in the insulating film at the interface. The thickness of the depletion layer (t_d) is proportional and inversely proportional to squaren roots of the interfacial potential barrier height ($\sqrt{\Phi_B}$) and carrier concentration ($(\sqrt{n})^{-1}$), respectively, as shown in eq. (2). Therefore, the carrier concentration can be inferred from the t_d if the t_d can be known by some other method because the Φ_B was measured as shown in Fig. 4.

$$t_d = (2\varepsilon_0 \varepsilon_r \Phi_B / qn)^{1/2} \quad (2)$$

The authors have shown that the t_d can be estimated from the measured dielectric constant with the dielectric film thickness in case of the Pt/$SrTiO_3$/Pt capacitors[10]. The variation of the dielectric constant (ε_r) with the BST film thickness (t_t) can be expressed as eq. (3) when t_t is larger than $2t_d$.

$$\varepsilon_r = \frac{\sqrt{k}\varepsilon' t_t}{\sqrt{k}(t_t - 2t_d) - \sqrt{\varepsilon'} \ln((\sqrt{\varepsilon'} - \sqrt{k}t_d)/(\sqrt{\varepsilon'} + \sqrt{k}t_d))} \quad (3)$$

where ε' is the bulk dielectric constant of the dielectrics and k is defined as $\varepsilon'(1-\beta)/t_d^2$, and β is defined as $\varepsilon''/\varepsilon'$, where ε'' is the dielectric constant of the BST layer in contact with the electrode.

Figure 9 shows the variation of ε_r of the Pt/BST/Pt capacitors with the variation of the BST film thickness; the circular dots represent the experimental data and and the line does the calculated value using eq. (3) by assuming t_d of 13 nm, ε' of 650 and β of 0.1. The calcuation matches very well with the experimental data. The carrier concentration estimated from eq. (2) using t_d of 13 nm and Φ_B of 1.45 eV is about $3\times10^{20}cm^{-3}$. Scott et al.[16]

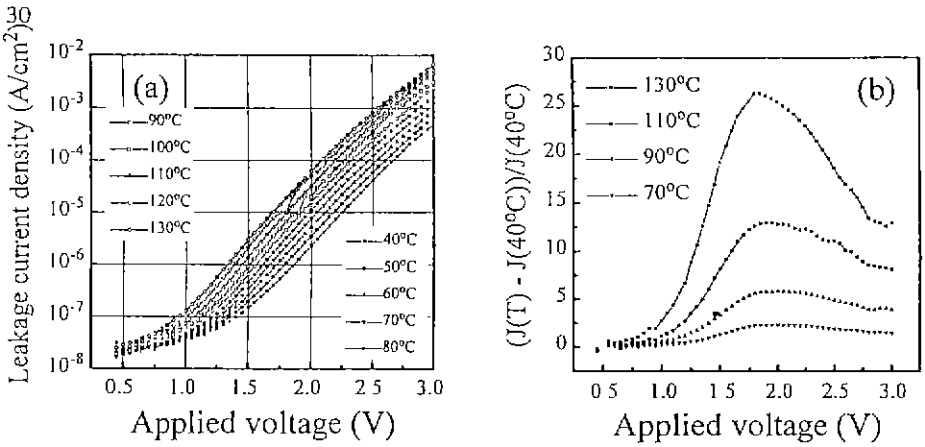

Fig. 7. The variation of J of the 20 nm thick BST film; (a) log(J) vs. V and (b) ratio of increase in J with temperature.

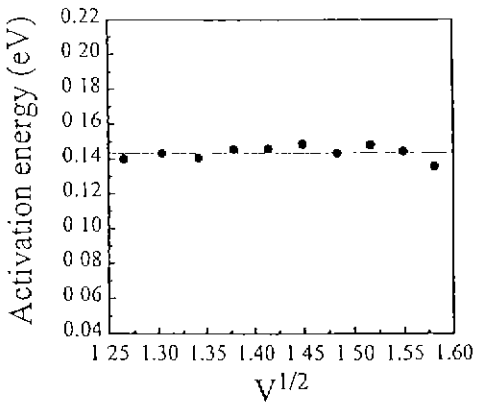

Fig. 8. Variation of activation energy of the 20 nm thick BST film with V.

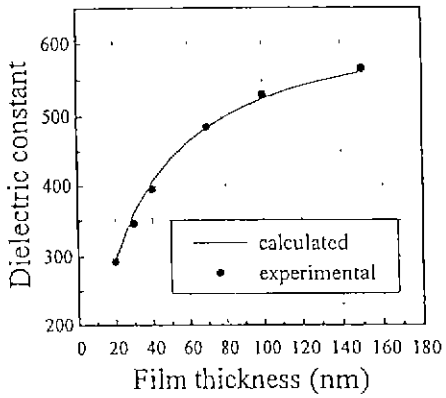

Fig. 9. Variation of ε_r of the Pt/BST/Pt capacitors with the variation of the BST film thickness.

have reported a similar value of t_d in case of the Pt/PZT/Pt capacitor.

IV. Discussions

Φ_B of the metal-insulator interface is strongly affected by the image forec effect[13] and various interface states, which trap the carriers.[16] The image force effect and interface states result in a smaller Φ_B value than the ideal Φ_B value of $\Phi_m - \chi$, where Φ_m and χ are the work function of the metal and the electron affinity of the insulator. In this case the measured Φ_B values, shown in figure 3 and figure 4 are much smaller than the ideal value of about 3.65 eV for Pt/BST interface. The carrier concentration also affect the Φ_B as well as above two factors.

The carrier concentration and the interface state density are dependent on the process conditions, such as the temperatures, atmospheres of the deposition and postannealing.

In this BST thin film case, the crystalline quality, grain size, composition are almost independent of the atmospheres during the postannealing or the time after the postannealing. Therefore, we believe that the image force and interface state density are almost independent of the annealing atmosphere. However, the annealing atmosphere must strongly affects the carrier concentration because the oxidation or reduction of the BST film decreases or increases the conducting electron density according to the following reduction-oxidation reaction eq. (4).

$$O_o = V_o + 1/2O_2 \text{ (gas)} \quad (4)$$

when the BST film is reduced by the annealing under N_2 atmosphere, the conducting electron density increases by the forward reaction of eq. (4). In that case the Φ_B increases due to the increased electron density However, during the sample is maintained in the air atmosphere after the annealing, the oxidation from the top surface of BST occurs and the Φ_B decreases to the saturation values shown in figure 3. Let us note that platinum can not serve as the barrier against oxygen diffusion. It is interesting that the Φ_B at the top electrode interface decreases more rapidly than that of the bottom electrode interface, whereas the Φ_B of the top electrode interface was initially larger than that of the bottom electrode interface. We believe that this is due to the difference in oxygen vacancy concentration variation between the top and bottom interfaces of the BST during the reduction and oxidation reactions. For the Pt/BST/Pt capacitor fabricated on the Si wafer, the reduction or oxidation can occur only from the top surface because the movement of oxygen through the bottom interface is blocked by the bulk Si wafer. Therefore, the local oxygen vacancy concentration and the local conducting electron density should be higher and lower at the top electrode interface than those of the bottom electrode interface during the annealing under N_2 atmosphere and maintaining in air, respectively. When the capacitor is annealed again under N_2 atmosphere, the Φ_B of the top electrode interface increases more than that of the bottom electrode interface which also supports the above model.

The Φ_B is not only dependent on the postannealing atmosphere and time after the annealing but also on the deposition temperature. When the BST film is deposited at 490° the Φ_B is only about 1.45 eV even only half day after the same postannealing under N_2 atmosphere as shown in figure 4. The crystalline quality, amount of non-crystalline phase, if any, and grain size etc. are strongly dependent on the deposition temperature and all of these factors can affect the interface state density and the Φ_B.

V. Summary

The interfacial potential barrier height Φ_B at the interface between the BST and Pt critically depends on the BST film deposition temperature, postannealing atmosphere and time after the annealing. The postannealing of a 40 nm thick BST film under N_2 at-

mosphere results in a high interface potential barrier height and low leakage current due to the increased carrier concentration. Maintaining the BST capacitor in air for a long time reduces the Φ_B from about 2.4 eV to 1.6 eV due to the oxidation. Φ_B is not so dependent on the film thicknesses ranging from 20 nm to 150 nm

The 20 nm thick BST film shows the tunneling conduction behavior whereas the Schottky emission at the interface between BST and Pt controls the leakage conduction of the thicker films.

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