Pseudomorphic AlGaAs/InGaAs /GaAs High Electron Mobility Transistors with Super Low Noise Performances of 0.41 dB at 18 GHz

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ABSTRACT

Fully passivated low noise AlGaAs/InGaAs/GaAs pseudomorphic (PM) HEMT with wide head T-shaped gates were fabricated by dose split electron beam lithography (DSL). The dimensions of gate head and footprint were optimized by controlling the splitted pattern size, dose, and spaces of each pattern. We obtained stable T-shaped gate of 0.15 μm gate length with 1.35 μm-wide head. The maximum extrinsic transconductance was 560 mS/mm. The minimum noise figure measured at 18 GHz at $V_{ds} = 2$ V and $I_{ds} = 17$ mA was 0.41 dB with associated gain of 8.19 dB. At 12 GHz, the minimum noise figure and an associated gain were 0.26 and 10.25 dB, respectively. These noise figures are the lowest values ever reported for GaAs-based HEMTs. These results are attributed to the extremely low gate resistance of wide head T-shaped gate having a ratio of the head to footprint dimensions larger than 9.

I. INTRODUCTION

Low noise HEMTs are promising devices for millimeter-wave and optical communications systems due to their excellent high frequency and low-noise performance [1]. At present, low noise HEMTs are widely used in the front end of satellite communications, radio astronomy, and satellite direct broadcasting receiver systems. As this applications progress, extremely low noise devices will be required in the microwave and millimeter wave ranges. Until now, the best noise performance has been reported for InAlAs/InGaAs/InP HEMTs [2]. The problems with InP-based HEMTs, such as their lack of reliability, and difficulties in controlling the defects and fabrication processes, encourage the development of low noise GaAs-based HEMTs [3].

In improving the minimum noise figures, the most important parameters are the gate and source resistances. In this study, we present the lowest noise characteristics of GaAs based HEMT comparable to InP based HEMT obtained by optimization of the fabrication technologies such as wide head T-shaped gate and selective recess etching as well as the design of epitaxial layer structure. In order to reduce the gate resistance, the cross sectional area of T-shaped gate must be increased while keeping the gate footprint constant. To increase the area of a T-shaped gate, several technologies such as multilayer resists and multiple electron beam lithography have been developed to delineate T-shaped gates reducing both the gate length and parasitic resistances simultaneously [4], [5]. However, these fabrication techniques have employed trilayer resists which require delicate control of resist sensitivity and development to form T-shaped gates. Also, there still exist difficulties in fabricating T-shaped gates with a wide gate head.

We developed the dose split electron beam lithography (DSL) for wide head T-shaped gates, and employed it for the fabrication of AlGaAs/InGaAs PM HEMTs with 0.15 μm gate length. The HEMT device exhibited extremely low noise figures of 0.26 dB and 0.41 dB at 12 GHz and 18 GHz, respectively. These results were attributed to the extremely low gate resistance, R_g, obtained from the high ratio of gate head length to gate footprint.

II. DOSE SPLIT ELECTRON BEAM LITHOGRAPHY (DSL)

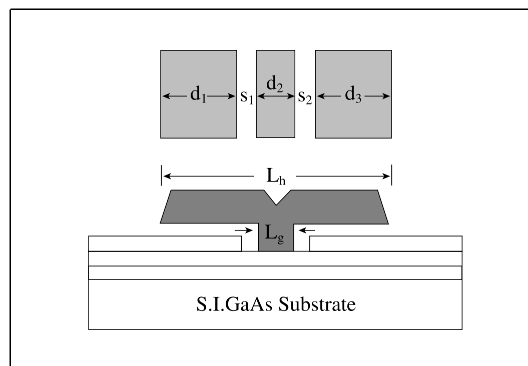

Fig. 1. The schematic drawing of T-shaped gate formed by DSL.

To form the T-shaped gate electrode with

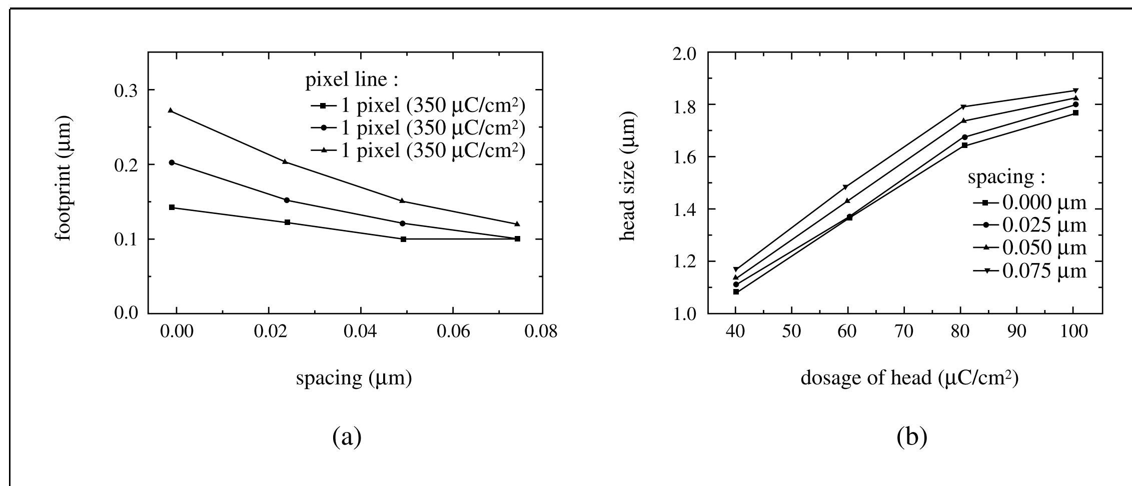

Fig. 2. (a) The variation of gate footprint with the change of spacing and pixel lines, (b) the head size variation with the change of head dosage and spacing.

a wide head on a small footprint, a DSL with electron beam system and two-layer resist systems have been developed. Fig. 1 shows the schematic drawing of T-shaped gate formed by DSL. As shown in the Fig. 1, the head length L_h is defined by the dimension composed of the patterns, d_1, d_2, and d_3, and the intervening spaces, s_1 and s_2. The size of the central pattern d_2 and the intervening spaces and the doses for each pattern determine the gate footprint, L_g. The designed head and central pattern dimensions were 1.15 μm and 0.1 μm, respectively. In this process, attention has been paid to the combination of the top and bottom resists: an overhanging profile for the top-layer resist and high resolution for the bottom-layer resist. A polymethyl metacrylate-methacrylic acid (P(MMA-MAA)) was used for the top layer and a polymethyl metacrylate (PMMA) for the bottom layer. After coating 0.3 μm thick PMMA and prebaking, 0.6 μm thick P(MMA-MAA) was coated and prebaked. To form the gate footprint with reproducibility, the spacing between central and side patterns, exposure doses, and resist development conditions were optimized. Fig. 2 shows the variation of the gate footprint with the change of spacing, pixel line, and dosage. As shown in Fig 2(a), the optimized spacing was 0.025 μm in case of 2 pixel line for 0.15 μm gate footprint. To obtain a T-shaped gate with footprint of 0.15 μm, we find that optimum dosage for the footprint of 2 pixel (0.050 μm) line is 440 μC/cm^2. The doses of the d_1 and d_3, and the central pattern d_2 were determined to 60 μC/cm^2 and 460 μC/cm^2, respectively. Fig. 2(b) shows the variation of head size with the change of dosage and spacing. As shown in Fig. 2(b), it is convenient to control the head

size by changing the dosage. Those patterns were exposed by Leica EBML300 system with 30 kV acceleration voltage. The top and bottom resists were developed using a mixed solution of MIBK and IPA. The overhang of the top resist was suitable for the following lift-off process.

III. HEMT STRUCTURE AND FABRICATION

The AlGaAs/InGaAs/GaAs pseudomorphic HEMT structures have been grown by using molecular beam epitaxy (MBE). The cross-section of the PM InGaAs channel HEMT is shown in Fig. 3. An 80 nm thick undoped GaAs buffer layer and ten AlAs-GaAs superlattices are grown on 3-inch diameter semi-insulating GaAs substrates, followed by a 600 nm thick undoped GaAs layer. The thickness of the $In_{0.15}Ga_{0.85}As$ channel layer is 12 nm. The planar doping layer with Si of a 5×10^{12} cm^{-2} density is separated from the active layer by a thin undoped $Al_{0.24}Ga_{0.76}As$ spacer, and a 30 nm thick undoped $Al_{0.24}Ga_{0.76}As$ Schottky layer is grown. To reduce parasitic resistance, the 50 nm thick GaAs cap layer is highly doped with Si of 5×10^{18} cm^{-3}. The carrier concentration in the two-dimensional electron gas (2DEG) has been determined from Hall measurements. The sheet carrier density of 2DEG and the electron mobility measured at room temperature are 2.1×10^{12} cm^{-2} and 6,100 $cm^2/V \cdot s$, respectively.

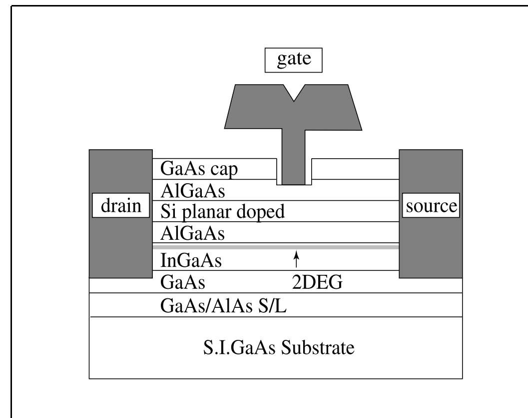

Fig. 3. The epitaxial layer structure of pseudomorphic InGaAs channel HEMT.

In the device fabrication, a mesa isolation was performed by wet chemical etching, ohmic contacts were formed by Ni/Ge/Au/Ti/Au evaporation, and then alloyed by rapid thermal annealing. To get low source resistance, the n^+ GaAs cap layer was selectively etched using a mixture of citric acid and hydrogen peroxide with a ratio of 3.5 : 1. The etch selectivity of GaAs to AlGaAs was higher than 40. After gate recess etching, Ti/Pt/Au (0.6 μm thick) layers were deposited and lifted-off. Finally, the device was passivated with Si_xN_y. Fig. 4(a) shows the cross sectional SEM photograph of an AlGaAs/InGaAs pseudomorphic HEMT fabricated by optimization of dose split E-beam lithography. As shown in Fig. 4(a), the T-shaped gate formed by dose split E-beam lithography has the ratio of gate head length (1.35 μm) to gate footprint (0.15 μm) larger than 9, which is more than twice that of the conventional T-shaped gate [5]. The planar

view of the AlGaAs/InGaAs/GaAs PHEMT device with Si_xN_y passivation layer is shown in Fig. 4(b).

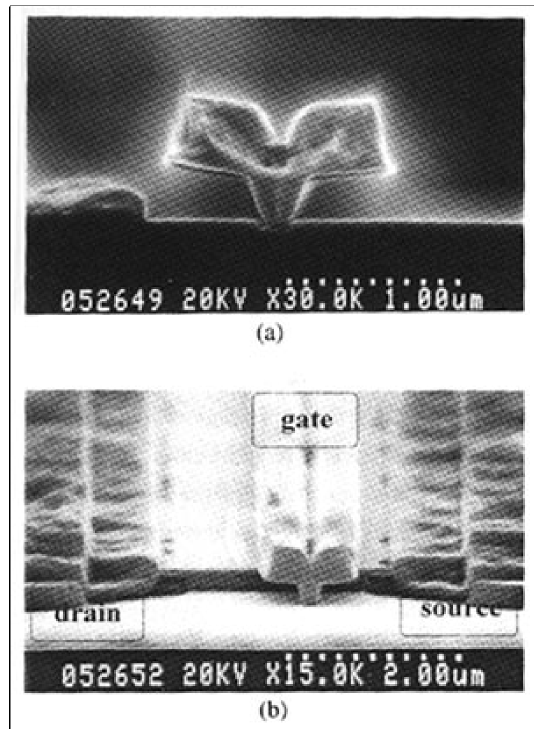

Fig. 4. (a) The cross-sectional SEM photographs of T-shaped gate formed by dose split lithography, and (b) planar view of passivated pseudomorphic InGaAs channel HEMT.

IV. DEVICE PERFORMANCE

The device performance was measured for a fully passivated HEMT with 0.15 μm gate length and a total gate width of 140 μm. As shown in Fig. 5, the drain saturation current I_{dss} measured at $V_g = 0$ V is 33 mA. As shown in Fig. 6, the maximum extrinsic transconductance measured at $V_g = 0$ V, $V_{ds} = 2.0$ V and the threshold voltage V_{th} were 560 mS/mm and -0.81 V, respectively.

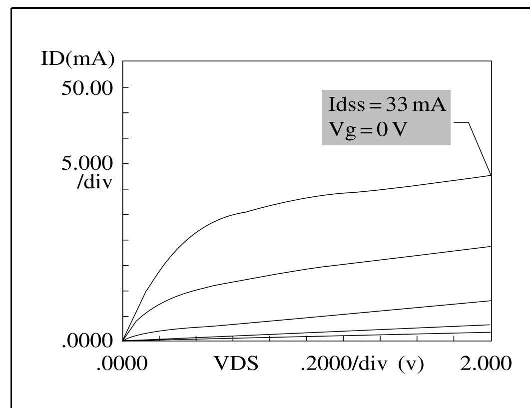

Fig. 5. The current voltage characteristics of 0.15×140 μm^2 HEMT device.

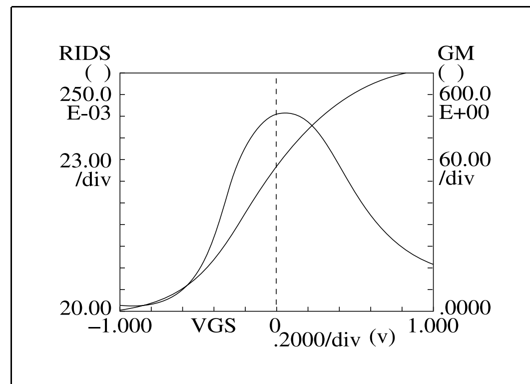

Fig. 6. The transconductance and drain current as a function of gate bias at $V_{ds} = 2$ V. The maximum transconductance and threshold voltage are 560 mS/mm and -0.8 V, respectively.

The cut-off frequency f_T was obtained from the extrapolation of the current gain, $|h_{21}|$, to unity using a -6 dB/octave slope, and the maximum frequency of oscillation $f_{\max}$

was extracted from small signal parameters. The cut-off frequency measured at $V_{ds} = 2$ V of a 0.15 μm gate device is 89 GHz. The extracted maximum frequency of oscillation is 197 GHz.

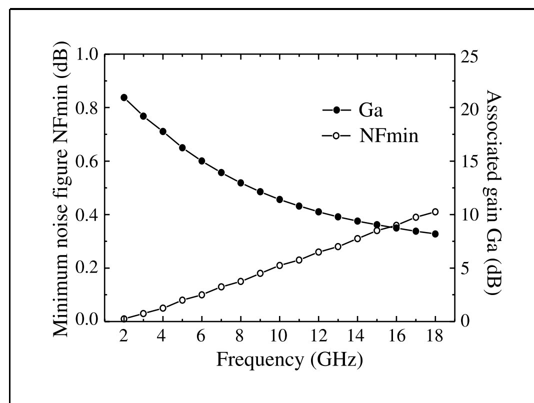

Fig. 7. Minimum noise figure, $NF_{\min}$, and associated gain, G_a, versus frequency at I_{ds} = 50 % I_{dss} (V_{ds} = 2 V, I_{dss} = 33 mA).

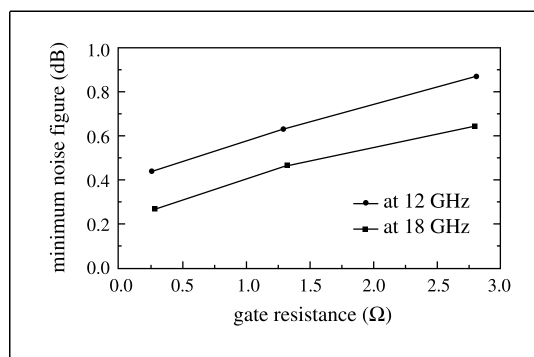

Fig. 8. The relationship between gate resistance and minimum noise figure.

Noise figure measurements have been carried out in the frequency range from 2 GHz to 18 GHz by using an HP 8510B network analyzer and an ATN NP5 noise parameter test set. After each calibration routine (LRM ISS and SOLT) the same low-noise HEMT device has been tested at a fixed biasing condition (V_{ds} = 2.0 V, I_{ds} = 17 (± 0.2) mA). The repeatability of the smoothed minimum noise figure, $NF_{\min}$, curves was within ± 0.035 dB up to 18 GHz. The difference between the smoothed and measured data was less than ± 0.04 dB. The associated gain values showed a maximum deviation of ± 0.50 dB from the mean value. We measured the dependence of $NF_{\min}$ on the drain-source current I_{ds}, which is controlled by the applied gate voltage. At a fixed drain-source voltage of 2.0 V, $NF_{\min}$ can be observed around 50% of the I_{ds}/I_{dss} ratio. Fig. 7 shows the $NF_{\min}$ and associated gain, G_a, versus frequency at 50% I_{dss} ($V_{ds} = 2$ V, $I_{ds} = 17$ mA). The $NF_{\min}$ measured at 12 GHz, including passivation loss is 0.26 dB with G_a of 10.25 dB. At 18 GHz, the $NF_{\min}$ is 0.41 dB with G_a of 8.19 dB. These noise figures are the lowest values ever reported for the passivated GaAs-based HEMTs, and are comparable to those for InP based HEMT [2]. Fig. 8 shows the relationship between gate resistances and minimum noise figures. As shown in Fig. 8, the R_g of the conventional and our T-shaped gate were 1.33 Ω and 0.25 Ω, respectively. For our device, the improvements of $NF_{\min}$ due to the reduction of R_g were 0.19 dB and 0.24 dB at 12 GHz and 18 GHz, respectively. We believe that the excellent noise characteristics can be attributed not only to the low source resistance, but also to the extremely low gate resistance owing to the large cross-sectional area

Table 1. Extracted parameters. The minimum noise figure, $NF_{\min}$, was measured and calculated for 0.15×140 μm^2 HEMT at $V_{ds} = 2$ V and $I_{ds} = 17$ mA.

g_m (mS)	C_{gs} (pF)	τ (psec)	C_{dg} (fF)	C_{ds} (fF)	L_g (pH)	L_d (pH)	L_s (pH)
76	0.12	0.5	40	30	0.10	11.65	0.1
R_i (Ω)	R_g (Ω)	R_d (Ω)	R_s (Ω)	NF_{m12} (dB)	NF_{c12} (dB)	NF_{m18} (dB)	NF_{c18} (dB)
17.35	0.25	3.59	0.30	0.26	0.25	0.41	0.40

NF_{m12}: measured at 12 GHz, NF_{c12}: calculated at 12 GHz,
NF_{m18}: measured at 18 GHz, NF_{c18}: calculated at 18 GHz,

of T-gate. This is one of the most promising devices for millimeter-wave and optical communications systems with excellent low noise performance.

The equivalent circuit model was used to extract the small signal parameters for calculation of the $NF_{\min}$ using the following:

$$NF_{\min} = 10 \cdot \log[1 + K_f \cdot f_M / f_T \cdot \{g_m \cdot (R_g + R_s) + K_i\}^{1/2}], \quad (1)$$

where f_M is the operational frequency, f_T is the cut-off frequency, K_f and K_i are Fukui constant, g_m is the transconductance, and R_s is source resistance, respectively [6]. We used values for K_f and K_i of 0.95 and 0.42 as estimated by Cappy [7]. The extracted parameters and calculated $NF_{\min}$ are listed in Table 1. The minimum noise figure was measured for a 0.15×140 μm^2 pseudomorphic HEMT at $V_{ds} = 2$ V and $I_{ds} = 17$ mA. As shown in Table 1, the measured minimum noise figures are well consistent with the calculated data.

V. CONCLUSION

We developed a dose split electron beam lithography for wide head T-shaped gates, and applied this technology for fabricating AlGaAs/InGaAs/GaAs PM HEMTs with 0.15 μm gate length. This device exhibited very low noise figures of 0.26 dB and 0.41 dB at 12 GHz and 18 GHz, respectively. These data were attributed to the extremely low R_g due to the high ratio of gate head length to gate footprint. The proposed technology is adequate for fabricating low noise and millimeter wave devices.

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