A Novel Body-tied Silicon-On-Insulator(SOI) n-channel Metal-Oxide-Semiconductor Field-Effect Transistor with Grounded Body Electrode

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ABSTRACT

A novel body-tied silicon-on-insulator(SOI) n-channel metal-oxide-semiconductor field-effect transistor with grounded body electrode named GBSOI nMOSFET has been developed by wafer bonding and etch-back technology. It has no floating body effect such as kink phenomena on the drain current curves, single-transistor latch and drain current overshoot inherent in a normal SOI device with floating body. We have characterized the interface trap density, kink phenomena on the drain current (I_{DS}-V_{DS}) curves, substrate resistance effect on the I_{DS}-V_{DS} curves, subthreshold current characteristics and single transistor latch of these transistors. We have confirmed that the GBSOI structure is suitable for high-speed and low-voltage VLSI circuits.

I. INTRODUCTION

Silicon-on-insulator(SOI) metal-oxide-semiconductor field-effect transistors(MOSFETs) are well known for several advantages such as simple process, perfect dielectric isolation, removal of parasitic latch-up phenomena, enhancement of operating speed, suppression of interference effect between devices and enhancement of radiation hardness [1]-[3]. Furthermore, turn-on characteristics and current drivability of fully-depleted SOI MOSFETs are enhanced [4], [5]. Especially, as the device made on thin film SOI substrate becomes smaller, short-channel and narrow-width effects are reduced and immunity for the punchthrough are enhanced compared to the bulk-Si counterpart [6]. However, various anomalous phenomena such as kink effect, drain current overshoot, single transistor latch and reduced drain breakdown voltage make it difficult to apply SOI MOSFET to VLSI circuits [7]. These problems are originated basically from the floating body in SOI MOSFET and can be eliminated with stabilized body potential. In general, two methods to stabilize the body potential are considered as the followings: biasing the substrate below the buried oxide to decrease the variation of the body potential and biasing the body directly. The former method has a drawback in optimizing both n-channel and p-channel MOSFETs, so that the latter case has become the technique for stabilizing the body potential. Therefore, novel structures for SOI MOSFET are required to bias the body directly.

In this paper, we propose a novel body-tied SOI MOSFET named GBSOI MOSFET structure to bias the SOI body directly. The GBSOI structure can sustain effective device area and large allowance in interconnect process. Therefore, the proposed structure is suitable for future very large scale integrated(VLSI) MOS circuits. This structure is accomplished by using wafer bonding and etch-back technology, including conventional MOS fabrication technology. The fabricated structures were electrically characterized to verify the device performance and reliability.

II. DEVICE STRUCTURE

Various structures have been proposed to directly bias the SOI body at a certain potential. For example, modification of the planar gate to H- or T-type structure [8], implantation of oxygen ions into the silicon substrate using a patterned photoresist as implanting mask [9], formation of epitaxial layer on the exposed silicon [10], connection between the source diffusion and SOI body diffusion layers through the metal or highly doped diffusion layers [11], [12] have been suggested. Modification of a normal gate layout, such as H- or T-gate structures, has an advantage regarding the compatibility with conventional process. However, it also has a disadvantage for large scale integration due to the extra consumption of lay-

out area. The formation of body-tied structures by selectively implanted oxygen and annealing has an advantage in consideration of the compatibility with the conventional circuit layout. However, it makes hard to apply this technology to VLSI circuits because the selective oxidation induces the surface bending problems due to the volume expansion in the oxygen implanted region. Selective epitaxy on the exposed silicon area results in the easy formation of body-tied structure, however, it also has a disadvantage of higher process complexity than the normal process and generation of crystal defects in the epitaxial layers. Connection between the SOI body and the source diffusion layers needs a double implantation in the source region thus making it difficult to control the diffusion profiles in thin film SOI, so that the device performances may be deteriorated due to a large resistance in the source region.

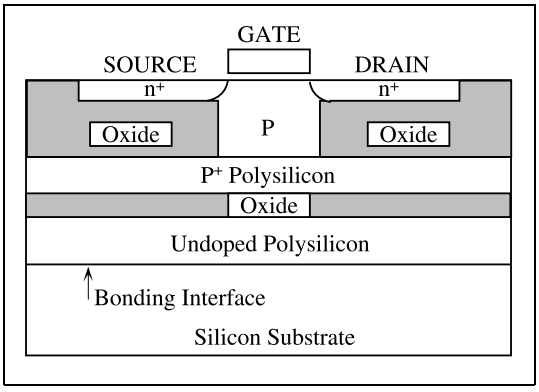

Fig. 1. The proposed Grounded body SOI(GBSOI) nMOSFET structure.

In this paper, we propose a novel SOI device structure named GBSOI MOSFET to bias the SOI body directly. Fig. 1 shows the body electrode under the channel region connected to the highly doped polysilicon of the same dopant type as the SOI body. In nMOSFET of the case, the body electrode of p^+ polysilicon with its periphery surrounded by the oxide is under the exposed active silicon. The oxide layer formed below the p^+ polysilicon acts as a buried oxide of the conventional SOI structure. The undoped polysilicon layer under the oxide layer acts as a normal silicon substrate with the handle wafer. Each device is isolated by the oxide. However, the SOI bodies are connected through the p^+ polysilicon. Therefore, the proposed device has the same steady-state characteristics as those of the bulk silicon counterpart. On the other hand, it has the same transient characteristics as those of the normal SOI device due to the reduced junction capacitance and the parasitic interconnect capacitance. In addition, GBSOI devices were isolated from the backside substrate by the buried oxide so that they have high radiation hardness for SEU. As the proposed device has a buried electrode under the active silicon area, it is very useful in circuit layout due to the freedom of device arrangement.

III. DEVICE FABRICATION

Figure 2 shows the fabrication steps of the GBSOI nMOSFET. Although the fabrication procedure was briefly described in [13], more detailed explanations focused on the wafer

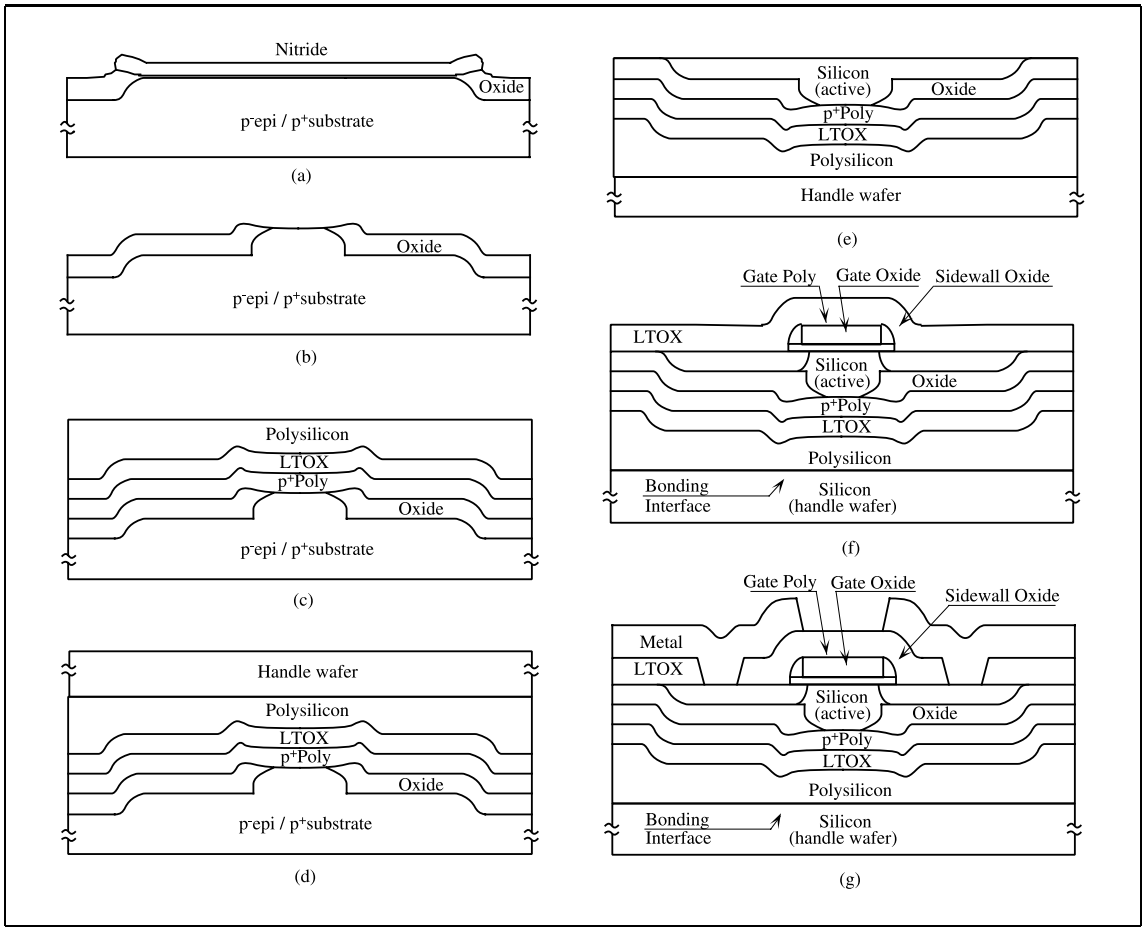

Fig. 2. Fabrication steps of the GBSOI nMOSFET. (a) active formation and mask oxidation for next RIE process, (b) tub formation and field oxidation by LOCOS, (c) buried electrode formation, oxide and thick polysilicon deposition, (d) surface polishing and wafer bonding, (e) lapping, selective etching, and surface polishing of device substrate, (f) gate formation, source/drain implantation, and cover oxide deposition, (g) contact formation and metallization.

bonding and etchback process among the fabrication steps are given in this section.

1. Pre-process on Device Wafer

The starting material for the GBSOI structure is a highly doped p-type silicon substrate of (100) orientation with a p^- epitaxial layer of 3 μm thickness. Dopant concentrations of the silicon substrate and the epitaxial layer are 5×10^{18} cm^{-3} and 3×10^{15} cm^{-3}, respectively. A sacrificial oxide of 25 nm was grown on the p^- epitaxial layer in a furnace and a nitride of 120 nm was formed on the oxide by LPCVD. Active regions were defined photolithographically and the nitride, the sacrificial oxide and

the silicon in the field regions were sequentially dry etched down to the depth of 350 nm from the surface of the p^- epitaxial layer. A thermal oxide of 300 nm was formed on the field regions in a conventional furnace to protect the silicon from any damage during the next dry etch (Fig. 2-(a)). Tub regions were defined photolithographically, the nitride (120 nm) and the sacrificial oxide (25 nm) in the active regions was dry etched. Subsequently, an extra p^- epitaxial silicon of 300 nm thickness were also dry etched. After the removal of the residual oxide on the field regions, a thermal oxide of 650 nm was formed in a conventional furnace to isolate devices. The nitride and the sacrificial oxide remaining in tub regions were removed (Fig. 2-(b)) and a polysilicon layer of 200 nm thickness was formed on the wafer by LPCVD. Boron ions were implanted into the polysilicon layer in a dose of 1×10^{15} cm^{-2} and on energy of 50 keV. A polysilicon layer of 200 nm was deposited on the previous polysilicon layer again.

2. Mirror Polishing

The body electrode was formed on the pre-processed wafer. An oxide layer of 200 nm thickness and an undoped polysilicon layer of 5 μm thickness were sequentially deposited on the wafer by LPCVD. Then the surface of the undoped polysilicon layer was mirror polished. Polishing was carried out by WESTECH 372 polishing machine. On mirror polishing, the initial polishing with a rate of 800-900 nm/min using SJ079 slurry was performed for 2 min and followed by 3 min final polishing with a rate of 20-30 nm/min using SJ068 slurry (Fig. 2-(c)).

3. Wafer Bonding

The bonding process consists of a bonding step in atmospheric ambient and a thermal heating in a conventional furnace. The pre-processed device wafer described previously and the handle wafers for supporting the thinned device substrates were cleaned in chemical solution. They were bonded with mirror-polished surfaces facing each other. Bonding force in atmospheric ambient was generated by OH radicals adsorbed at the native oxide on the polished polysilicon. For stronger adhesion between the two wafers, the bonded wafers were heated in a conventional furnace at 900°C in wet oxidation ambient. The initial bonding by OH radicals is converted into mating by Si-O-Si bonds through the heat treatment at high temperature, thus leading to strong bonding (Fig. 2-(d)).

4. Selective Etch

The highly doped silicon substrate was well etched in dilute solution ($HF : HNO_3 : CH_3COOH = 1; 3 : 8$), having the p^- epitaxial layer hardly etched. Etch selectivity between the p^+ and the p^- silicon is 160-180 : 1 and the critical dopant concentration for selective etching of the p^+ silicon was 2.5×10^{17} cm^{-3}. After the selective etching, the p^- sili-

con epitaxial layer was left over as an SOI film for MOS devices for fabrication.

5. Selective Polishing

The wafer on which the p^- silicon epitaxial layer is left has to be thinned down by selective polishing until the field oxide is reached. To obtain a uniform thickness of the p^- epitaxial layer, we need a high selectivity in polishing between the silicon and the oxide. Equipments and process conditions used for this polishing are the same as the case of the mirror polishing, except that the polishing is done until the field oxide on the device wafer is exposed. After the polishing, a thin oxide was thermally grown and stripped off to remove any possible surface damage due to polishing (Fig. 2-(e)).

6. Post-process on Device Wafer

The remaining process steps are similar to the conventional MOS fabrication process. Boron ions were implanted into the active regions with an energy of 30 keV and a dose of 1.5×10^{12} cm^{-2} to adjust the device threshold voltage. A gate oxide of 23 nm thickness was grown by dry oxidation in 920°C and followed by deposition polysilicon of 400 nm thickness by LPCVD. Source and drain regions were formed by arsenic ion implantation with a dose of 5×10^{15} cm^{-2} and an energy of 100 keV. Implanted dopants were activated and driven-in by thermal annealing at 920°C in N_2 ambient for 30 min in a conventional furnace (Fig. 2-(f)). After the contacts were defined by photolithography and dry etch, an Al-1% Si layer of 1 μm thickness was deposited by sputtering and metal lines were formed by photolithography and dry etch (Fig. 2-(g)). Finally, the wafer was annealed at 450°C for 30 min. in H_2/N_2 ambient in a conventional furnace.

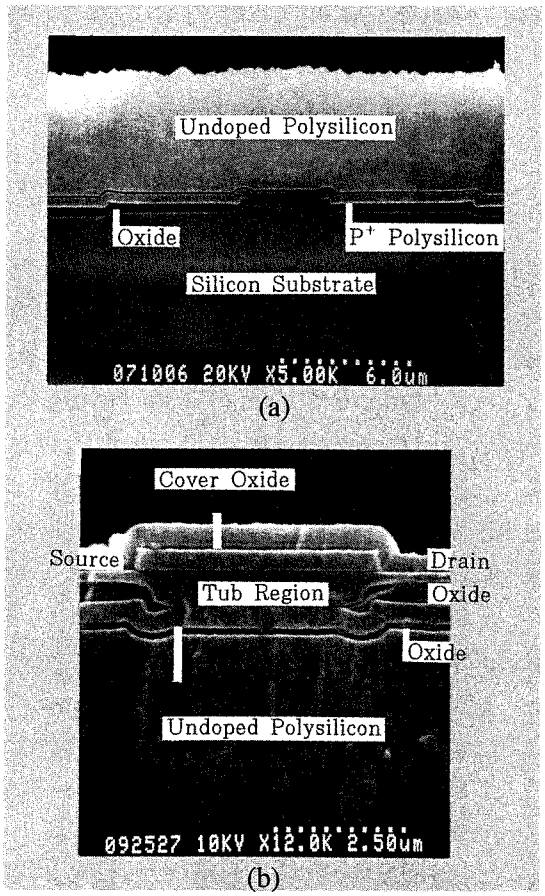

Fig. 3. Cross sectional views of SEM micrograph. (a) after thick polysilicon deposition (Fig. 2-(c)), (b) after cover oxide deposition (Fig. 2-(f)).

Figure 3-(a) and 3-(b) show the cross

sectional view of SEM micrograph after the polysilicon deposition and the cover oxide deposition, respectively. In Fig. 3-(a), the rough surface polysilicon, the buried oxide, the buried polysilicon and the tub region are shown. In Fig. 3-(b), the tub region for body contact, the extended silicon region for the source and drain, the polysilicon for the gate electrode, and the cover oxide are presented.

IV. CHARACTERIZATION OF THE GBSOI nMOSFET

To characterize GBSOI nMOSFETs, conventional SOI and bulk silicon nMOSFETs were also fabricated in the same lot. The interface trap density at the gate oxide/silicon interface was measured using charge pumping method to estimate surface damage due to the polishing. The drain current-drain voltage (I_{DS}-V_{DS}) characteristics, the drain current dependence on the substrate resistance, the subthreshold characteristics, the single transistor latches were also measured and analyzed.

1. Interface Trap Density

The most efficient method to measure interface trap density (D_{it}) of bulk silicon MOSFET is the charge pumping method [14], [15]. As the GBSOI device has a body electrode, the charge pumping method may be used, which is not the case for a normal with floating body SOI device. Interface trap densities can be extracted from measured charge pumping current (I_{CP}) with techniques developed by G. Groeseneken *et al*. [16]. This technique yields a mean interface trap density of representative values between the flatband and threshold according to

$$\overline{D_{it}} = \frac{1}{2qkTA_g} \times \frac{\Delta Q_{it}}{\Delta \ln(f)},$$

where A_g is the gate area and f is the pulse frequency applied to the gate. $Q_{it} = I_{CP}/f$ is defined as the a recombined interface trap charge per cycle.

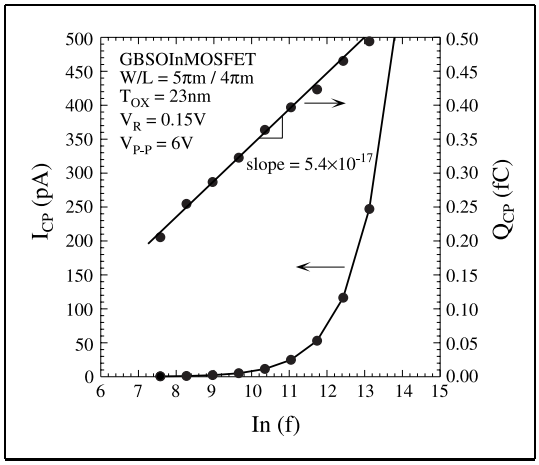

Fig. 4. Plot of measured charge pumping current (Icp) and interface trap charge (Q_{it}) versus nature logarithm of frequency ($\ln(f)$) for the GBSOI nMOSFET.

Figure 4 shows the measured I_{cp} versus $\ln(f)$ and calculated Q_{cp} versus $\ln(f)$. In the measurement, triangular waveform (6 V peak to peak, 50% duty cycle) is applied to the gate sweeps from 1 kHz to 1 MHz. To stimulate charge accumulation at the surface dur-

ing the negative portion of the waveform, a reverse bias of 0.15 V was applied to both source and drain. In figure 4, $\Delta Q_{cp}/\Delta \ln(f)$ is obtained from Q_{cp} versus $\ln(f)$ plot. The values of $\Delta Q_{cp}/\Delta \ln(f)$ for the novel body-tied SOI nMOSFET is 5.4×10^{-17}. Calculated interface trap density at the gate oxide/silicon interface of the novel body-tied SOI nMOSFET was about 3.2×10^{10} $eV^{-1}cm^{-2}$, which was somewhat larger than 1.9×10^{10} $eV^{-1}cm^{-2}$ of the conventional bulk silicon nMOSFET.

2. I_{DS}-V_{DS} Characteristics

The current-voltage (I_{DS}-V_{DS}) curves for a channel width of 5.0 μm and a channel length of 1.6 μm are shown in Fig. 5. The floating body SOI nMOSFET is also shown for comparison with the GBSOI nMOSFET. The threshold voltages of the two devices are both 0.7 V. In this figure, kinks appear on the drain current curves in the saturation region of the floating body SOI nMOSFET, while no kinks can be seen on the curves of the GBSOI nMOSFET. This phenomenon demonstrates that the GBSOI MOSFET structure is very useful not only for high-speed and low-power MOS devices but also for analog devices. For more a detailed check of kink points, conductance, the derivative of the drain current with respect to the drain voltage ($\partial I_{DS}/\partial V_{DS}$, was calculated for the GBSOI and the floating body SOI nMOSFET. In Fig. 6, the peaks appear on the conductance curves of the floating body SOI nMOSFET in the saturation region, while no peaks are seen on the curves of the GBSOI. So we can conclude that kink effect can be completely eliminated in the GBSOI nMOSFET.

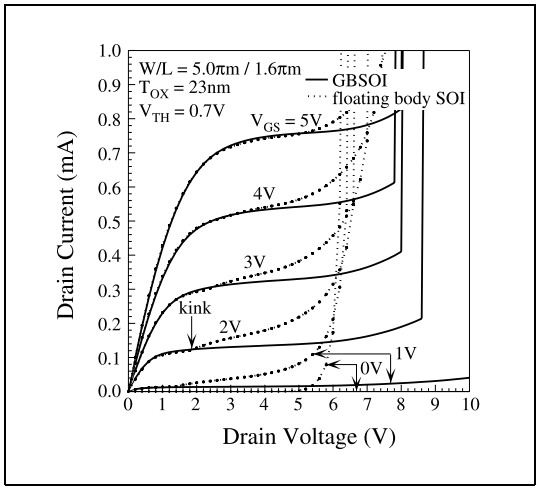

Fig. 5. I_{DS} - V_{DS} curve of the floating body SOI and GBSOI nMOSFET. The kinks appear on the drain current curves in the saturation region of the floating body SOI nMOSFET, while no kinks appear on the curves of the GBSOI nMOSFET.

3. The Effect of the Substrate Resistance

The effect of the substrate resistance on the kink phenomena has been analyzed by simulation [17]. We may expect that, as the substrate resistance of the GBSOI nMOSFET is increased, kink phenonena appear in the drain current curves of the GBSOI nMOSFET. To evaluate the level of the kink appearance, external resistors were connected to the buried electrode of the GBSOI nMOSFET. First, we measured the internal resistance due to the

buried p^+ polysilicon electrode. The measured internal resistance of the diode from current-voltage characteristics was about 2.5 kΩ. Next, the external resistors ranging from 7.5 kΩ to 1 MΩ were connected to the buried electrode or the buried electrode was left floating.

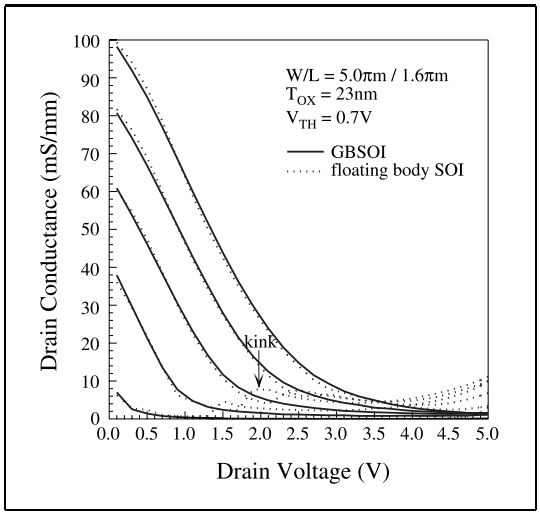

Fig. 6. Conductance characteristics of the floating body SOI and GBSOI nMOSFET. Conductance peaks appear on the curves in the saturation region of the floating body SOI nMOSFET, while no peaks appear on the curves of the GBSOI nMOSFET.

Figure 7 shows the variation of the I_{DS}-V_{DS} characteristics of the GBSOI nMOSFET with the external resistance. There are no kinks on the drain curves even for the external resistance of 100 kΩ, while weak kinks appear for 1 MΩ. From these results, kink effect needs not to be considered for a buried electrode resistance up to about 100 kΩ.

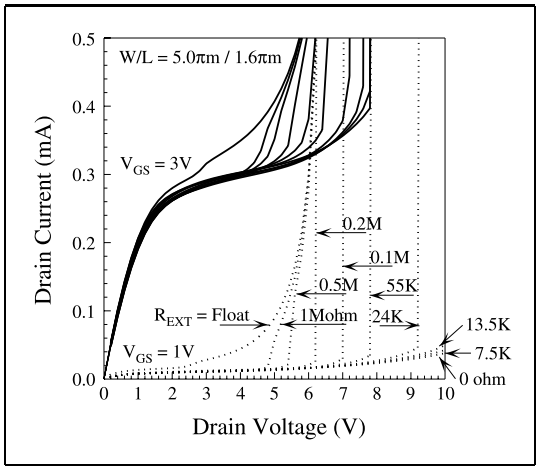

Fig. 7. The effects of substrate resistance on I_{DS} - V_{DS} curves of the GBSOI nMOSFET. No kinks occur on the I_{DS} - V_{DS} curves up to about 100kΩ of external resistance.

4. Subthreshold Characteristics

Figure 8 shows the subthreshold current (I_{DS}-V_{DS}) curves of the two nMOSFET mentioned above. The subthreshold swings of the two nMOSFET have nearly the same value of 90 mV/dec at a drain bias of 0.05 V. However, those of the GBSOI and the floating body SOI nMOSFET are 82 mV/dec and 47 mV/dec, respectively, at the drain bias of 5.05 V. The subthreshold swing for the GBSOI nMOSFET is nearly independent of the drain bias. On the other hand, subthreshold swing is strongly dependent on the drain bias for the floating body SOI nMOSFET, which is the other manifestation of the kink effect. At a certain high drain voltage, subthreshold swing of the floating body SOI nMOSFET nearly reaches a zero value, which is due to the parasitic lateral bipo-

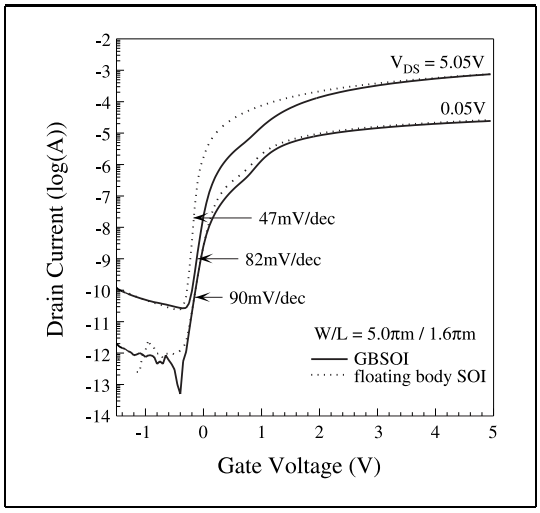

Fig. 8. I_{DS} - V_{DS} curves of the floating body SOI and GBSOI nMOSFET. Subthreshold swing is nearly independent of the drain bias for the GBSOI nMOSFET. However, that of the floating body SOI nMOSFET is strongly dependent of the drain bias.

lar turn-on called single-transistor latch [18]. In this figure, humps are seen in the linear regions of the curves of the two nMOSFET. It is known to be due to the parasitic channel at the edge of the field oxide in the channel width direction [19]. Figure 9 shows the I_{DS}-V_{DS} curves of the two nMOSFET at V_{DS} of 6.0 and 6.5 V. The floating body SOI nMOSFET shows the nearly identical curves in the forward V_{GS} scan from -1 V to 5 V and the reverse VGS scan from 5 V to -1 V for V_{DS} of 6.0 V. However, I_{DS} remains high even though the gate voltage is lowered below the threshold voltage in the reverse V_{GS} scan for V_{DS} of 6.5 V, due to the single transistor latch. On the other hand, this hysteretic phenomenon does not appear for the GBSOI nMOSFET.

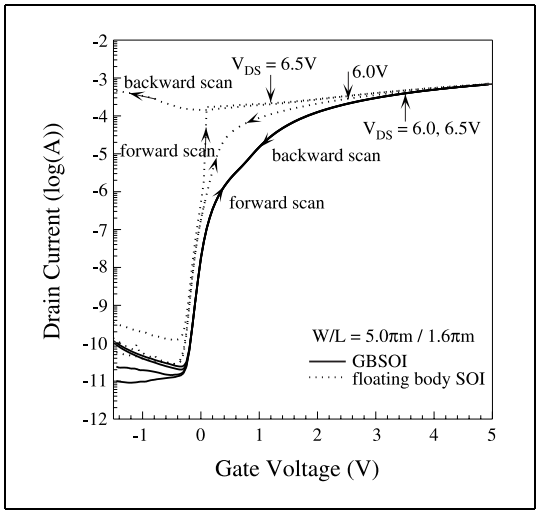

Fig. 9. I_{DS} - V_{DS} curves of the floating body SOI and GBSOI nMOSFET at high drain bias. Hysteresis phenomena appear on the curves for the floating body SOI nMOSFET, while these phenomena do not appear for the GBSOI nMOSFET.

V. CONCLUSIONS

The GBSOI MOSFET has been proposed, fabricated and characterized to verify the applicability for high speed and low power VLSI circuits including digital and analog circuits. This structure, with its body tied to a grounded p^+ polysilicon layer buried under the channel region, was realized by wafer bonding and polishing technology. There was no significant damage at the gate oxide/silicon interface, as was confirmed by the measurement of interface trap density by the charge pumping method. The GBSOI device with a buried elec-

trode eliminated body floating effects such as drain current kink, single transistor latch and it increased drain breakdown voltage. An occurrence of drain current kink depending on the resistance was monitored by connecting various external resistors to the p^+ polysilicon of the buried electrode. As a result, kink effect was not observed for the buried electrode resistance under 100 kΩ. Interconnection was done under the channel of the GBSOI device so that there was no consumption of layout area. This technique can also be applied to pMOSFET by exchanging the dopant type of the nMOSFET and extended to CMOS device by adding extra two masks for the buried electrode to GBSOI nMOSFET process. Therefore, the GBSOI device is suitable for future high-speed and low-power VLSI circuits.

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