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DESIGN CONCEPT FOR SINGLE CHIP MOSAIC CCD CONTROLLER

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ABSTRACT

The CCDs are widely used in astronomical observations either in direct imaging use or spectroscopic mode. However, the areas of available sensors are too small for large imaging format. One possibility to obtain large detection area is to assemble mosaics of CCD, and drive them simultaneously. Parallel driving of many CCDs together rules out the possibility of individual tuning; however, such optimisation is very important, when the ultimate low light level performance is required, particularly for new, or mixed devices. In this work, a new concept is explored for an entirely novel approach, where the drive waveforms are multiplexed and interleaved. This simultaneously reduces the number of leadout connections and permits individual optimisation efficiently. The digital controller can be designed within a single EPLD (Erasable Programmable Logic Device) chip produced by a CAD software package, where most of the digital controller circuits are integrated. This method can minimise the component count, and improve the system efficiency greatly, based on earlier works by Han et al. (1996, 1994). The system software has an open architecture to permit convenient modification by the user, to fit their specific purposes. Some variable system control parameters can be selected by a user with a wider range of choice. The digital controller design concept allows great flexibility of system parameters by the software, specifically for the compatibility to deal with any number of mixed CCDs, and in any format, within the practical limit.

Key Words : Instrumentation, Mosaic CCDs - controller design

I. INTRODUCTION

CCDs have a fundamental restriction of small sensing areas compared to photography. In practice, a CCD covers at best only a few percent of the focal plane of the largest telescopes. The concept of the mosaic focal plane with multiple CCDs and the required drive techniques have been discussed elsewhere (Reiss 1994, Leach and Denune 1994). Recently some good examples for wide field focal plane coverage with such multiple CCDs have been reviewed by Kron (1995).

An efficient and compact mosaic CCD controller design has been developed by Han et al. (1994, 1996) designed with a EPLD CAD software system, without using any microprocessors. This method realises the possibility of controlling multiple CCDs simultaneously in terms of *indefinite expandability* of sensing area with mixed devices and in any format. This is realized by specifying the multiplexed drive waveforms as a digital bit pattern. An ungraded design concept is proposed here using only a single EPLD chip, based on the earlier works by Han et al., aiming at versatile flexibility of the system design.

II. SYSTEM DESIGN APPROACHES

The single chip mosaic controller design approach is based on programable designs such that electronic funtions can be controlled by computer command. The design concept is concentrated mainly on the simplicity, compactness and flexibility using only a single EPLD chip. Most CCD systems employ microprocessors to generate the logic drive waveforms (Leach and Denune, 1994; Reiss 1994). In contrast, the heart of our mosaic CCD hardware is the digital controller logic that is contained in a single PLD chip. The PLDs are based on CMOS EPROM (Erasable Programmable Read Only Memory) technology. A CAD development system (MAXPLUS II) for these PLDs was purchased from the Altera company. Recent advances of CMOS EPROM technology make it possible to integrate a complicated digital circuit that consists of up to 100,000 logic gates into one device. This means that it is possible to concentrate the logic for a mosaic CCD controller into a single PLD chip. The system approach are explained in detail by Han et al. (1996)

III. HARDWARE DESIGN CONCEPT

In most cases, digital controller is the heart of the whole system that provides digital waveforms, all necessary system control logic includig interfacing between the system and computer. Most of other mosaic CCD works employed microprocessors in dealing with digital logic for required waveforms and other control signals.

The PLD designed by Han et al. (1996) sequences the specific digital signals required for driving CCDs using some external memory devices. There is no functional difference with a microprocessor based design. The PLD design approach retains the flexibility of microprocessor based controllers. The controller of Han et al. was basically a memory device control circuit. The information stored in the memory device is downloaded from a host computer in the form of a digital bit pattern (a *bitmap*), which represents the specific timing

waveforms for multiple CCDs. A bitmap is defined as a series of logical 0's and 1's in controller memory that specifies the low or high of CCD waveforms. After writing the bitmap into the memory devices, cycling round the memory generates the digital waveforms directly. This approach allows great flexibility for implementation of various CCD drive waveforms by modifying the *bitmap* off-line, because it directly reflects the required analog waveforms.

Very recently, due to the advances of EPROM technology, it is possible to integrate a complicated digital circuit that consists of up to 100,000 logic gates and 24,576 RAM bit by the EPLD CAD system. This means that it is possible to concentrate a whole digital controller circuit into a single EPLD chip, even *without* using external memory devices. The internal EPLD memory can be organised by any format according to user's specific purpose. All *bitmap* information to drive multiple CCDs can be stored into the internal memory within a PLD chip. Except this, the system design concept is basically the same to that of our earlier work (Han et al. 1996). This approach can reduce the chip count and system design becomes much simpler, because it does not require any external device such as digital buffer to control data or address bus.

The bitmap can be coded by software so that multiple CCDs of different kinds and various operational modes can be implemented. The most important part of the design is the logic circuit which controls memory addresses when (i) downloading a bitmap, and (ii) reading out from memory. Many system parameters like pixel and line counts can also be given as input data.

IV. SOFTWARE DEVELOPMENT

It is very important to organise such *bitmap* efficiently by the software to deal with any waveforms. The whole procedure to generate proper waveforms is entirely dependent on the software. The EPLD also includes some other control signals and buffer control signals. The whole design can be organised into several subdesigns as lower hierachy level of the top-level design according to their functions. In this design, the system control parameters are supplied from the software. It includes a unit of repeat pattern for waveforms as a form of the *bitmap*, DAC (Digital to Analog Converter) control information and controller initialise parameters.

Such digital information is given as variable inputs from the keyboard or initial file, together with some control commands that supply trigger signals for any operation mode. The hardware design of the controller requires its initial conditions to be set before any operations. Here the term 'initial conditions' directly refers to the system parameters of one pixel readout time for both horizontal and vertical, and number of pixels and lines of CCD. Internal latches of a EPLD can store this information digitally, down-loaded from the software. Some other commands are prepared to operation shutter, temperature control.

A balanced combination of each unit in the whole system with associated software is the critical factor for reliable performance. Based on the design concept of this approach, all controller digital logic can be accommodated into a single chip with a great flexibility. The system design approach of this concept allows the opportunity of such optimisation process conveniently even to the novice users without having background experience in system design. It is with these two term goals - flexibility and compactness - in a view that we consider the prospect for a versatile mosaic CCD controller.

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