

## CCD CONTROLLERS FOR THE 6-M TELESCOPE OF RAS WITH IMPROVED ACCURACY OF SIGNAL PROCESSING

S. V. MARKELOV, V. A. MURZIN, N. G. IVASHCHENKO, I. V. AFANASIEVA, AND A. N. BORISENKO  
Special Astrophysical Observatory, Nizhniy Arkhyz, Karachai-Circassian Republic, Russia, 357147

### ABSTRACT

The principles to attain improved accuracy in a new controller for large CCD and mosaics detectors with the application of 16- and 32-bit DSP are presented.

*Key Words* : CCD controller, MOSFET, sensitivity, amplitude distortions

Within the frame of the project of creation of a new CCD controller, we have investigated amplitude signal distortions, introduced by the on-chip MOSFET, which is the main source of distortions in the signal processing channel. For measurements we selected the CCD's with transistors having the width-to-length ratio  $W/L=75/4$  and  $W/L=15/6$ . The objective of the investigation was to estimate the effect the transistor electrical condition has on the value of the charge-to-voltage conversion factor  $K_q$  (sensitivity) and conversion nonlinearity.

The sensitivity  $K_q$  of the source follower is defined by both the differential transistor parameters (gate-to-source transconductance  $S_g$ , substrate-to-source transconductance  $S_b$  and channel conductance  $G_{ds}$ ) and the variant of applied external circuit. The measurements have shown the differential parameters to be related with the drain bias current  $I_d$ , drain-to-source  $U_{ds}$  and gate-to-source  $U_{gs}$  voltages:

$$S_g = f_1(I_d, U_{ds}), S_b = f_2(I_d, U_{ds}, U_{gs}), \\ G_{ds} = f_3(I_d, U_{ds}).$$

The transconductances are dependent on the drain current as  $S_g \sim I_d^{1/2}$  and  $S_b \sim I_d^{1/2}$ , which is consistent with the known static MOSFET models [Cobbold70].

At the same time  $S_g$  and  $S_b$  are seen to depend strongly on the drain-to-source voltage because of high channel conductance which is typical of short-channel transistors. The conductance causes the sensitivity to decrease and is an extra source of instability.

To increase  $K_q$  and ensure its maximum stability, one has to stabilize  $I_d$  and  $U_{ds}$ . To stabilize  $U_{ds}$  it is necessary to apply ac signal from the MOSFET source to the drain with a special circuit. The expression for the charge conversion factor is determined in this case as

$$K_q(\omega) = \frac{S_g + j\omega C_{gs}}{(S_g + j\omega C_{gs})C_{gb} + (S_b + j\omega C_{bs})(C_{gb} + C_{gd} + C_{gs})},$$

where  $C_{gs}$ ,  $C_{gb}$ ,  $C_{gd}$  and  $C_{bs}$  are the gate-to-source, gate-to-substrate, gate-to-drain and substrate-to-source capacitances respectively.

Stepping up of the source-to-substrate voltage decreases the substrate-to-source transconductance, raises

sensitivity and lowers the degree of its dependence on  $U_{gs}$ .

The instability of bias current and voltages strongly affects the charge conversion factor and hence the photometric accuracy of the CCD system. We have compared the instabilities in three circuits of the source follower: with a load resistor, a load current sink and the one with current sink and drain-to-source voltage stabilization.

In the circuit with a load resistor the variation of  $K_q$  with varying drain voltage was measured to be 12.5 %/V, while it was 5.5 %/V when the voltage was varied at the gate.

In the circuit with current sink the effect of the drain current and gate and drain voltage instabilities on  $K_q$  is 10.0 %/mA, 2.2 %/V and 2.5 %/V, respectively.

In the circuit with current and drain-to-source voltage stabilization the influence of instabilities is considerably less. With variation of the drain current, voltages at the gate and drain-source the variation of  $K_q$  is 2.5 %/mA, 0.85 %/V and 0.6 %/V, respectively.

The above mentioned experimental data represent the maximum instability values within the current and voltage operating ranges.

The requirements to the charge conversion factor stability will set limits on the instability of the bias current and voltages.

The nonlinearity of the charge conversion in the follower circuits with a load resistor or current sink may range from -0.3% to +0.1% and from -0.3% to -0.05%, respectively, depending on the chosen conditions.

At the same time the circuit with stabilization of the drain current and drain-to-source voltage ensures the nonlinearity of 0.04-0.055% with an essentially weaker dependence on bias current and voltages, which allows it to be taken into account with the higher accuracy through calibration.

Due to compensation of the gate-to-drain capacity the detector node effective capacity has been reduced to 33 fF as compared to 43 fF in the circuit with a current sink. Moreover due to high voltage gain in this circuit, which may amount to 0.9 and somewhat more, we have increased  $K_q$  from 3.2 to 4.05  $\mu V/e^-$ .

We have used this circuit in seven CCD systems with VPCCD 1040 x 1160 pixels, which permitted readout channel nonlinearity of 0.05% and charge-digit code conversion instability of 0.05% to be attained. Besides, the use of digital correction of bias level in the CDS-processor ensured the bias instability  $< 0.5$  LSB/hour.

When defining an optimum MOSFET operation condition, one should take into account a set of conflicting requirements:

- to attain maximum sensitivity and minimum effective input capacity and nonlinearity needs the drain current, drain-to-source voltage, and gate voltage to be increased;

- according to the MOSFET noise theory the thermal noise can be reduced when decreasing the drain-to-source voltage and stepping up the gate voltage, while the  $1/f$ -noise can be lowered with decreasing the gate voltage.

Since 1995 the laboratory of advanced design of SAO RAS has been developing a universal CCD controller, taking into account the results of the investigations. The controller has a modular extending architecture (up to 32 readout ports) and includes three basic modules based on the ADSP-21060 and ADSP-2181: system controller, CDS-processor and clock generator/driver.

The CCD controller has the following functional characteristics:

- it provides precision stabilization of the MOSFET regime and its digital variation for automatic measurements and selection of optimum current and voltages, and voltage gain autocalibration;

- a digital CDS-processor with fast ADC and DSP, which measures the noise power spectrum and its correlation function to define the number of samples, and corrects nonlinearity in real time;

- the maximum throughput of the system is 50 Mpixel/s with the use of fibre-optics connection in the Fibre Channel standard.

This work is supported by RFFI (project 95-02-04640).

## REFERENCES

Cobbold R.S.C., Theory and applications of field-effect transistors, New York, Wiley, 1970.