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비용장 오류 정정과 궤환결합을 갖는 차동 검파 시스템 (Differential Detection Systems with Nonredundant Error Correction and Feedback Combining)

韓 榮 烈 *

(Youngyearl Han)

요 약

본 논문에서는, 차동MSK와 GMSK 시스템을 위한 기존차동검파기의 k개의 연속적인 출력과 k-심볼 주기 지인을 갖는 차동검파기 출력사이의 관계를 고찰한다. 기존차동검파기의 연속적인 k개의 출력, k-심볼 주기 인소자를 갖는 검파기의 출력의 곱과 이원가산에는 주기성이 존재함을 알 수 있다. 이 관계들은 기존차동검파의 성능이득을 구하는데 사용되어졌다. 이 방법의 오율성능분석은 컴퓨터 모의 실험에 의해 이루어졌고, 차동 MSK와 GMSK 시스템의 성능을 향상시켰다.

Abstract

In this paper, the relationship between k consecutive outputs of the conventional differential detector and output of differential detector with k-symbol periods delay for differential MSK and GMSK systems is investigated. It is shown that there exists periodicity in modulo-2 sum and product of k successive outputs of the conventional differential detector with the output of a detector with k-symbol periods delay circuit.

This relationships are used to achieve performance gains over conventional differential detection. The error rate performance of the method is carried out by computer simulation and performance improvement is achieved for differential MSK and GMSK systems.

I. Introduction

Differentially coherent detection is widely employed in the digital radio systems because of simple circuit configurations. However, it is known that the bit error rate (BER) performance of differential detection in an additive white Gaussian channel is generally

inferior to coherent detection. But the scheme does not require the acquisition of a local reference signal in phase coherence with the received carrier.

In the past, in order to improve the system error rate performance of differential detection several methods have been proposed by taking into consideration the difference in the carrier phase between two received signals separated by two or more symbol periods^{[1]-[4]}.

Masamura et al^[2] has shown that, for an MSK signal, the outputs of conventional,

* 正會員, 漢陽大學校 電子通信工學科

(Dept. of Elec. Communication Eng., Hanyang University)

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detector and a detector with a two symbol periods delay circuit correspond to the data and parity, respectively, of a single error correcting self-orthogonal convolutional code.

Makrakis et al^[4] introduces a receiver structure which improves the BER performance of DMSK system. It uses combining with feedback to add the signal samples from conventional detector with 2-symbol periods delay.

The scheme described utilizes output that employs the received signal delayed by more than two symbol periods in two ways. First, the symbols created from the difference in phase between two successive adjacent symbol intervals is the transmitted data. On the other hand, the symbol appearing at the output of the differential detector which uses a k-symbol periods delay forms the parity bit. Furthermore, with n data outputs of the conventional differential detector and n parity outputs of the k-symbol periods delayer differential detection, (2n,n) systematic orthogonalizable convolutional code can be generated. Secondly the receiver utilizes the outputs of the detector with k-symbol periods delay which contains the information about the transmitted data. It uses combining with feedback to add the signal samples from conventional and k-symbol periods delay circuits. The error rate performance of the nonredundant error correction and feedback combining methods are carried out by Monte Carlo simulation method and the error rate performance of the two methods are compared. The remainder of this paper is presented as follows. The next section gives a brief overview of the MSK signal and derivation of the relationship between the k output sequence of the conventional differential detection and the output of the differential detector which uses a k-symbol periods delay. The application to DMSK and DGMSK with error rate performance are discussed in setion 3. Finally, in section 4, we conclude our study on differential detector with nonredundant

error correction and feedback combining.

II. K-TH Order Differential Detection of MSK

An MSK signal can be expressed in the general form

$$x(t) = A \cos[\omega_c t + \theta + \phi_k + 2\pi f_d a_k(t - kT)] \quad (1)$$

where A and T are the amplitude and bit duration, f_c is the carrier frequency, θ is an arbitrary carrier phase which can be set to zero. The parameter f_d equals the frequency shift away from f_c . f_d and ϕ_k are given by

$$f_d = \frac{1}{4T} \quad (2)$$

$$\phi_k = \frac{\pi}{2} \sum_{j=0}^{k-1} a_j \quad (3)$$

Equation (3) can be also written as

$$\phi_k - \phi_{k-i} = \frac{\pi}{2} \sum_{j=0}^{i-1} a_{k-j} \quad (4)$$

If the phase path of an MSK signal is plotted versus t, as shown in Figure 1, it follows that it is piecewise linear and increases or decreases exactly $\pi/2$ radians each T seconds. Lines with positive slope represent binary message 1 and lines with negative slope represent binary message sequence 11000111 is shown by heavy line in Figure 1.

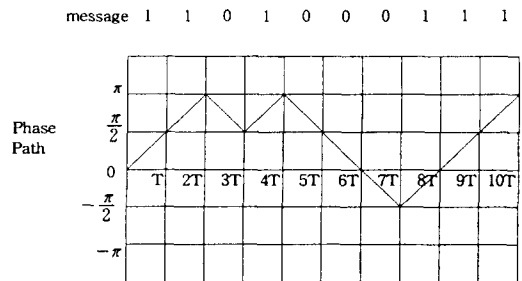


그림 1. MSK신호 대 t의 위상경로
Fig. 1. Phase path of an MSK signal versus t.

The conventional differential detector corre-

sponds to detector with one symbol period delay. Transmitted data is detected from the phase difference between the successive adjacent signaling by using sine phase comparator. The sine phase comparator output at the sampling instant of the conventional detector in the absence of noise is

$$\sin(\phi_k - \phi_{k-1}) = \sin\left(\frac{\pi}{2} a_k\right) = a_k, \quad a_k = \pm 1 \quad (5)$$

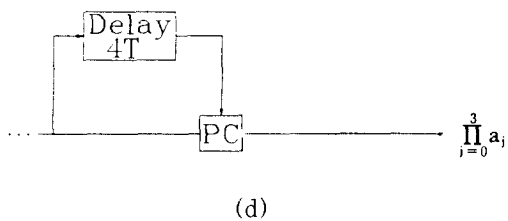
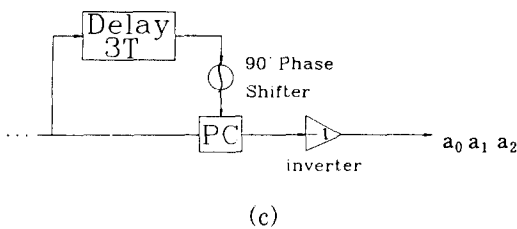
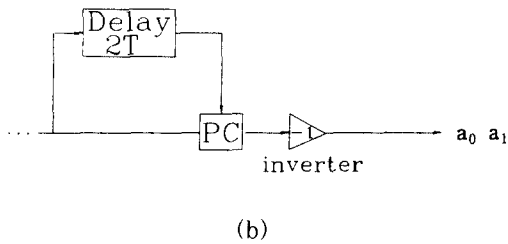
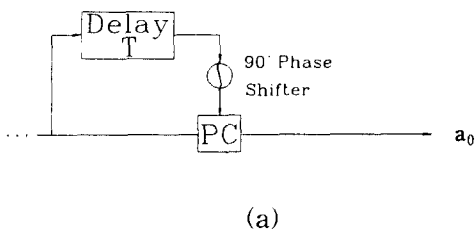


그림 2. 지연기를 갖는 차동검파기
 (b),(c) 반전기가 있는 검파기
 (a)(d) 반전기가 없는 검파기

Fig. 2. Differential detectors with delay.

(b),(c) detectors with inverter.

(a),(d) detectors without inverter.

The relationship between the multiplication of successive output a_k 's from the conventional detector and the output of current received signal and its replica delayed by k -symbol periods in the carrier phase are shown in Figure 2.

PC is a phase comparator which is composed of multiplier and low-pass filter. Inverter inverts the sense of the output with respect to the input.

The output of inverter takes the value of +1 for input -1 and -1 for input +1. In general, the relationship between the number of delay and output of a detector with k -symbol periods delay at the i -th instant is given in Table 1.

표 1. DMSK에서 i 번째 순간의 지연기의 수와 검파기 출력사이의 곱의 관계

Table 1. Product relationship between the number of delay and output of detector at the i th instant for DMSK.

configuration	number of delay	output of detector
(a)	$1 + 4(n-1)$	$\prod_{j=0}^{4(n-1)} a_{k-j}, n \geq 1$
(b)	$2 + 4(n-1)$	$-\prod_{j=0}^{1+4(n-1)} a_{k-j}, n \geq 1$
(c)	$3 + 4(n-1)$	$-\prod_{j=0}^{2+4(n-1)} a_{k-j}, n \geq 1$
(d)	$4 + 4(n-1)$	$\prod_{j=0}^{3+4(n-1)} a_{k-j}, n \geq 1$

Theorem 1

Following relationships hold for MSK. That is: the value of cosine function at the odd multiple of sampling time and the value of sine function at the even multiple of sampling time are zero.

$$\cos\left(\frac{\pi}{2} \sum_{j=0}^{2p} a_{k-j}\right) = 0 \quad (6)$$

$$\sin\left(\frac{\pi}{2} \sum_{j=0}^{2p+1} a_{k-j}\right) = 0 \quad (7)$$

where $a_{k-j} = \pm 1$ and p is a positive integer.

Proof

We will prove equation (6).

$$\cos\left(\frac{\pi}{2} \sum_{j=0}^{2p} a_{k-j}\right) = \cos\left[\frac{\pi}{2}(a_k + a_{k-1} + a_{k-2} + \dots + a_{k-2p})\right] \quad (8)$$

If we assume that the number of $a_k = +1$ is r and the number of $a_k = -1$ is $(2p+1-r)$, then

$$\begin{aligned} \cos\left(\frac{\pi}{2} \sum_{j=0}^{2p} a_{k-j}\right) &= \cos\left[\frac{\pi}{2}(r \cdot (+1) + (2p+1-r) \cdot (-1))\right] \\ &= \cos\left[\frac{\pi}{2}(2r - 2p - 1)\right] \\ &= \cos\left[\frac{\pi}{2}(2(r-p) - 1)\right] \\ &= \cos\left[\pi(r-p) - \frac{\pi}{2}\right] \end{aligned} \quad (9)$$

By using trigonometric identity, we have

$$\begin{aligned} \cos\left(\frac{\pi}{2} \sum_{j=0}^{2p} a_{k-j}\right) &= \cos[(r-p)\pi] \cos\left(\frac{\pi}{2}\right) \\ &\quad + \sin[(r-p)\pi] \sin\left(\frac{\pi}{2}\right) \end{aligned} \quad (10)$$

since $\cos(\frac{\pi}{2}) = 0$ and $\sin[(r-p)\pi] = 0$, we obtain

$$\cos\left(\frac{\pi}{2} \sum_{j=0}^{2p} a_{k-j}\right) = 0$$

In the similar fashion we have equation (7).

Theorem 2

For the differential MSK detection, following relationship hold between the outputs of the conventional detector and the detector with $[m+4(n-1)]$ symbol delay, where $m=1,2,3,4$ and $n \geq 1$.

$$\sin(\phi_k - \phi_{[k-(1+4(n-1))]}) = \prod_{j=0}^{4(n-1)} a_{k-j}, \quad n \geq 1. \quad (11)$$

$$\cos(\phi_k - \phi_{[k-(2+4(n-1))]}) = - \prod_{j=0}^{1+4(n-1)} a_{k-j}, \quad n \geq 1. \quad (12)$$

$$\sin(\phi_k - \phi_{[k-(3+4(n-1))]}) = \prod_{j=0}^{2+4(n-1)} a_{k-j}, \quad n \geq 1. \quad (13)$$

$$\cos(\phi_k - \phi_{[k-(4+4(n-1))]}) = \prod_{j=0}^{3+4(n-1)} a_{k-j}, \quad n \geq 1. \quad (14)$$

Proof

We will prove equation (11) by mathematical induction. From equation (3), we have

$$\phi_k = \frac{\pi}{2} \sum_{j=0}^{k-1} a_j$$

which can be also written as

$$\phi_k - \phi_{k-1} = \frac{\pi}{2} \sum_{j=0}^{k-1} a_{k-j}$$

For the $[1+4(n-1)]$ th order detector, we have

$$\phi_k - \phi_{[k-(1+4(n-1))]} = \frac{\pi}{2} \sum_{j=0}^{4(n-1)} a_{k-j} \quad (15)$$

By taking sine function on both side, we obtain

$$\sin(\phi_k - \phi_{[k-(1+4(n-1))]}) = \sin\left(\frac{\pi}{2} \sum_{j=0}^{4(n-1)} a_{k-j}\right) \quad (16)$$

Let $p(n)$ be the statement

$$\sin(\phi_k - \phi_{[k-(1+4(n-1))]}) = \sum_{j=0}^{4(n-1)} a_{k-j} \quad (17)$$

We will prove by induction that $p(n)$ is true for all positive integer n . When $n=1$, we have

$$\sin(\phi_k - \phi_{[k-(1+4(n-1))]}) = \sin\left(\frac{\pi}{2} a_k\right) = a_k \quad (18)$$

Suppose that $p(r)$ is true

$$\sin(\phi_k - \phi_{[k-(1+4(n-1))]}) = \sum_{j=0}^{4(r-1)} a_{k-j} \quad (19)$$

We wish to deduce that $p(r+1)$ is true. When $n=r+1$, we have

$$\sin(\phi_k - \phi_{[k-(1+4(r+1-1))]}) = \sin\left(\frac{\pi}{2} \sum_{j=0}^{4r} a_{k-j}\right) \quad (20)$$

We see that the right-hand side becomes by using the trigonometric identity.

$$\begin{aligned} \sin\left(\frac{\pi}{2} \sum_{j=0}^{4r} a_{k-j}\right) &= \sin\left[\frac{\pi}{2} \sum_{j=0}^{4(r-1)} a_{k-j} + \frac{\pi}{2} \sum_{j=4(r-1)+1}^{4r} a_{k-j}\right] \\ &= \sin\left(\frac{\pi}{2} \sum_{j=0}^{4(r-1)} a_{k-j}\right) \cos\left(\frac{\pi}{2} \sum_{j=4(r-1)+1}^{4r} a_{k-j}\right) \\ &\quad + \cos\left(\frac{\pi}{2} \sum_{j=0}^{4(r-1)} a_{k-j}\right) \sin\left(\frac{\pi}{2} \sum_{j=4(r-1)+1}^{4r} a_{k-j}\right) \end{aligned} \quad (21)$$

Since $\sin(\phi_k - \phi_{[k-(1+4(r-1))]}) = \prod_{j=0}^{4(r-1)} a_{k-j}$ and $\cos(\frac{\pi}{2} \sum_{j=0}^{4(r-1)} a_{k-j}) = 0$ from theorem 1, this yields

$$\begin{aligned} \sin\left(\frac{\pi}{2} \sum_{j=0}^{4r} a_{k-j}\right) &= \sin\left(\frac{\pi}{2} \sum_{j=0}^{4(r-1)} a_{k-j}\right) \cos\left(\frac{\pi}{2} \sum_{j=4(r-1)+1}^{4r} a_{k-j}\right) \\ &= \prod_{j=0}^{4(r-1)} a_{k-j} \left[\cos\left(\frac{\pi}{2} a_{[k-4(r-1)-1]}\right) + \frac{\pi}{2} \sum_{j=4(r-1)+2}^{4r} a_{k-j} \right] \\ &= \prod_{j=0}^{4(r-1)+1} a_{k-j} \left[-\sin\left(\frac{\pi}{2} a_{[k-4(r-1)-2]}\right) + \frac{\pi}{2} \sum_{j=4(r-1)+3}^{4r} a_{k-j} \right] \\ &= \prod_{j=0}^{4(r-1)+2} a_{k-j} \left[\sin\left(\frac{\pi}{2} a_{[k-4(r-1)-3]}\right) \sin\left(\frac{\pi}{2} a_{[k-4(r-1)-4]}\right) \right] \\ &= \prod_{j=0}^{4r} a_{k-j} \end{aligned} \quad (22)$$

By applying the same procedure to the detector with $[2+4(n-1)]$, $[3+4(n-1)]$ and $[4+4(n-1)]$ symbol period delay, we obtain the desired formulas.

Let the sequence a_k be related to the binary message sequence m_k by

$$a_k = 2(m_k - 0.5), \quad m_k = 1, 0$$

The relationship between the modulo-2 sum of successive output m_k 's from the conventional detector and the output of the current receives signal and its replica delayed by k -symbol periods in the carrier phase are shown in Figure 3.

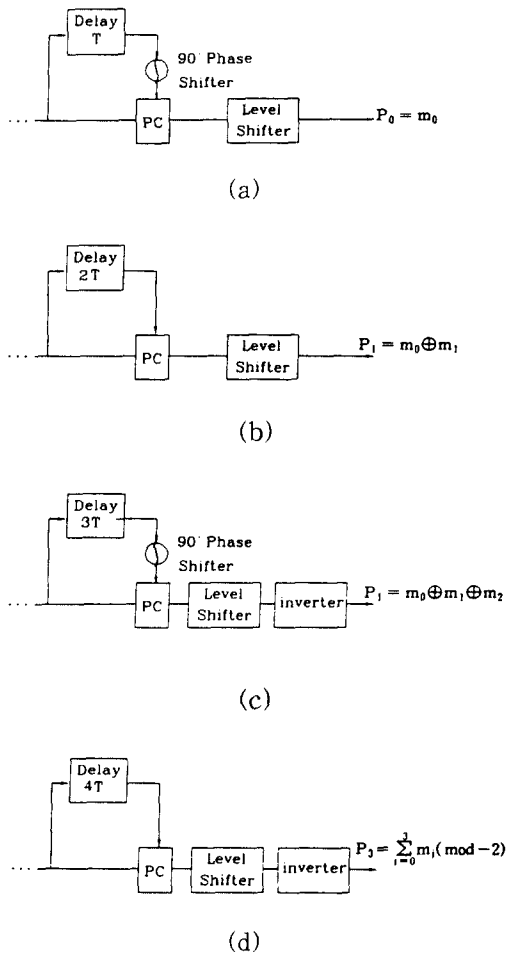


그림 3. 지연기를 갖는 차동검파기
(a),(c) 90° 위상 천이기가 있는 검파기

(b),(d) 90° 위상 천이기가 없는 검파기

Fig. 3. Differential detectors with delay.
(a),(c) detectors with 90° phase shifter.
(b),(d) detectors without 90° phase shifter.

These can be easily deduced from the outputs of detector with k -symbol periods delay in Figure 2. In Figure 3, level shifter shifts level -1 to 0 and level 1 remains same.

표 2. DMSK에서 1번째 순간의 지연기 수와 검파기 출력사이의 이원가산의 관계

Table 2. Modulo-2 sum relationship between the number of delay and output of detector at the i th instant for DMSK.

configuration	number of delay	output of detector
(a)	$1+4(n-1)$	$\sum_{j=0}^{4(n-1)} m_{i-j} \pmod{-2}, n \geq 1$
(b)	$2+4(n-1)$	$\sum_{j=0}^{4(n-1)} m_{i-j} \pmod{-2}, n \geq 1$
(c)	$3+4(n-1)$	$\sum_{j=0}^{4(n-1)} m_{i-j} \pmod{-2}, n \geq 1$
(d)	$4+4(n-1)$	$\sum_{j=0}^{4(n-1)} m_{i-j} \pmod{-2}, n \geq 1$

The relationship between the number of delay of detector and output of the detector with k -symbol periods delay at the i th instant is given in Table 2. Hence, if we compare not only two consecutive symbols but also two alternate symbols, the results can be used for nonredundant error correction.

If a premodulation baseband Gaussian low pass filter is added to an MSK modulator which is a continuous-phase digital FM with a modulation index 0.5, GMSK signal can be obtained. A GMSK signal can be detected by differential detector which is exactly the same as for MSK. With GMSK signaling, instantaneous frequency and phase is affected depending on the introduction of premodulation LPF.

III. Application DMSK AND GMSK Systems

(a) Nonredundant Error Correction Method
Differential MSK system with double error correction circuit is constructed to improve

the performance. In coherent demodulation an error is caused when the noise shifts the phase of the signal into the error region. In differential demodulation an error is caused when the sum of noise phases in two consecutive bit intervals shifts the differential signal into the error region. The non-redundant error correction circuitry exploits the fact that if the sum of noise sample in two consecutive intervals causes an error, the sum of noise samples in two alternate intervals does not necessarily cause an error. The illustrative demodulators with corresponding single^[2] and double error correction circuit diagram are shown in Figures 4 and 5, respectively.

If the received data and parity bit at the i th decision instant are represented by D_i and P_i respectively, the relationship between D_i and P_i for the single error correction circuit in Figure 4 is

$$P_i = D_i \oplus D_{i-1} \tag{23}$$

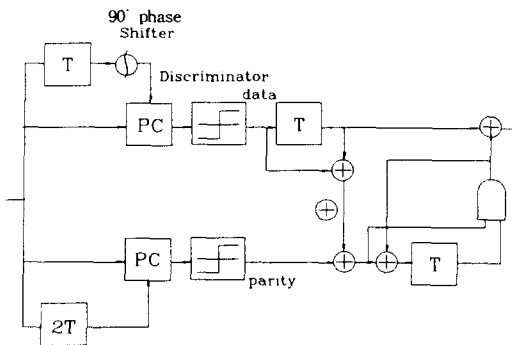


그림 4. 단일오류정정회로가 있는 복조기
Fig. 4. Demodulator with single error correction circuit.

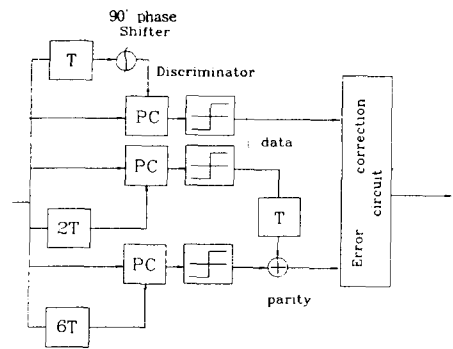
where \oplus denotes the modulo-2 sum. This corresponds to the (2,1) single error correcting self-orthogonal convolutional code^{[5], [6]} whose syndromes are given as follows

$$S_i = e_{D_i} \oplus e_{D_{i-1}} \oplus e_{P_i} = e_{D_i} \oplus e_{P_i} \oplus e_{D_{i-1}} \tag{24}$$

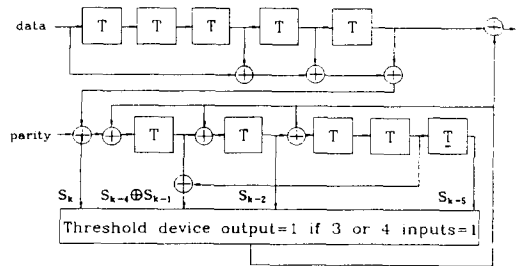
$$S_{i-1} = e_{P_{i-1}} \oplus e_{D_{i-1}} \tag{25}$$

e_{D_i} and e_{P_i} represent error variable, whose value is 1 when there is an error and 0 otherwise. When the number of nonzero elements among e_{D_i} , e_{P_i} and $e_{P_{i-1}}$ is less than one, it corrects one error. The relationship between D_i and P_i for the double error correcting circuit in Figure 5 is

$$P_i = D_i \oplus D_{i-3} \oplus D_{i-4} \oplus D_{i-5} \tag{26}$$



(a)



(b)

그림 5. 이중오류정정회로가 있는 복조기

(a) 복조기의 블럭도

(b) 이중오류정정회로

Fig. 5. Demodulator with double error correction circuit.

(a) block diagram of demodulator.

(b) double error correction circuit.

The parity bit is obtained as follows. The output of the detector with 6 bit delay is $D_i \oplus D_{i-1} \oplus D_{i-2} \oplus D_{i-3} \oplus D_{i-4} \oplus D_{i-5}$. The output of the detector with 2 bit delay delayed by T second

is $D_{i-1} \oplus D_{i-2}$. The modulo-2 sum of the outputs from the detector with 6 bit delay and detector with 2 bit delay delayed by T second is $D_i \oplus D_{i-3} \oplus D_{i-4} \oplus D_{i-5}$, which is a parity bit. This corresponds to the (2,1) double error correcting orthogonalizable convolutional code^[6]. Syndromes are formed as follows

$$\begin{cases} S_i = e_{D_i} \oplus e_{D_{i-1}} \oplus e_{D_{i-3}} \oplus e_{D_{i-4}} \oplus e_{D_{i-5}} \\ S_{i-2} = e_{D_{i-1}} \oplus e_{D_{i-3}} \oplus e_{D_{i-4}} \oplus e_{D_{i-5}} \\ S_{i-2} = e_{D_{i-2}} \oplus e_{D_{i-5}} \\ S_{i-3} = e_{D_{i-3}} \oplus e_{D_{i-4}} \\ S_{i-4} = e_{D_{i-4}} \oplus e_{D_{i-5}} \\ S_{i-5} = e_{D_{i-5}} \oplus e_{D_{i-4}} \end{cases} \quad (27)$$

We consider the set of equations S_i, S_{i-2}, S_{i-5} and the modulo-2 sum of $(S_i \oplus S_{i-4})$.

$$\begin{cases} S_i = e_{D_i} \oplus e_{D_{i-1}} \oplus e_{D_{i-3}} \oplus e_{D_{i-4}} \oplus e_{D_{i-5}} \\ S_{i-2} = e_{D_{i-1}} \oplus e_{D_{i-3}} \oplus e_{D_{i-5}} \\ S_i \oplus S_{i-4} = e_{D_{i-1}} \oplus e_{D_{i-3}} \oplus e_{D_{i-4}} \oplus e_{D_{i-5}} \\ S_{i-5} = e_{D_{i-5}} \oplus e_{D_{i-4}} \end{cases} \quad (28)$$

These equations have two important properties.

- 1) Each equation contains $e_{D_{i-5}}$, the error in the first data
- 2) No other data error occurs in more than one equation.

Such set of equation is said to be orthogonal on $e_{D_{i-5}}$. If $e_{D_{i-5}} = 1$ and no other error occur, all the syndromes will be 1. If any other error variable is 1 alone among 12 error variables, one equation in (28) will be 1 and other three equations will be 0. If $e_{D_{i-5}} = 1$ and any other variable is 1 among the 12 error variables, three equations are 1 and the three is a 0. Finally, if $e_{D_{i-5}} = 0$ but two other error variables are 1, at most two equations of (28) will be 1, since each such error term occurs in one equation. Thus it is clear that $e_{D_{i-5}} = 1$ if three or four of the equation (28) equal 1. It corrects errors when the number of nonzero elements among 12 error variables is less than two.

(b) Feedback combining method

The receiver structure is based on the

observation that the estimate of a_k , \hat{a}_k , can be obtained from the outputs of the conventional detector and detector with 2-symbol periods delay which contain the information about the input symbol a_k ^[4].

In the absence of noise, the estimate \hat{a}_k can be obtained

$$\hat{a}_k = \text{sgn}[a_k + \hat{a}_{k-1}(a_{k-1} \cdot a_k)] \quad (29)$$

where $\text{sgn}(x)$ indicates that the decision is based on the sign of x . a_k is the output of conventional detector in the noiseless situation. \hat{a}_{k-1} is the estimate of a_{k-1} of previous symbol which takes the values of +1 or -1. $(a_{k-1} \cdot a_k)$ is the output of the detector with 2-symbol periods delay.

When $\hat{a}_{k-1} = a_{k-1}$ and $\hat{a}_{k-1} \cdot a_{k-1} = 1$ in noiseless situation, \hat{a}_k becomes

$$\hat{a}_k = \text{sgn}(2a_k) \quad (30)$$

Since a_k can be taken only +1 or -1, $2a_k$ takes the value of +2 or -2. The receiver structure which performs the operation of Equation (29) is shown in Figure 6.

The input of the hardlimiter is compared with reference and the output is digitized into one of two states: +1 and -1. Extension of this procedure is straightforward using k -symbol periods delay.

$$\hat{a}_k = \text{sgn}[a_k + \hat{a}_{k-1} \cdot (a_{k-1} \cdot a_k) + \hat{a}_{k-1} \cdot \hat{a}_{k-2} \cdot (a_{k-2} \cdot a_{k-1} \cdot a_k) + \dots + \hat{a}_{k-1} \cdot \hat{a}_{k-2} \cdot \dots \cdot \hat{a}_{k-n} \cdot (a_{k-n} \cdot \dots \cdot a_{k-1} \cdot a_k)] \quad (31)$$

In the absence of noise, \hat{a}_k becomes

$$\hat{a}_k = \text{sgn}[n \cdot a_k] \quad (32)$$

Extended form of DMSK detector block diagram with feedback combining is shown in Figure 7.

The dotted rectangle over the 90° phase shifter and inverter at the last stage in Figure 7 indicates that its existence depends on the number of delayer of the detector.

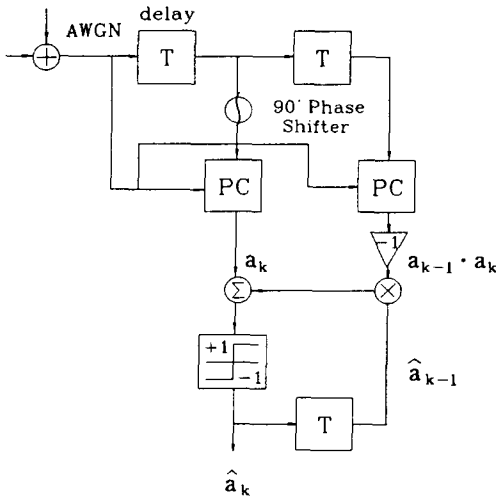


그림 6. 2-심볼 주기 지연을 갖는 차동 검파기의 수신기 구조

Fig. 6. Receiver structure of differential detector with 2-symbol periods delay.

Having described the form of demodulator for DMSK, we now simulate the performance in terms of probability of error in AWGN channel.

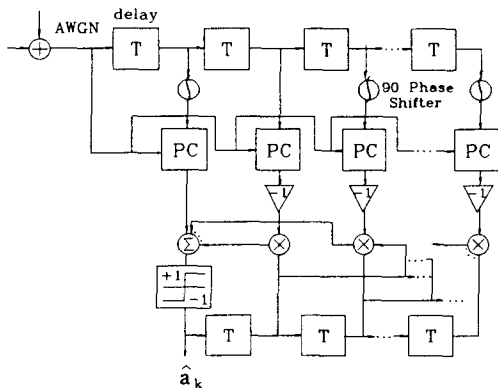


그림 7. k-심볼 주기 지연을 갖는 차동 검파기의 수신기 구조

Fig. 7. Receiver structure of differential detector with k-symbol periods delay.

IV. Simulation Results and Discussion

The probability density function of the carrier phase fluctuation (ψ) due to AWGN is given by ^[7]

$$f(\psi) = \frac{\exp^{-R}}{2\pi} + \frac{1}{2} \sqrt{\frac{R}{\pi}} \exp(-R \sin^2 \psi) \times \cos \psi [1 + \operatorname{erfc}(\sqrt{R} \cos \psi)] \quad (33)$$

$$-\pi \leq \psi \leq \pi$$

To simulate the performance of DMSK with nonredundant error correction and feedback combining, the rejection method is applied. The rejection method is applicable when the probability density function, $f(x)$, has a lower and upper limit to its range, a and b , respectively, and an upper bound c . When the cumulative distribution can not be integrated and inverted, the rejection method is a convenient method of generating random numbers of the desired probability density function. The method can then be specified as follow

- 1) Compute the values of two independent uniformly distributed variables u_1 and u_2
- 2) Compute $X_0 = a + u_1(b - a)$, $Y_0 = cu_2$
- 3) If $Y_0 \leq f(X_0)$, accept X_0 as the desired output, otherwise repeat the procedure with two new uniform variables.

To generate random noise phase, rejection method described above is used. The procedure to evaluate the error rate performance of DMSK is as follows

- 1) Generate a random phase for a given signal to noise ratio for each incoming signal
- 2) The random phase is added to the absolute carrier phase of incoming signal
- 3) The phase difference between two incoming signal to the phase comparator is calculated
- 4) If the phase difference lies in the region which gives correct decisions, no error occurs, otherwise error occurs.

The simulated results for DMSK with non-

redundant error correction are shown in Figure 8. The theoretical coherent and differential coherent demodulation curves are included as reference. Figures 9 and 10 illustrate the bit error rate performance of the differential detection for GMSK with nonredundant error correction for BT products equal to 0.3 and 0.5 respectively. In the computer simulation, the phase angle for intersymbol interference (ISI) was taken 4 bits before and after current symbol.

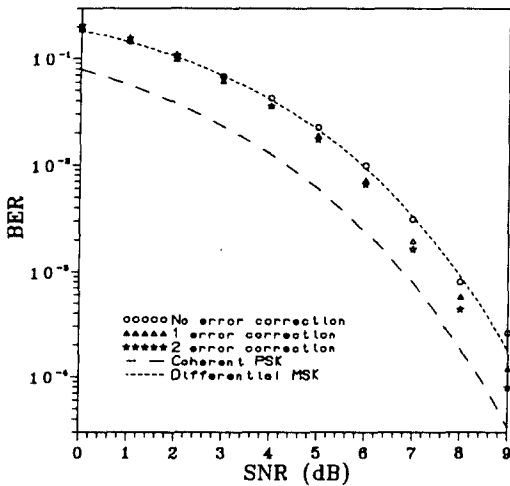


그림 8. 비용상 오류정정을 갖는 DGMSK 복조기의 오율성능(B.T=0.5)
 Fig. 8. Error rate performance of DMSK demodulator with nonredundant error correction

As the BT product increases, the performance is improved as expected approaching the curve of DMSK. Furthermore, significant performance improvement for GMSK with nonredundant error correction is clearly evident from the curves.

The simulated results for DMSK with feedback combining are shown in Figure 11. Here, also the theoretical coherent and differential coherent demodulation curves are included as reference. The error rate performance using 1T, 2T, 3T and 4T delay feedback combining for the BT = 0.3 and 0.5 are plotted in Figure 12 and Figure 13. The

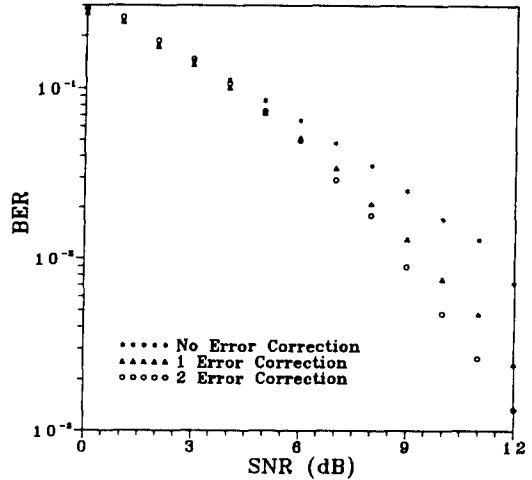


그림 9. 비용상 오류정정을 갖는 DGMSK 복조기의 오율성능(B.T=0.3)
 Fig. 9. Error rate performance of DGMSK demodulator with nonredundant error correction (B.T=0.3)

performance dependence of the number of delayer is clearly seen in Figure 12 and Figure 13.

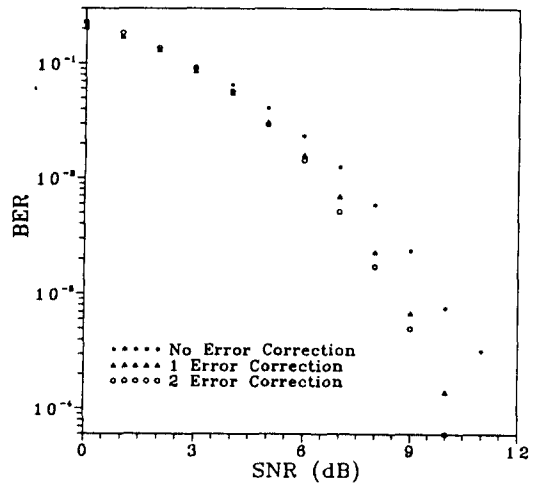


그림 10. 비용상 오류정정을 갖는 DGMSK 복조기의 오율성능(B.T=0.5)
 Fig. 10. Error rate performance of DGMSK demodulator with nonredundant error correction (B.T=0.5).

The error rate performance improvement of double error correction over single error

correction and 2T feedback combining over 1T feedback combining are small for DMSK. But for the DGMSK the error rate performance improvement increases significantly as the number of delayer increases. Overall feedback combining method provided a little better performance improvement over error correction method when the same number of delayer are employed.

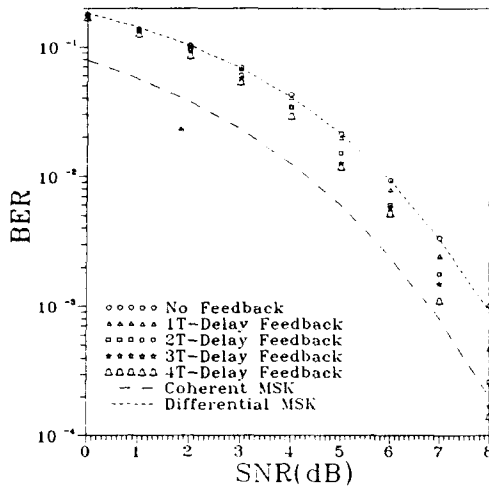


그림 11. 궤환결합을 갖는 DMSK 복조기의 오율 성능
 Fig. 11. Error rate performance of DMSK demodulator with feedback combining.

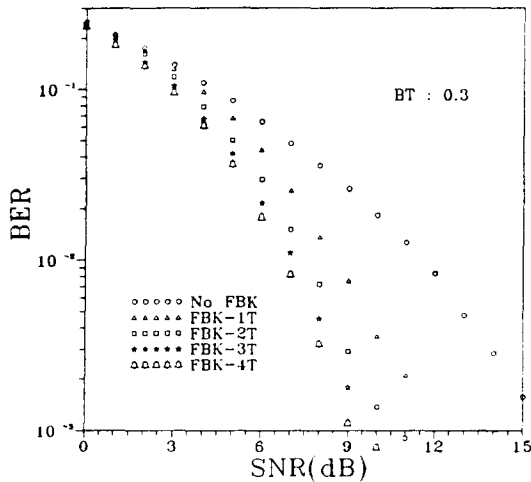


그림 12. 궤환결합을 갖는 DMSK 복조기의 오율 성능(BT=0.3)
 Fig. 12. Error rate performance of DGMSK demodulator with feedback combining (BT=0.3)

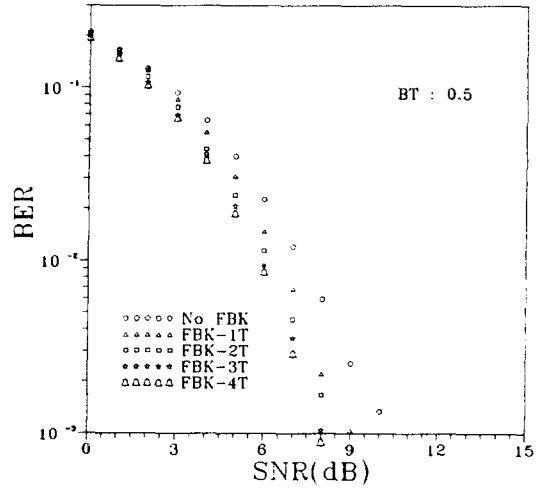


그림 13. 궤환결합을 갖는 DGMSK 복조기의 오율 성능(BT=0.5)
 Fig. 13. Error rate performance of DGMSK demodulator with feedback combining (BT=0.5).

IV. Conclusion

In this paper, the method which improves the performance of a DMSK and DGMSK system employing nonredundant error correction and feedback combining circuits have been described. It utilizes the relationship between the outputs of conventional differential detector and the detector with k-symbol periods delay.

The error correcting method is based on the error correcting orthogonalizable conventional code which can be decoded using simple circuit configuration. Feedback combining method utilizes the output of the detector with k-symbol periods delay which contains the information about the transmitted symbol.

Simulation was performed to verify the improvement of the error rate performance of the differential detection with nonredundant

error correction and feedback combining for DMSK and DGMSK. The simulated results have shown the capability to improve the performance of the differential systems.

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저 자 소 개

韓 榮 烈(正會員)

1938년 6월 10일생. 1960년 서울대학교 전자공학과 학사. 1976년 미주리 대학교 대학원 공학석사. 1979년 미주리 대학교 대학원 공학박사. 1980년 - 현재 한양대학교 전자통신공학과 교수. 1980년 - 1994년 통신공학회 이사, 상임이사, 부회장. 1995년 - 현재 통신공학회 수석 부회장.