[논 문] 한국재료학회지
Korean Journal of Materials Research
Vol. 5, No. 2 (1995)

Characteristics of Low-Temperature Polysilicon Thin Film Transistors

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Abstract Polysilicon thin film transistors (poly-Si TFTs) with different channel dimensions were fabricated on low-temperature crystalized amorphous silicon films and on as-deposited polysilicon films. The electrical characteristics of these TFTs were characterized and compared. The performance of the TFTs fabricated on the solid-phase crystalized amorphous silicon films was shown to be superior to that of the TFTs fabricated on the as-deposited polysilicon films. It was found that the performance of poly Si TFTs depends strongly on the material characteristics of the polysilicon films used as the active layers, but only weakly on the channel dimensions.

1. INTRODUCTION

Polysilicon thin film transistors (poly-Si TFTs) are very attractive for large-area electronics applications such as image sensors and active martrix liquid crystal displays (AMLCDs), since they have higher mobility and reliability and can be integrated into peripheral driving circuits with driving elements, as compared to the amorphous silicon TFTs[1,2]. Recent research efforts in poly-Si TFTs have focused on low-temperature process of building poly-Si TFTs on low-cost glass substrates.

Since the electrical properties of poly-Si TFTs depend on the material characteristics of polysilicon films used as active layers, the formation of high-quality polysilicon films is essential.

Crystallization techniques in formation of polysilicon films at low temperature make use of laser annealing[3], rapid thermal annealing[4] and solid phase crystallization(SPC)[5]. Although requiring a long annealing time, the SPC method has the advantage of both higher uniformity and reproducibility than the other crystalization processes. In this paper, the electrical properties of low-temperature poly-Si TFTs with various channel dimensions using SPC polysilicon films and as-deposited polysilicon films are discussed.

2. EXPERIMENTAL

N-channel polysilicon TFTs with various channel dimensions (W/L=12/16, 12/12, 12/8, 12/6, 12/3, 12/2) were fabricated using the following process steps: A 150nm low-pressure chemical-vapor-deposition (LPCVD) silicon films were deposited in amorphous phase at 550℃ and in polycrystalline phase at 625℃ onto a 500nm SiO_2 layer, which was deposited on a Si substrate by a atomspheric-pressure chemical-vapor-deposition (APCVD) method at 480℃. The amorphous silicon films were crystalized by thermal annealing at 600℃ for 36hrs in the N_2 ambient. After definition of polysilicon islands, a 150nm thick SiO_2 films deposited by APCVD was used as the gate dielectric layer. A 180nm thick layer of silicon film used for gate electrode was deposited by LPCVD at 550℃. After gate patterning, phosphorous ions were implanted at a dose of $5\times10^{15}cm^{-2}$ and at 40 KeV to form the drain, source, and gate regions using the self-alignment technique. After deposition of 300nm thick pure SiO_2, activation annealing was performed at 600℃ for 24hrs in the N_2 ambient. Al(+1% Si) was deposited to form contacts,

and the substrate was annealed at 450℃ for the 1hr in the forming gas.

3. RESULTS AND DISCUSSION

X-ray diffraction was used to study the degree of crystallinity and texture of the as-deposited and SPC polysilicon films. As shown in Fig. 1, the LPCVD silicon films deposited at

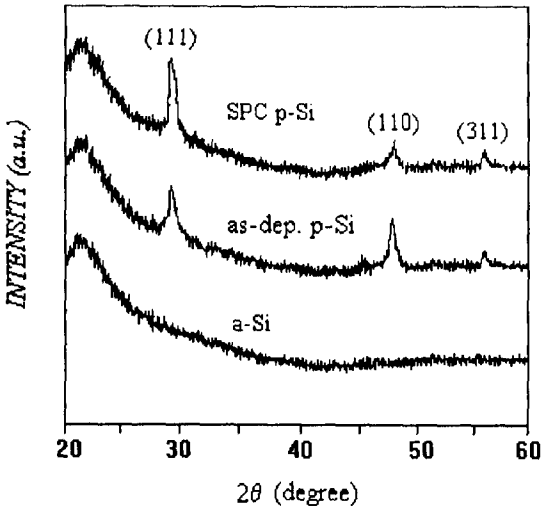

Fig. 1. X-ray diffraction patterns of as-deposited and SPC polysilicon films.

625℃ were mainly polycrystalline with the dominant (110) orientation, which the same type of films deposited at 550℃ were mainly amorphous. For the SPC polysilicon films, the (111) component was greater than the (110) and (311) components. The (111) X-ray diffraction intensity was used to monitor the amorphous to crystalline annealing kinetics. Fig. 2 shows scanning electron microscope (SEM) photographs of LPCVD silicon films. Based on the surface texture, the SPC polysilicon films are smoother than the as-deposited polysilicon films. The as-deposited polysilicon films formed at 625℃ have a columnar structure, while the SPC polysilicon films have dendritic structure. The grain sizes in the polysilicon films can be estimated from the tunneling electron microscope (TEM) micrographs as shown in Fig. 3. The SPC

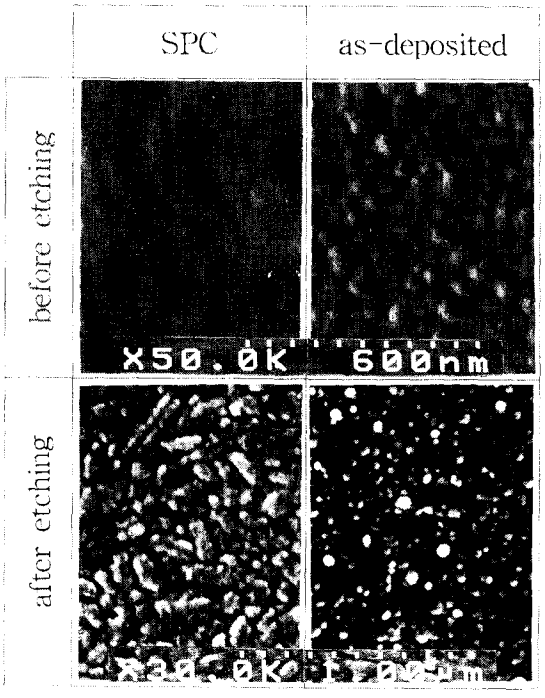

Fig. 2. SEM photographs of as-deposited and SPC polysilicon films.

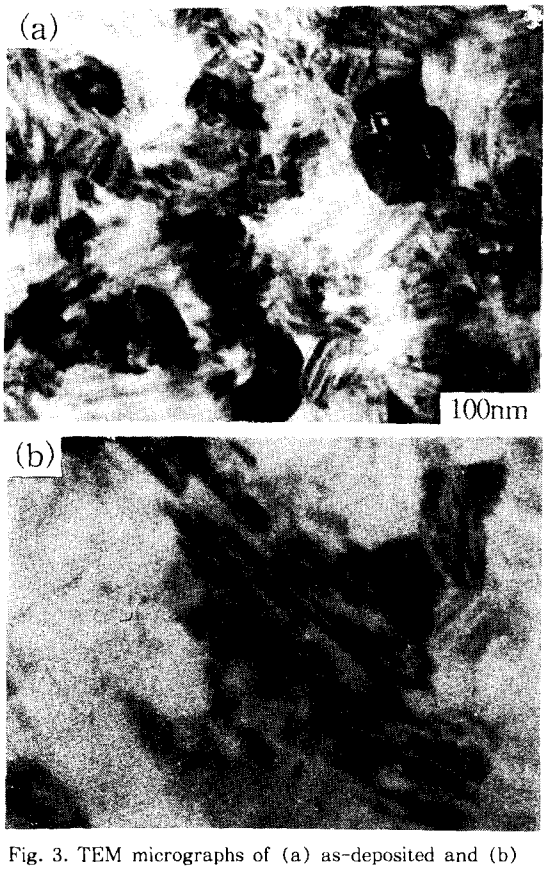

Fig. 3. TEM micrographs of (a) as-deposited and (b) SPC polysilicon films.

polysilicon film has an average grain size of about 5000Å. The as-deposited polysilicon film, on the other hand, shows an average grain size of about 1000Å.

Fig. 4 shows I_D-V_G curves with various channel lengths. The leakage current (I_L) in the n-channel poly-Si TFTs increases when the negative gate voltage (V_G) is increased, and the minimum leakage current decreases linearly with respect to the inverse of the channel length. This indicates that the leakage current is not limited by the reverse-biased p-n^+ junction resistance but by the polysilicon channel resistivity. That is, the leakage current is mainly the field-assisted current via trap states near the drain junction. As the channel length is decreased (from L=16㎛ to L=2㎛), the V_G (at the minimum I_L condition) values decrease from +3.5V to −1.5V for the poly-Si TFTs with SPC polysilicon films and from +9.0V to +6.2V for the poly-Si TFTs with as-deposited polysilicon films. Since the conduction and valence bands are nearly flat at the minimum leakage current condition, the reduction of V_G is likely due to the decrease in grain boundary trap states as a function of decreasing channel length. The overall difference in V_G of the two respective TFTs indicates that the trap states are higher in the as-deposited polysilicon films. In the case of the n-channel poly-Si TFTs, the trap states capture electrons near the surface, and, as the result, the net effect is similar to doping with p-type impurities. According to the I_D-V_G curves at various drain voltages illustrated in Fig. 5(a) and (b), the poly-Si TFTs with SPC polysilicon films have higher drive currents, lower subthreshold slopes, the lower leakage currents than the poly-Si TFTs with as-deposited polysilicon films. This is be

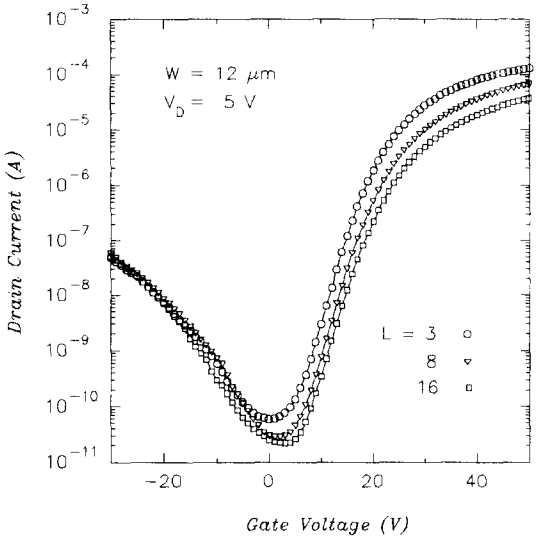

Fig. 4. I_D-V_G curves for polysilicon TFTs with various channel lengths.

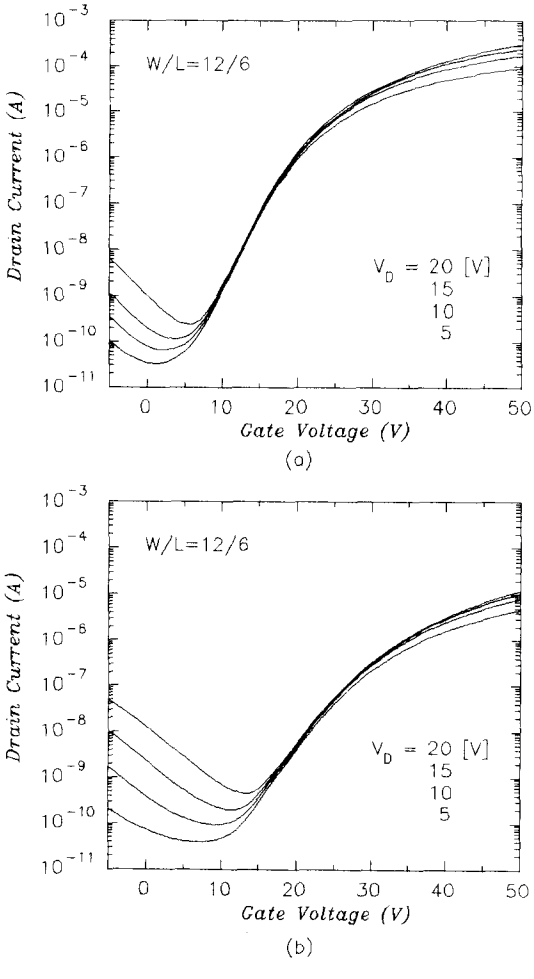

Fig. 5. I_D-V_G curves for polysilicon TFTs (W/L=12/6) with at various drain voltages : (a) SPC and (b) as-deposited polysilicon films.

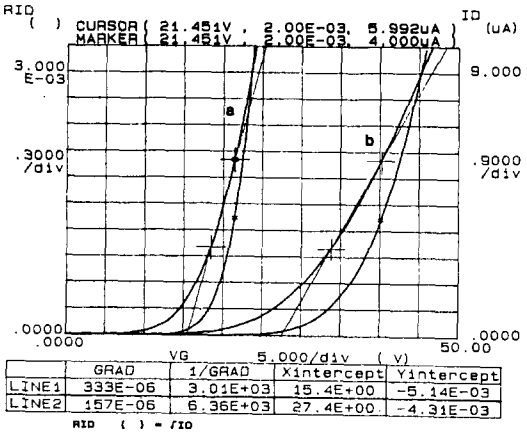

Fig. 6. $\sqrt{I_D}-V_G$ curves for polysilicon TFTs (W/L=12/6) with SPC(a) and as-deposited polysilicon films(b).

cause of the fact that the overall quality of the polysilicon films, i.e, surface smoothness, grain size, etc., is superior in the poly-Si TFTs made of crystalized amorphous silicon films than in those made of as-deposited polysilicon films. At constant gate voltages, the leakage current seems to increase exponentially as a function of the drain voltage (V_D), and the degree of increase is greater in the case of the poly-Si TFTs with as-deposited polysilicon films. These results seem to indicate that the poly-Si TFTs with as deposited polysilicon films have higher trap states, since the trap states are most likely acting as the generation sites for the leakage current. It also shows that the leakage current is strongly dependent on the gate and drain voltages. Fig. 6 represents the threshold voltage (V_{TH}) derived form the slope of the $I_D^{1/2}-V_G$ curve at $I_D^{1/2}=1\,\mu$A and $I_D^{1/2}=4\,\mu$A. Since the threshold voltage is dependent on the thickness of the gate oxide layer and the trap states of the active polysilicon layer, the poly-Si TFTs, because of the thick gate oxides (150nm), have shown a high threshold voltage. It also shows that the threshold voltage is higher in the case of the poly-Si TFTs with as-deposited polysilicon films than in the case of the poly-Si TFTs with SPC polysilicon films, because of higher trap states in the former. Fig. 7 illustrates I_D- and g_m-V_G curves for the poly-Si TFTs with as-deposited and SPC polysilicon films. The transconductance (g_m) value of the poly-Si TFTs with SPC polysilicon films is about ten times higher than that of the poly-Si TFTs with as-deposited polysilicon films. The field-effect mobility was calculated from the transconductance values in the linear region at $V_D=0.2$V.

Table 1 lists key electrical characteristics of poly-Si TFTs with various channel dimensions. Even without hydrogenation treatments, all of the poly-Si TFTs tested have shown excellent electrical properties, regardless of the channel dimensions. The poly-Si TFTs with SPC polysilicon films, of course, have better electrical properties including the lower threshold voltage, higher mobility and higher On/Off current ratio than the poly-Si TFTs with as-deposited polysilicon films. Table 1 also shows that the shorter the channel length, the lower is the threshold voltage and mobility. This can be explained by the short-channel effects due to increasing electric field intensity between the drain and the source as a function of decreasing channel length. These results indicate that the electrical properties of poly-Si TFTs

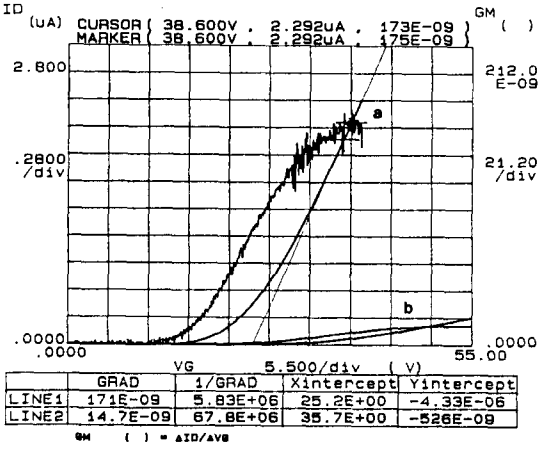

Fig. 7. I_D and g_m-V_G curves for a polysilicon TFTs (W/L=12/6) with SPC(a) and as-deposited polysilicon films.

Table 1. Electrical characteristics of poly-Si TFTs with various channel dimensions.

W/L	SPC			as-deposited		
	V_{TH} [V]	μ_{fe} [$cm^2/V \cdot s$]	ON/OFF current ratio $I(V_G=40V)/I_{min}$	V_{TH} [V]	μ_{fe} [$cm^2/V \cdot s$]	ON/OFF current ratio $I(V_G=40V)/I_{min}$
12/6	18.2	22.6	8.5×10^5	31.1	4.48	2.8×10^4
12/12	17.8	21.8	8.5×10^5	30.2	2.54	3.0×10^4
12/8	16.3	20.3	1.5×10^5	29.1	1.88	3.3×10^4
12/6	15.9	18.7	1.5×10^4	26.0	1.63	3.3×10^4
12/3	13.9	16.0	1.3×10^4	24.2	1.04	4.8×10^4
12/2	13.0	12.7	1.3×10^4	23.0	0.83	5.4×10^4

are mainly governed by the material characteristics of the polysilicon thin films and not significantly by the channel dimensions.

4. CONCLUSION

Using low-temperature crystalized amorphous silicon films and as-deposited polysilicon films as the active layers, n-channel poly-Si TFTs with various channel dimensions were fabricated by a low-temperature process. With respect to key electrical properties, the poly-Si TFTs with SPC polysilicon films are superior to those with as-deposited polysilicon films. This indicates that the surface smoothness, crystal qualities and grain size strongly influence the poly-Si TFTs performance. Except for the channel length less than 6μm, the device dimensions had little effect on electrical properties. In the case of a device with the dimension of W/L=12/16, a mobility of 22.6$cm^2/V \cdot$ sec was achieved with the poly-Si TFTs with SPC polysilicon films even without hydrogenation. With the poly-Si TFTs with as-deposited polysilicon films, the mobility was 4.5$cm^2/V \cdot$sec. These results indicate that high performance poly-Si TFTs could indeed be fabricated by optimizing device structure, improving polysilicon film quality and incorporating hydrogenation.

REFERECNES

1. I. Yudasaka and H. Ohshima, Mat. Res. Soc. Symp. Proc., 182, 333(1990)
3. S. Morozumi, H. Kurihara, T. Takeshita, H. Oka and K. Hasekawa, IEEE Trans. Elec. Dev., ED-32, 1546(1985)
3. S. D. Brotherton, D. J. Meculloch, J. B. Clegg, and J. P. Gowers, IEEE Trans. Elec. Dev., 40, 407(1993)
4. N. T. Tran, M. P. Keyes, S. shiffman, G. Lin and S. J. Fonash, Extended Abstracts of the 1991 International Conference on SSDM, 617(1991)
5. S. Takenaka, M. Kunii, H. Oka and K. Kurihara, Jpn. J. Appl. Phys., 29, L2380 (1990)
6. T. Serikawa and S. Shirai, IEEE Electron Devices, 36, 1929(1989)
7. M. K. Hatalis and D. W. Greve, J. Appl. Phys 63, 2260(1988)
8. J. Hajjar and R. Reif, Journal of Electronics Materials, 19, 1403(1991)
9. N. Yamauchi, J. Hajjar and R. Reif, IEEE Electron Deverices, 38, 55(1991)
10. M. J. Tompson, J. of Non-Crystalline Solids., 137 & 138 1209(1991)
11. W. G. Hawkins, IEEE Transaction on Electron Devices, ED 33(4), 477(1990)