A GaAs Power MESFET Operating at 3.3V Drain Voltage for Digital Hand-Held Phone

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CONTENTS

ABSTRACT

A GaAs power metal semiconductor field effect transistor (MESFET) operating at a voltage as low as 3.3V has been developed with the best performance for digital hand-held phone. The device has been fabricated on an epitaxial layer with a low-high doped structure grown by molecular beam epitaxy. The MESFET, fabricated using 0.8 μm design rule, showed a maximum drain current density of 330 mA/mm at V_{gs} = 0.5V and a gate-to-drain breakdown voltage of 28 V. The MESFET tested at a 3.3 V drain bias and a 900 MHz operation frequency displayed an output power of 32.5-dBm and a power added efficiency of 68%. The associate power gain at 20 dBm input power and the linear gain were 12.5dB and 16.5dB, respectively. Two tone testing measured at 900.00MHz and 900.03MHz showed that a third-order intercept point is 49.5 dBm. The power MESFET developed in this work is expected to be useful as a power amplifying device for digital hand-held phone because the high linear gain can deliver a high power added efficiency in the linear operation region of output power and the high third-order intercept point can reduce the third-order intermodulation.

I. INTRODUCTION

High frequency power MESFETs operating at low voltages [1]-[10] have been actively sought for high performance hand-held phone. It is known that the size and weight of a phone can be reduced by decreasing the number of battery cells. Lithium ion battery has been regarded as a good power supply for next generation hand-held phone. The performance of a lithium ion battery has been significantly improved in recent years and are now displaying state-of-the-art energy density which can enhance calling length of the hand-held phone. The voltage of a battery is normally 3.6V at a stationary state, but decreases to 3.0V toward the end of its life [11].

In order to obtain a high efficiency at low biases of 3.0∼3.6V, both a low knee voltage and a high gate-to-drain breakdown voltage in power amplifying device are required. The low knee voltage entails a wide range of voltage swing of the RF output signal, which attributes to high power added efficiency (PAE) with high output power. In order to apply the power FETs for digital hand-held phone, linearity performance should be high enough to reduce third-order inter-modulation, the magnitude of which is dependent upon the DC characteristics, namely transconductance variation with gate bias. At this point of view, an optimization of channel structure in the MESFET is essentially needed in developing low-voltage operation power MESFET with high PAE.

Recent advances in material preparation and device fabrication techniques have produced *L*-band GaAs power FETs operating at drain voltages of 2.9∼3.6V with respectable output power and efficiencies [4]-[10], but there has been no report on the linearity performance.

In the application of the GaAs power MESFETs to digital mobile communication, low-distortion characteristics are extremely important. The distortion could be reduced by lowering 2nd- and 3rd-order harmonic levels of output power characteristic.

In this paper, we report the state-of-the-art RF performance of a low-high doped GaAs power MESFET with low distortion that has been optimized for highly efficient medium-power operation at a drain bias of 3.3V. The performances are better than the best results reported for both GaAs power MESFET [7] and pseudomorphic heterojunction FET [6]. Especially, the linearity performance of our low-high doped GaAs power MESFET is high enough to be used as a power amplifying device for digital hand-held phone.

II. EXPERIMENTAL

A layer structure was prepared by molecular-beam-epitaxy (MBE) on 3 inch semi-insulating GaAs wafer. The structure consists of a 1μm thick undoped buffer layer, a thin active layer doped to mid $10^{17}/cm^3$ (high-doped layer), a thick active layer doped

to mid $10^{16}/cm^3$ (low-doped layer), and an undoped GaAs layer for surface passivation. Figure 1 shows the material structure. In order to improve power gain by reducing the output conductance, GaAs/AlGaAs superlattices were introduced into the buffer layer. The top layer of undoped GaAs is used for protecting the active channel layer from surface defects created by oxygen chemisorption [12].

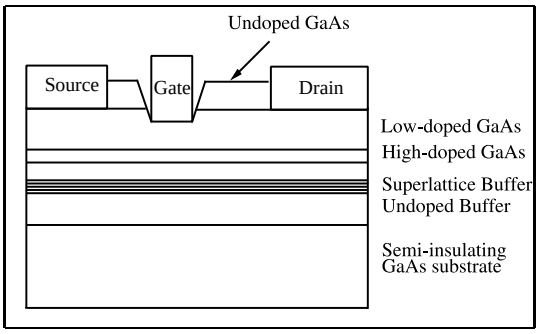

Fig. 1. Structure of low-high doped MESFET.

The thickness of the low-doped layer was designed to be twice larger than the depletion layer width after gate formation. The role of this layer is to decrease the gate capacitance and to improve the Schottky characteristics of the gate metal, which results in high power gain of MESFET. The high-doped layer acts as a main channel for carriers and provides most of the drain current of MESFET. Thickness and doping concentration of this layer determine DC characteristics, such as pinch-off voltage, gate-to-drain breakdown voltage, and transconductance. This layer was made thin to obtain both a uniform transconductance with gate bias and high transconductance at *class AB* bias condition.

MESFETs with a total gate width of 18 mm having 200 μm-wide fingers were fabricated using 3 inch wafer process. In order to decrease source resistance followed by a low knee voltage, gate-to-source spacing was minimized. Figure 2 shows the sequence of the fabrication process of the power FET. First, wet etching was used for device isolation, followed by the formation of AuGe/Ni ohmic contacts. Typical value of specific contact resistance was about $2 \times 10^{-6} \Omega \cdot cm^2$. 0.8 μm gate pattern was defined with image-reversal lithography using *i*-line stepper, and the channel was etched down to deliver the final desired saturation current value. The 0.5 μm-thick Ti/Pt/Au gates were then fabricated. The fabricated FETs were protected with a thin Si_3N_4 and the source pads were connected by airbridge. After thinning the wafer to 100 μm, a gold metal was evaporated on the backside to reduce thermal resistance. All devices were finally passivated using 0.8 μm-thick Si_3N_4 film to enhance reliability.

We obtained a low specific contact resistance of $2 \times 10^{-6} \Omega \cdot cm^2$ without n^+ cap layer, which is comparable to the mean value of the previous reported results with n^+ layer doped to $1.5 \times 10^{18}/cm^3$. That is due to the penetration of ohmic junction into the high-doped channel layer because the junction by AuGe/Ni is formed at depth of 0.2$\sim$0.3 μm below the interface of AuGe/GaAs. The advantage of this process is that low specific contact resistance can be achieved without heavily doped cap

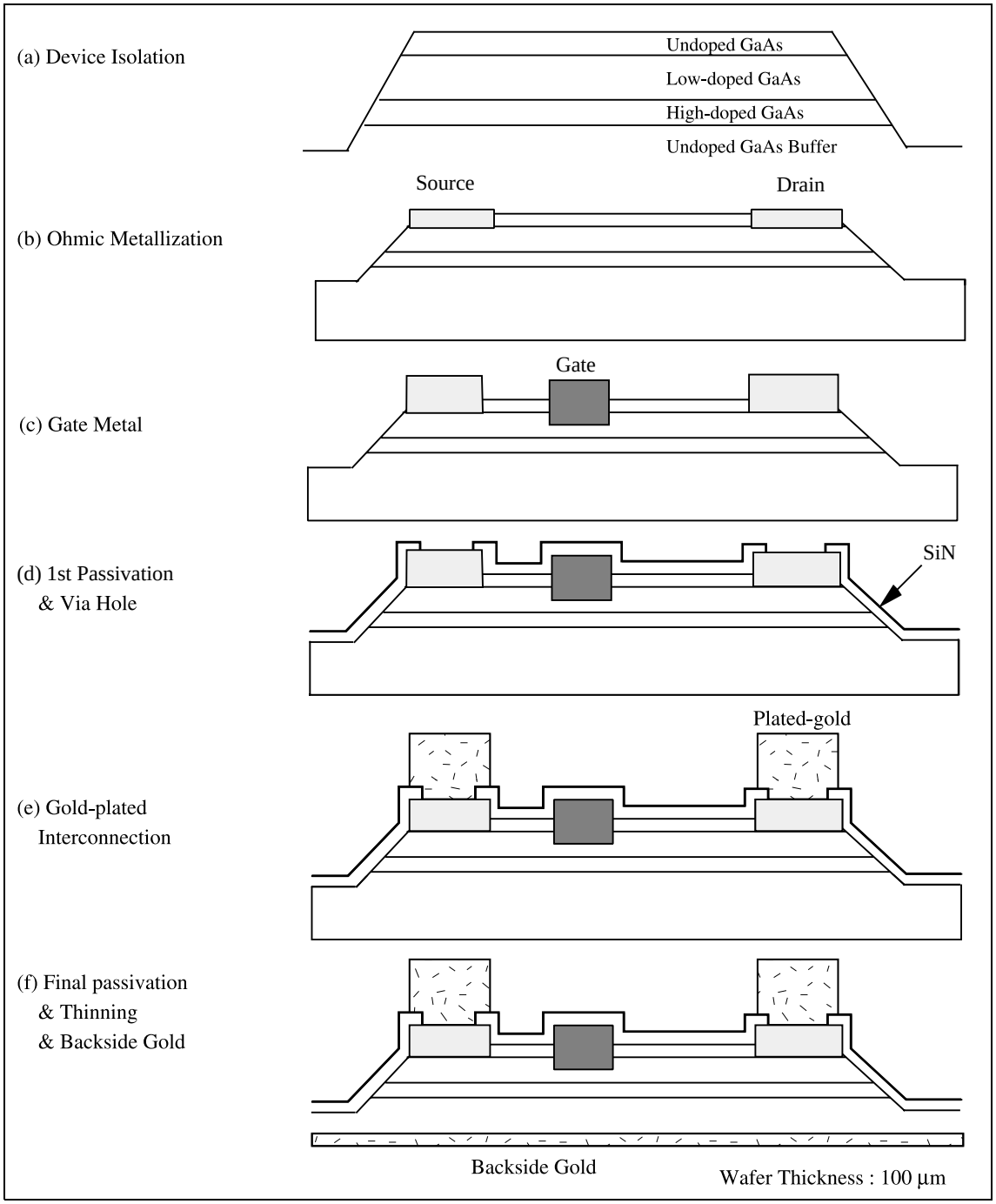

Fig. 2. A schematic processing flow of GaAs power MESFET.

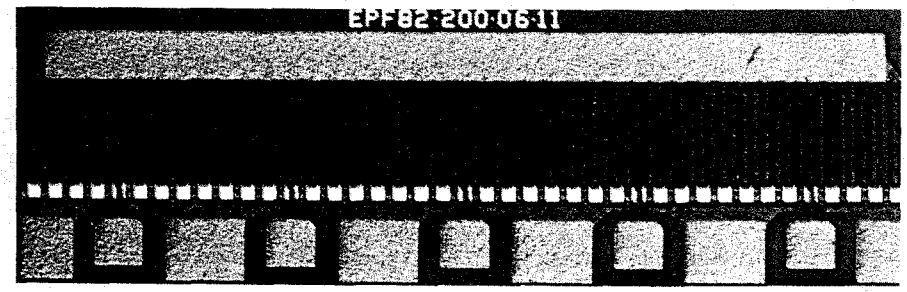

Fig. 3. Photograph for GaAs power MESFET with a gate width of 18 mm and a gate length of 0.8 μm.

cap layer, which will simplify the fabrication process by omitting wide-recess etching process for removal of n^+ cap layer.

Figure 3 is a photography of the fabricated power MESFET. The total gate width is 18 mm. Figure 4 shows the gate area of the FET. The drain side is moved away from the gate to maintain high gate-to-drain breakdown voltage and low output conductance. The source pads between the gates are interconnected by the thick plated-gold.

III. RESULTS AND DISCUSSION

Figure 5 is a typical DC $I_d - V_d$ characteristics of the FET. The maximum drain current, defined as the drain current measured at $V_{gs} = 0.5$V, is 5.0A and maximum current density, $I_{\max}$, is 330mA/mm. A source resistance is measured to be 0.06 Ω, which results in a very low knee voltage of 1.0V at $V_{gs} = +0.5$V.

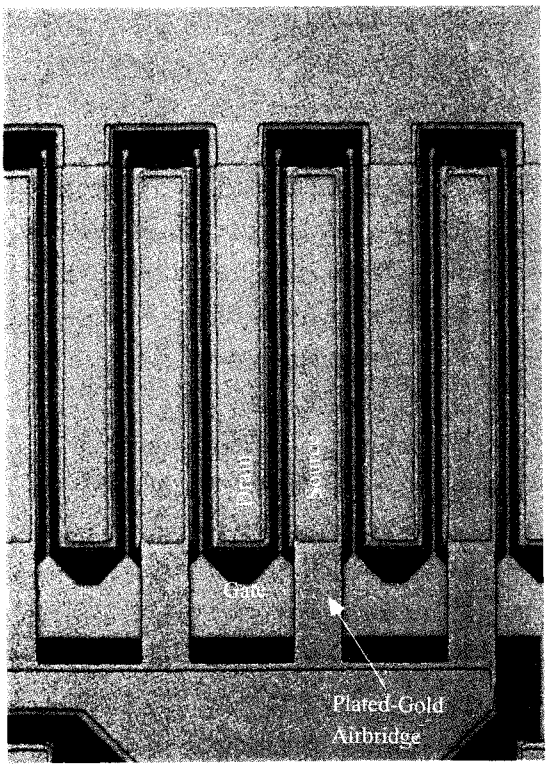

Fig. 4. A photograph of gate area of a GaAs power MESFET.

Especially, the effective knee voltage of 0.3V,

is lower than that of heterojunction pseudomorphic FET (HFET), 0.35∼0.45V [6]. The transconductance is about 110 mS/mm and uniform with the gate voltage of −1.9V to +0.5V, as shown in Fig. 6. The gate-to-drain breakdown voltage (BV_{gd}), measured at a gate current density of 1mA/mm, is 28V, as shown in Fig. 7. This BV_{gd} is higher than that of the MESFET with planar gate structure [5] ($BV_{gd} = 22$V, $I_{\max} = 310$ mA/mm at $V_{gs} = +0.5$V). This value is also higher than that of HFET with an undoped AlGaAs cap layer and a recessed gate structure [6] ($BV_{gd} =$ 21V, $I_{\max} = 220$ mA/mm). This higher value of BV_{gd} is due to the separation of the high-low doped channel layer from the surface defects created by oxygen chemisorption by growing the top layer of undoped GaAs. If the surface defects are created at channel layer, they act as a trapping site for carrier, and cause the reduction of BV_{gd} [12].

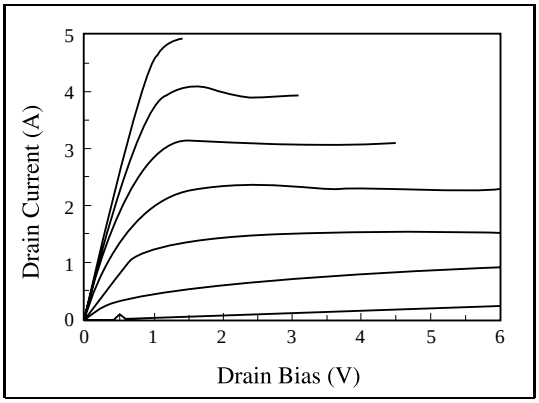

Fig. 5. Typical current-voltage characteristics for GaAs power MESFET with gate width of 18mm. Top curve is for gate voltage of +0.5 V and its step is -0.5 V.

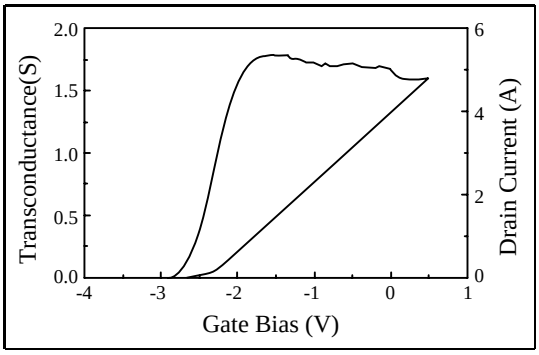

Fig. 6. Transconductance and drain current as a function of gate voltage at a $V_{ds} = 2.0$ V for GaAs power MESFET with gate width of 18mm.

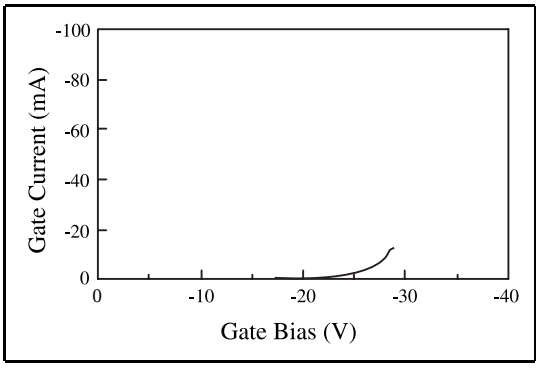

Fig. 7. Gate-to-drain breakdown voltage for GaAs power MESFET with gate width of 18mm.

The current gain cutoff frequency f_t of the 400 μm-wide device (2×200 μm), measured at the bias condition for power operation ($V_{gs} = -2.1$V and $V_{ds} = 3.3$V), was around 18GHz. Power characteristics of the FETs were measured using automated tuner system at 900MHz with a drain bias of 3.3V. The device was operated under *class AB* condition with a bias current of 0.40A, corresponding to 8% of $I_{\max}$. Optimum impedance matching points for both source and load sides were

searched by source pull and load pull methods, followed by power sweeping to measure the power performance of the device. The source and load impedances were $\Gamma = 0.882/-174.8^o$ and $\Gamma = 0.793/-165.8^o$, respectively. An output power of 32.5 dBm and a PAE of 68% were obtained at an input power of 21 dBm, as shown in Fig. 8. Linear power gain and the 1dB gain compression power were measured to be 16.5 dB and 31.0 dBm, respectively. A very linear gain of 16.5 dB was obtained with the input power, as shown in Fig. 9. The constant gain of 16.5 dB was maintained within $\pm$ 0.10 dB at the output power range of 15 $\sim$ 30 dBm. When the drain bias was decreased to 3.0V, an output power of 31.4 dBm with a PAE of 68% was recorded.

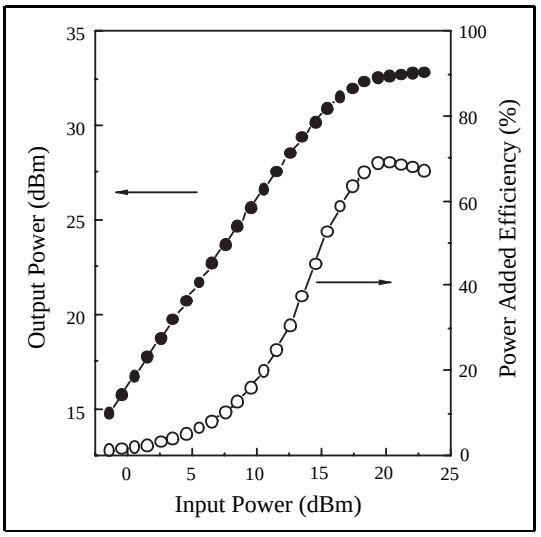

Fig. 8. Output power, power added efficiency, and drain current as a function of input power for GaAs power MESFET with gate width of 18mm. Data were taken at 900MHz at a drain bias of 3.3V.

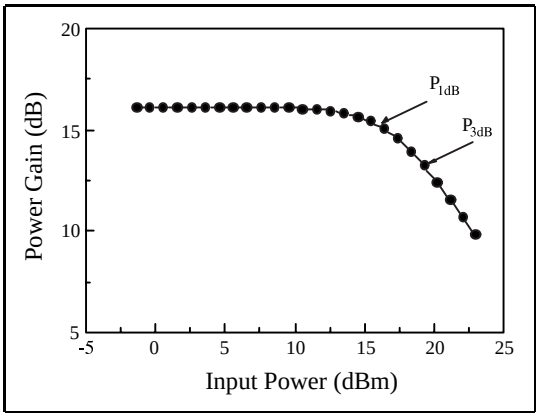

Fig. 9. Power gain as a function of input power for GaAs power MESFET with gate width of 18mm.

The constant transconductance with respect to the gate bias in Fig. 6 implies lower 2nd- and 3rd-order harmonics and results in enhancement of linearity, which is a major requirement in digital radio mobile communications. The 2nd- and 3rd-order harmonics were measured to be -45 dBc and -35 dBc, respectively. In order to demonstrate the linearity performance of the device, the third-order inter-modulation of a 18 mm MESFET was measured at two tone frequencies of 900.00MHz and 900.03MHz, respectively. Figure 10 shows the third-order power and the fundamental output power as a function of input power. The bias condition was a drain bias of 3.3V and a gate bias of -1.95V, corresponding to 12% $I_{\max}$ (*class AB* condition). A third-order intercept point, IP_3, was determined to be 49.5 dBm. A linearity figure-of-merit (LFOM : IP_3/P_{DC}) was 45, which is comparable with the state-of-the art LFOM of a HBT (LFOM of 44) [15] and a spike-doped

MESFET (LFOM of 50) [16].

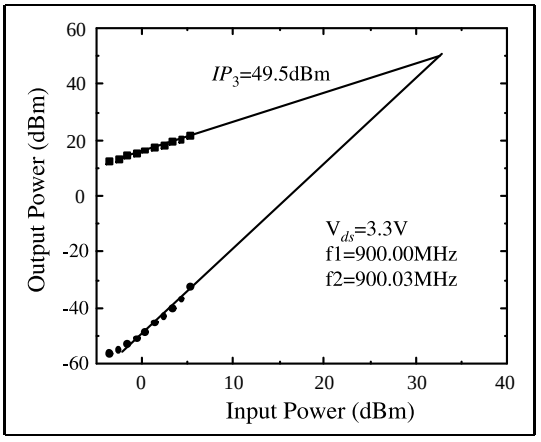

Fig. 10. Measured fundamental and third order product of 18 mm GaAs power MESFET.

The performance of power MESFET developed in this work is better than the previously recorded results in MESFET [7], namely output power of 31.6 dBm and 65% PAE at 3.5V and in heterojunction FET [6], output power of 31.4 dBm and 60% PAE at 3.0V. This paper reports the best power performance, ever achieved with GaAs power FETs at a drain bias in the range of 3.0∼3.5V. The most significant result is the simultaneous achievement of output power, PAE, power gain and third-order inter-modulation. These results are attributed to simultaneous achievement of low V_k and high BV_{gd} by using optimized channel structure for 900 MHz power MESFET. The high transconductance at *class AB* condition (10% $I_{\max}$ at $V_{gs} = -1.9$V), as shown in Fig. 6, can deliver high linear gain. The linear gain of 16.5 dB in this work is much higher than the reported results for MESFET [7] and that for HFET [6], which are 12 dB and 12.7 dB, respectively. It is believed that the power MESFET developed in this work is quite suitable for the digital cellular phone application because the high gain can deliver a high PAE in the linear operation region of output power and the IP_3 is high enough to obtain a low third-order inter-modulation.

IV. CONCLUSIONS

A state-of-the-art GaAs power MESFET operating at a voltage as low as 3.3V has been developed using the low-high doped structure grown by molecular beam epitaxy. The 0.8 μm gate length GaAs power MESFET with a total gate width of 18 mm is shown to have a maximum drain current of 5.0 A, transconductance of 1.7 S, and a gate-to-drain breakdown voltage of 28 V. The MESFET tested at 3.3 V drain bias and a 900 MHz operation frequency shows output power of 32.5 dBm and PAE of 68%. The low-high doped structure designed in the present work demonstrates that high PAE could be obtained even at a low drain bias of 3.0V. At 3.0V drain bias, an output power of 31.4 dBm with a PAE of 68% was recorded. This is the best power performance that has been ever achieved with power FETs at drain biases of 3.0∼3.5V. Two-tone testing measured at 900.00MHz and 900.03MHz shows that a third-order intercept point is 49.5 dBm. This excellent performance was attributed to the achievement of a device struc-

ture with optimum material parameters and minimum parasitics. The power MESFET developed in this work is expected to be useful as a power amplifying device for digital hand-held phone because the high linear gain can deliver a high power added efficiency in the linear operation region of output power and the high third-order intercept point can reduce third-order inter-modulation.

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