Performance Evaluation of a Cell Reassembly Mechanism with Individual Buffering in an ATM Switching System

Gwangman Park, Sungyeol Kang and Chimoon Han

CONTENTS

ABSTRACT

We present a performance evaluation model of cell reassembly mechanism in an ATM switching system. An ATM switching system may be designed so that communications between processors of its control part can be performed via its switching network rather than a separate inter-processor communications network. In such a system, there should be interface to convert inter-processor communication traffic from message format to cell format and vice versa, that is, mechanisms to perform the segmentation and reassembly sublayer. In this paper, we employ a continuous-time Markov chain for the performance evaluation model of cell reassembly mechanism with individual buffering, judicially defining the states of the mechanism. Performance measures such as message loss probability and average reassembly delay are obtained in closed forms. Some numerical illustrations are given for the performance analysis and dimensioning of the cell reassembly mechanism.

I. INTRODUCTION

In the past few years, broadband integrated services digital network (B-ISDN) has received increasing attention as a communication architecture capable of supporting multimedia applications. The key to a successful B-ISDN is the ability to support a wide variety of traffic with diverse service requirements. B-ISDN should also be able to cope with expected (as well as unexpected) future services in a practical and easily expandable fashion.

Several techniques have been proposed as the switching and multiplexing schemes for B-ISDN. Among them, asynchronous transfer mode (ATM) is expected to be the most promising transfer technology because of its efficiency and flexibility. ITU-T also is actively working on standardizing ATM-based B-ISDN.

By segmenting information from sources into fixed-size cells and multiplexing these cells on a shared medium, ATM can readily integrate diverse traffic types from multiple sources. Thus, the traffic transferred across the ATM network is a stream of cells. But, there must exist some network elements performing a reassembly of the information from multiple constituent cells before forwarding the information to the upper layers.

Quite a few ATM switch architectures have been suggested and many experimental ATM switches are being developed. An ATM switching system is usually composed of many switching modules and each module may be controlled by its own processor. In such an ATM switching system, inter-processor communications (IPCs) are necessary in order to perform switching control functions properly. Furthermore, an ATM switching system can be designed so that its switching network can be used for IPCs without a separate IPC network. In the switching system, there should be interfaces to convert IPC traffic from message format to cell format and vice versa, that is, mechanisms to perform the segmentation and reassembly (SAR) sublayer functions. In this paper, we concern the reassembly block among them, so called, *cell reassembly function block*.

Many studies in packet communications have dealt with packetization buffers and their results may be applied to the design of mechanism that performs the segmentation of messages in ATM environment [1], [2]. But, the literatures contain little analysis of reassembly buffers. Moors *et al*. [3] identify a number of critical issues that are particular to the implementation of receivers for ATM-based networks, and propose alternatives for dealing with these issues. Smith *et al*. [4] concern the virtual channel queue for the broadband terminal adaptor, to convert data packets into ATM cells and vice versa. They derive an upper bound for the fraction of packets sacrificed by comparing the sample paths of the completed work processes for finite and infinite buffers. Heijenk *et al*. [5] model and analyze the SAR processes. They obtain the first two moments of the interdeparture time distribution, given the first two moments of the interarrival time distribution by extending the analysis of the class of queueing networks considered in Queueing Network Analyzer (QNA), a software package developed at AT&T Bell Labs by Whitt et al. But, these papers mentioned in the above [3]-[5] have analyzed reassembly buffers whose buffer management schemes are different from that of this paper.

In this paper, we consider a method to implement this block and develop its performance evaluation model. We begin in Section II with the description of a method to implement cell reassembly function block and associated terminologies. Performance analysis is given through analytical modeling under certain limited assumptions and performance measures such as message loss probability and average reassembly delay are obtained in closed forms in Section III. Comparisons of the results obtained by simulation and analytical approach are given for the validation of analytical modeling in Section IV. Some numerical illustrations are given for the performance analysis and dimensioning of the reassembly block. Finally, we conclude in Section V.

II. A METHOD FOR IMPLEMENTING CELL REASSEMBLY FUNCTION BLOCK

Cell reassembly function block assembles cells transmitted by ATM switching network into messages. If a message to be transferred using ATM fits within one cell payload, then it can be transmitted as a single segment message. Otherwise, the message must be segmented by the source and transferred in multiple cells. Cells for the message can be classified into Begin Of Message (BOM), Continuation Of Message (COM), and End Of Message (EOM) cells. They represent the first cell, the continuation cell and the last cell of the message respectively. These cells are multiplexed with those from other messages, possibly from other sources. In ATM, the occurrence of cells containing information from a specific source is not necessarily periodic. Hence, cells from different messages may be arbitrarily interleaved as shown in Fig. 1, where subscript numbers represent message identifiers.

The cells of a message arrive at the block and wait to be ready for reassembly in buffer until the EOM cell of the message arrives. For convenience, we call a message whose BOM cell has arrived but EOM cell has not yet an *unready* message. Once the EOM cell of an unready message arrives, its constituent cells are assembled in its turn into original message format. After completing the reassembly of the message, the buffer space assigned for its constituent cells can be reassigned for other message.

We now consider a scheme for constructing this block performing the function described in the above, called *individual buffering mechanism*. This scheme assigns buffer space reserved individually for each message. The size of buffer space separated for a mes-

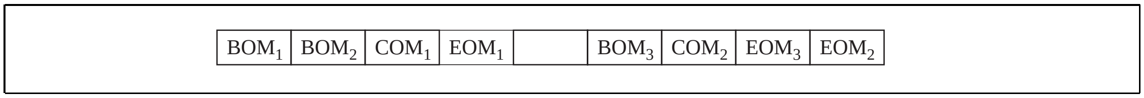

Fig. 1. Possible cell interleaving.

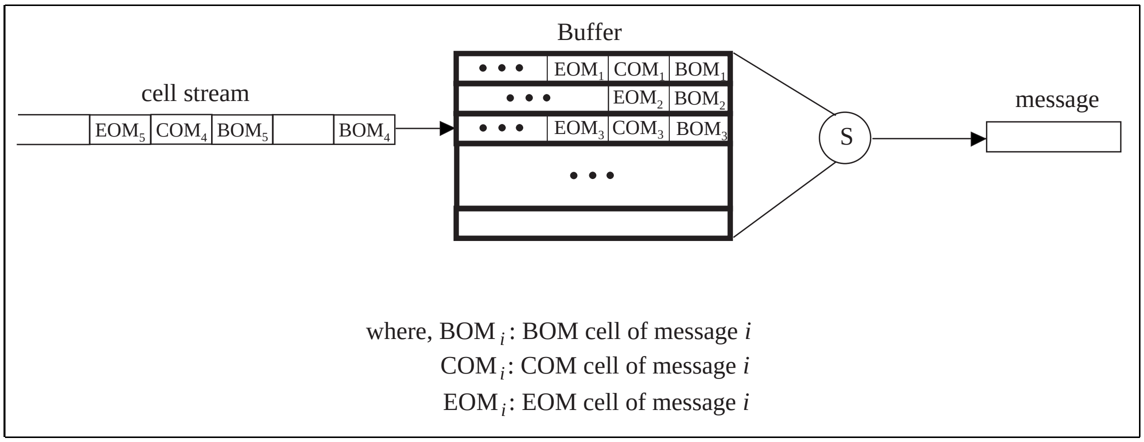

Fig. 2. Operation of individual buffering mechanism.

sage is designed considering the maximum length of messages and fixed in this mechanism. This buffering mechanism is very simple in implementation and buffer management.

Figure 2 shows the functioning of individual buffering mechanism for cell reassembly function block. The boldfaced rectangular is the buffer storing one message. If a message occupies a part of an individual buffer space, its remaining space cannot be used for storing other messages. So, there is a possibility that buffer utilization is very low if the maximum size of messages is large but the great part of messages is small in comparison with the maximum. It is probable that the entire buffer is occupied with many small-size messages, resulting in large unused remaining space in buffer. However, we expect that the variation in IPC message size may be limited within a certain bound so that the utilization problem can be alleviated.

III. PERFORMANCE MODELING OF CELL REASSEMBLY FUNCTION BLOCK

As previously mentioned, individual buffering mechanism assigns dedicated buffer space for each message. When BOM cell of a message arrives at cell reassembly block, it occupies dedicated buffer space reserved individually for each message irrespective of actual message size. Once the EOM cell of the message arrives, its constituent cells may be assembled into original message format and then the buffer space can be reassigned for other message. Thus important events which change system state of this buffering mechanism are as follows.

- arrival of BOM cells
- arrival of EOM cells
- reassembly completion of a message

In this paper, we assume the arrival process of cells as follows. The arrival process of BOM cells is Poisson process with rate λ. Interarrival time distribution between BOM cell and EOM cell of each message is exponential with mean $1/\beta$ and the distribution of reassembly time is assumed to be exponential with mean $1/\mu$. Practically, message length in cells is variable according to the class and content of message. Hence, interarrival time between BOM cell and EOM cell and reassembly time of each message are influenced by its length. However, there exist some difficulties in analytic modeling incorporating the dependency of these times on the message length. Here, we assume that interarrival time between BOM cell and EOM cell and reassembly time of a message are exponentially distributed. Validation to these assumptions is given at the next section. We also assume that the capacity of buffer storing messages is K.

Before getting further to the performance model of the block, let's consider obtaining the estimates of β and μ a little bit. The length of a message must be considered in estimating β and μ since it seriously affects them. Let α_n be the probability that a message is composed of n cells and $\bar{x}_n$ be the mean of the interarrival time between the BOM cell and EOM cell of a message with the length of n cells. In that case, we can estimate β as

$$\beta = \frac{1}{\sum_n \alpha_n \bar{x}_n}.$$

The time required to reassemble a message with length of n cells may increase linearly as n does, that is, nd, where d represents the processing time per cell for reassembly of the message. So, μ is estimated by

$$\mu = \frac{1}{\sum_n \alpha_n nd}.$$

We are interested in message loss probability, mean number of messages queued in buffer and average delay of a message in buffer as the performance measures for the cell reassembly function block. Among them, message loss probability requirement is most critical in the design of the block. The message loss probability is defined as the number of lost messages over the total number of messages arriving at this function block. We assume that message loss only occurs when BOM cell of a message finds that buffer space reserved individually for each message is fully occupied. And a message seizes buffer space from arrival of BOM cell to reassembly completion of the message.

In this paper, we develop its performance evaluation model employing a continuous-time Markov chain (CTMC). We define the states of this CTMC model by (i, j), where i represents the number of messages in buffer whose BOM cell has arrived and j represents the number of messages in buffer whose EOM cell has arrived, $0 \le j \le i \le K$.

So, in state (i, j), i out of K units of buffer are occupied with (either unready or ready) messages and j out of those i messages are ready for reassembly with their all constituent cells or under reassembly.

The state transition diagram of the CTMC is shown in Fig. 3. Let's denote by $p_{(i,j)}$ the steady-state probability that the reassembly block will be in state (i, j). Then, the balance equations of this system are given by

$$\begin{aligned}
&[\lambda + (i-j)\beta + \mu] p_{(i,j)} \\
&\quad = \lambda p_{(i-1,j)} + (i-j+1)\beta p_{(i,j-1)} \\
&\quad + \mu p_{(i+1,j+1)}, \ 0 < j < i < K \\
&\left[\lambda + (i-j)\beta\right] p_{(i,0)} = \lambda p_{(i-1,0)} + \mu p_{(i+1,1)}, \\
&\qquad 0 < i < K, \ j = 0 \\
&(\lambda + \mu) p_{(i,i)} = \beta p_{(i,i-1)} + \mu p_{(i+1,i+1)}, \\
&\qquad 0 < i = j < K \\
&\left[(K-j)\beta + \mu\right] p_{(K,j)} = \lambda p_{(K-1,j)} \\
&\qquad + (K-j+1)\beta p_{(K,j-1)}, \\
&\qquad i = K, \ 0 < j < K \\
&\lambda p_{(0,0)} = \mu p_{(1,1)}, \ i = j = 0 \\
&K\beta p_{(K,0)} = \lambda p_{(K-1,0)}, \ i = K, \ j = 0 \\
&\mu p_{(K,K)} = \beta p_{(K,K-1)}, \ i = j = K \qquad (1)
\end{aligned}$$

Manipulating these balance equations, we can get a nice result on the steady-state probabilities $p_{(i,j)}$ as follows.

Theorem 1. *For any* (i, j), $0 \le j \le i \le K$,

$$p_{(i,j)} = \frac{\lambda^i}{(i-j)!\beta^{i-j}\mu^j} p_{(0,0)}$$

and

$$p_{(0,0)} = \left[\sum_{i=0}^{K} \sum_{j=0}^{i} \frac{\lambda^i}{(i-j)!\beta^{i-j}\mu^j} \right]^{-1}. \qquad (2)$$

Using "Poisson arrival sees time average" (PASTA) property, we now can obtain message loss probability P_{loss}. That is,

$$\begin{aligned}
P_{loss} &= \sum_{j=0}^{K} p_{(K,j)} \\
&= \frac{\displaystyle\sum_{j=0}^{K} \frac{\lambda^K}{(K-j)!\beta^{K-j}\mu^j}}{\displaystyle\sum_{i=0}^{K} \sum_{j=0}^{i} \frac{\lambda^i}{(i-j)!\beta^{i-j}\mu^j}}. \qquad (3)
\end{aligned}$$

And, we can obtain the mean number of messages queued in buffer, L, as follows.

$$\begin{aligned}
L &= \sum_{i=0}^{K} i \sum_{j=0}^{i} p_{(i,j)} \\
&= \frac{\displaystyle\sum_{i=0}^{K} i \sum_{j=0}^{i} \frac{\lambda^i}{(i-j)!\beta^{i-j}\mu^j}}{\displaystyle\sum_{i=0}^{K} \sum_{j=0}^{i} \frac{\lambda^i}{(i-j)!\beta^{i-j}\mu^j}}. \qquad (4)
\end{aligned}$$

Average delay of messages in buffer (mean sojourn time of a message from its arrival through reassembly completion), W, can be obtained, using Little's law and effective arrival theorem, by

$$L = \lambda_e W, \qquad (5)$$

where λ_e represents the effective arrival rate of messages at the buffer and is calculated by

$$\lambda_e = \lambda(1 - P_{loss}). \qquad (6)$$

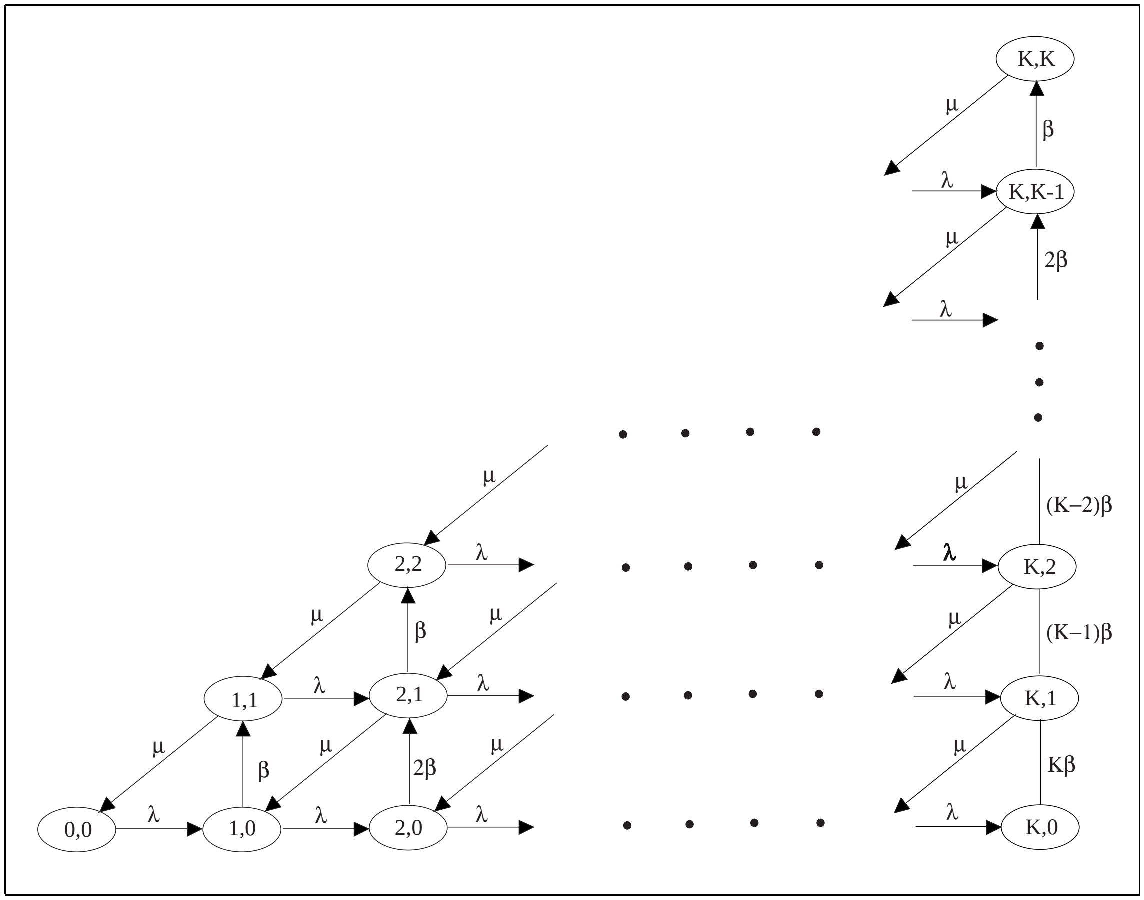

Fig. 3. State transition rate diagram.

Thus, W can be evaluated by

$$W = \frac{L}{\lambda(1 - P_{loss})}. \tag{7}$$

IV. NUMERICAL ANALYSIS

We now compare the results obtained from analytic model with those from simulation. In analytic modeling, we have assumed that both interarrival time distribution between BOM and EOM and reassembly time distribution of each message are exponentially distributed. But, as previously mentioned, they are influenced by the length of each message. Thus, we have reflected them in the simulation model as follows. We assume that the size of messages (in cells) ranges from 1 to M. Practically, there must exist upper bound of maximum message size which is dependent upon implementation schemes. Interarrival time distribution between BOM cell and EOM cell of a message with k cells is assumed to be k-Erlangian distribution. We also assume that reassembly time of a message is proportional to its size (in cells) and that of one cell is constant. The distribution of message size is expected to affect the performance measures. In this simulation model, two different distributions, truncated geometric and discrete uniform, are considered. The probability mass function of truncated geometric distribution is given by

$$Pr\{\text{message size is } i \text{ cells}\} = \frac{p(1-p)^{i-1}}{1-(1-p)^M},$$

where p represents the parameter of truncated geometric distribution.

The simulation model has been implemented in a simulation language, ARENA. In simulation, we have carried out ten replications at each specific condition. The run length of each replication is based on the message loss probability obtained from analysis. One value of performance measures, that is, P_{loss}, L and W, is sampled by generating messages about one hundred times as the reciprocal of message loss probability. For example, if message loss probability is 10^{-3}, the number of generated messages is about 10^5.

Comparisons of the results obtained from analytical approach and those from simulation are shown in Tables 1~6. Without loss of generality, we assume that μ is 1. In these tables, minimum and maximum values of each performance measure obtained by simulation are shown. From these tables, we can see that the results from analytic approach are well consistent with those of simulation.

Here, some numerical illustrations are also presented for demonstrating changes of performance measures as traffic load of this block changes. The changes of performance measures such as message loss probability, average number of messages queued in buffer and average delay time of messages are shown in Figs. 4~6. In these figures, we can see the in-

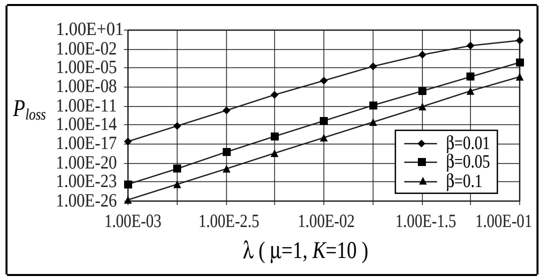

Fig. 4. Message loss probability as a function of input traffic.

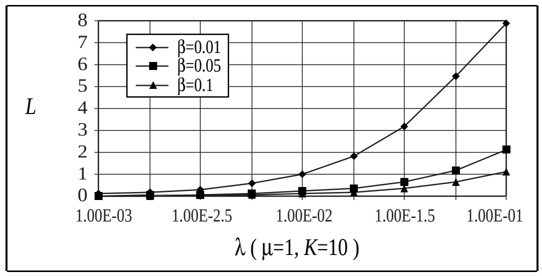

Fig. 5. Mean number of messages as a function of input traffic.

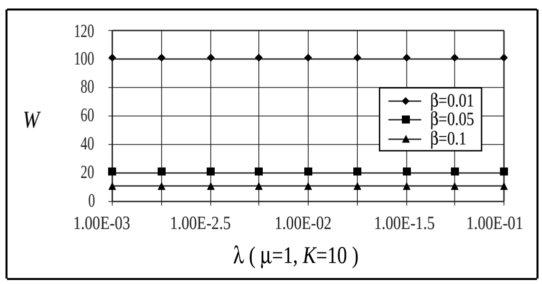

Fig. 6. Average delay time of message as a function of input traffic.

Table 1. Comparison of message loss probability between simulation and analytic results ($\beta = 0.01,\ \mu = 1.0,\ M = 10$).

λ	Analytic Result	Simulation (truncated geometric, $p = 0.2$)		Simulation (discrete uniform)	
		min.	max.	min.	max.
0.05	1.94E-2	1.57E-2	2.08E-2	1.60E-2	2.16E-2
0.06	4.51E-2	3.87E-2	5.01E-2	3.77E-2	4.67E-2
0.07	8.18E-2	7.19E-2	9.30E-2	7.34E-2	8.50E-2
0.08	1.26E-1	1.19E-1	1.36E-1	1.07E-1	1.34E-1
0.09	1.73E-1	1.60E-1	1.79E-1	1.64E-1	1.79E-1
0.10	2.20E-1	2.04E-1	2.22E-1	2.12E-1	2.25E-1

Table 2. Comparison of mean number of messages queued in buffer between simulation and analytic results ($\beta = 0.01,\ \mu = 1.0,\ M = 10$).

λ	Analytic result	Simulation (truncated geometric, $p = 0.2$)		Simulation (discrete uniform)	
		min.	max.	min.	max.
0.05	4.95	4.81	4.96	4.90	4.98
0.06	5.79	5.65	5.86	5.68	5.80
0.07	6.50	6.39	6.57	6.39	6.53
0.08	7.07	6.92	7.14	6.97	7.11
0.09	7.53	7.38	7.60	7.42	7.62
0.10	7.89	7.77	7.90	7.81	7.93

Table 3. Comparison of average delay of a message in buffer between simulation and analytic results ($\beta = 0.01,\ \mu = 1.0,\ M = 10$).

λ	Analytic Result	Simulation (truncated geometric, $p = 0.2$)		Simulation (discrete uniform)	
		min.	max.	min.	max.
0.05	101.05	99.38	101.95	100.11	101.39
0.06	101.06	99.50	102.20	99.68	101.36
0.07	101.06	99.70	102.04	99.99	101.44
0.08	101.07	99.43	102.72	100.06	101.49
0.09	101.07	99.60	101.82	99.98	102.26
0.10	101.08	99.22	102.43	99.608	102.08

Table 4. Comparison of message loss probability between simulation and analytic results ($\beta = 0.02,\ \mu = 1.0,\ M = 20$).

λ	Analytic Result	Simulation (truncated geometric, $p = 0.3$)		Simulation (discrete uniform)	
		min.	max.	min.	max.
0.05	2.55E-4	1.40E-4	2.50E-4	2.20E-4	3.35E-4
0.06	9.47E-4	6.55E-4	8.50E-4	8.70E-4	1.08E-3
0.07	2.66E-3	1.95E-3	2.45E-3	2.30E-3	3.12E-3
0.08	6.07E-3	4.92E-3	5.78E-3	5.18E-3	6.90E-3
0.09	1.19E-2	9.32E-3	1.08E-2	9.70E-3	1.39E-2
0.10	2.06E-2	1.63E-2	1.85E-2	1.56E-2	2.40E-2

Table 5. Comparison of mean number of messages queued in buffer between simulation and analytic results ($\beta=0.02,\ \mu=1.0,\ M=20$).

λ	Analytic Result	Simulation (truncated geometric, $p=0.3$)		Simulation (discrete uniform)	
		min.	max.	min.	max.
0.05	2.55	2.47	2.49	2.54	2.56
0.06	3.06	2.95	2.99	3.05	3.07
0.07	3.57	3.45	3.48	3.53	3.59
0.08	4.06	3.92	3.98	4.03	4.11
0.09	4.54	4.40	4.44	4.46	4.61
0.10	5.01	4.86	4.89	4.91	5.05

Table 6. Comparison of average delay of a message in buffer between simulation and analytic results ($\beta=0.02,\ \mu=1.0,\ M=20$).

λ	Analytic Result	Simulation (truncated geometric, $p=0.3$)		Simulation (discrete uniform)	
		min.	max.	min.	max.
0.05	51.05	49.44	49.79	50.96	51.12
0.06	51.06	49.36	49.86	50.96	51.13
0.07	51.07	49.44	49.77	50.88	51.24
0.08	51.09	49.37	49.85	50.91	51.26
0.09	51.10	49.42	49.82	50.03	51.50
0.10	51.11	49.38	49.87	50.16	51.45

crease of P_{loss} and L as traffic load does. But, Fig. 6 shows that W defined as the average sojourn time from its arrival through reassembly completion is almost constant although input traffic load increases. This is because the interarrival time between BOM cell and EOM cell is much longer than the reassembly time. Generally, L and W increase under certain bound since the capacity of buffer is limited, but P_{loss} increases rapidly.

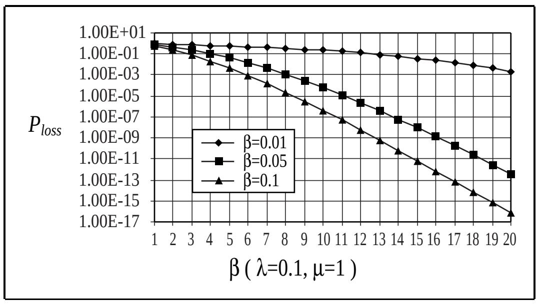

Fig. 7. Message loss probability as a function of buffer capacity.

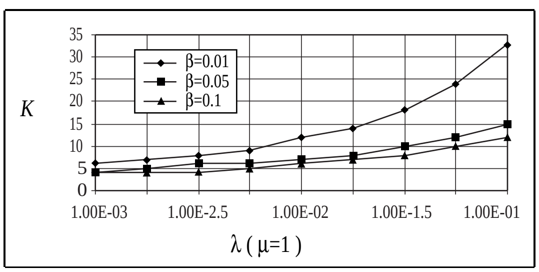

Fig. 8. Minimum buffer size required to maintain message loss probability under 10^{-8} as a function of input traffic.

Cell reassembly function block has to be designed to guarantee prescribed performance level, especially, message loss probability. Figure 7 shows the changes of message loss probability as buffer capacity increases. As shown in Fig. 7, the message loss probability reduces slightly as buffer capacity increases in case of $\lambda = 0.1$, $\beta = 0.01$ and $\mu = 1$. On the contrary, the message loss probability reduces remarkably even though buffer capacity increases slightly in case of $\lambda = 0.1$, $\beta = 0.1$ and $\mu = 1$. From this figure, we can observe that the obtainable message loss probabilities are very different depending on traffic parameters. Therefore, it is very important to correctly estimate the traffic parameters in the performance evaluation of this block. Figure 8 shows the minimum buffer size required to maintain P_{loss} under 10^{-8}. We can see there how the minimum buffer size required to maintain P_{loss} under prescribed value increases as traffic load does.

The major factors which have critical effects on the performance of the reassembly block are the processing capability of the block and the size of the buffer. In deciding those system parameters, we also need to consider other technological and economical aspects. Anyhow, it is necessary to consider the changes of its performance measures as illustrated here.

V. CONCLUSION

In this paper, we have established an analytical model for the performance analysis and dimensioning of a cell reassembly function block with individual buffering which performs SAR sublayer functions for IPC messages. This block performs interface to convert IPC traffic from cell format to message format. We have used a CTMC with judicially defined states for it and obtained the performance measures of this block such as message loss probability, mean number of messages queued in buffer and average delay time of message in buffer in closed forms. The cell reassembly mechanism of SAR sublayer functions is also necessary for signaling messages and user traffic. So, the results in this study may be useful for solving the teletraffic engineering issues of those function blocks as well as that of IPC traffic. Furthermore, these results may serve as helpful ingredients for the method of estimating the call processing capabilities of the control network part of such an ATM switching system considered here.

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Gwangman Park was born in 1969. He received the B.E. and M.E. degrees in industrial engineering from Seoul National University, Seoul, Korea, in 1991 and 1993, respectively. Since 1993 he has been with the Switching Technology Division of ETRI, Taejon, Korea. His current research interests are in architechture and performance evaluation of ATM networks.

Sungyeol Kang was born in 1957. He completed both of his undergraduate program and his master program in Seoul National University, majoring in industrial engineering and operations research, in 1981 and 1983, respectively. He received his Ph.D. degree in industrial and systems engineering from Georgia Institute of Technology, USA, in March 1992. He has worked for ETRI since March 1983. He participated in various projects, related to telecommunications network planning and the development of digital switching systems. He has recently been in charge of the performance engineering team for ATM switching systems under development there. His major research interests are in performance modeling of communication systems, teletraffic engineering, and switching technologies.

Chimoon Han was born in Taegu, Korea in 1951. He received the B.E. and M.E. degrees in electronics engineering from Kyung-pook National University in 1977 and Yonsei University in 1983 respectively. He received the Ph.D. degree in electronics engineering from the University of Tokyo, Japan in 1990. Since he joined Korea Institute of Science and Technology in 1977, he was involved in developing optical fiber communication and radio mobile communication systems until 1982. Since 1983, he has been involved in developing ISDN user-network interface system, LAN system, ATM switching system and wireless ISDN system in ETRI. He is currently the Director of Systems Technology Department in Switching Technology Division of ETRI. His research interests include the ATM switching system architecture and its performance evaluation, the traffic control and ATM based PCS.