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Design of a New ISFET Array Chip

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Abstract

A new ISFET array chip, based on detection of the threshold voltages of ISFETs by using an adjustable input, was designed. The chip includes 240 pH-ISFETs and circuitry such as comparators, a decoder and register. The chip has increased reliability, improved accuracy, digital output capability and the possibility of multisensor implementation. To fabricate the chip, an extended CMOS process was devised and implemented.

요 약

가변 입력전압을 이용하여 ISFET의 문턱전압을 검출하는 새로운개념의 ISFET array chip을 설계하였다. 설계된 칩은 240개의 pH-ISFET와 신호처리회로를 포함하며, 증가된 신뢰성 및 정확성, 디지탈 출력 그리고 멀티센서로의 응용성 등의 특성을 가진다. 칩제조를 위해 CMOS공정을 응용한 새로운 공정을 설계하였고 칩을 layout 하였다.

1. Introduction

Ion Sensitive Field-effect Transistors(ISFETs)[1-2], a sub set of the well known semiconductor chemical sensors, have several advantages such as small size, rapid response, low cost and the possibility for smart and multisensor implementation. They are impedance transformation devices in which the high impedance voltage signal at the input produces a low impedance output signal. Therefore, they do not require high input impedance amplifiers and high precision filters for noise reduction. In spite of these advantages, ISFETs do suffer some problems. One of them is that ISFETs can be destroyed by electrostatic discharge. This is because they are electronic active devices and their gate regions are not protected.

The development of microelectronic technology has made possible the development of extremely small semiconductor sensors to fabricate large sensor arrays in a small chip area. We believe that such a sensor array can produce advantages such as increased sensing reliability, improved accuracy, multisensing capability and spatial distribution measurement. To date, very few papers have appeared in the literature dealing with such sensor array research.[3-5] There has been no research on an ISFET array chip in the true sense of the word.

This paper describes the new concept[5], involving the detection of the threshold voltage of an ISFET by using an adjustable input, and the design of a pH-ISFET array chip based upon this concept. The chip is composed of 240 pH-ISFETs and measurement circuitry including a decoder, comparators and a register. The chip has numerous advantages such as digital output capability, increased reliability

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and accuracy. The simulation results of the designed circuitry are presented. For the chip fabrication, the process design by using the modified CMOS process and chip layout are also described.

2. Array Chip Features

The proposed ISFET array chip will have the following features;

a. Digital output

The ISFET output signal via the threshold detection circuit would be "0" or "1". Therefore, the chip can be connected to a computer or to a data aquisition card without the need of an analog to digital convertor.

b. Increased reliability

There are 240 ISFETs in the chip. These ISFETs can be checked individually for correct operation and hence the damaged or failed ISFETs can be automatically excluded from the measurement.

c. Improved accuracy

ISFETs can have a variation in characteristics such as threshold voltage, sensitivity and stability, even if they are fabricated in the same chip. The same situation also occurs in the circuitry. Statistical calculation of the output data of many ISFETs make it possible to overcome these charateristic variation problems. Improved accuracy can thus be achieved.

d. Low power consumption

In order to keep the total chip power consumption to a minimum, the decoder turns only 16 ISFETs in the same column on at once. Hence, overheating effects of the chip can be disregarded.

e. Possibility of multisensor implementation

The array chip includes 240 pH-ISFETs. But by forming different sensing membranes on designated pH-ISFET gates, the chip can be implemented as a multisensor for taste sensing for example.

3. Operational Concept of The Array Chip

In the saturation region, a drain current of a nMOSFET is approximated by

$$I_D = K\frac{W}{L}(V_G - V_T)^2 \quad (1)$$

Here, $K=C_o\mu$ is the gain factor, C_o is the gate capacitance of a MOSFET per unit area and μ is the mobility of the electrons in the channel. W is the channel width and L is the channel length.

A threshold voltage of a pH-ISFET is given by[6]

$$V_{TI} = \Phi_{RS} - \frac{Q_I}{C_I} - \frac{Q_D}{C_I} + 2\Phi_F + \Phi_{RL} - \Phi(pH) \quad (2)$$

$$= \Phi_C - \Phi(pH)$$

Here, Φ_{RS} is the work function difference between the reference electrode and a semiconductor, and C_I is the gate capacitance per unit area. Φ_{RL} is the potential difference between the reference electrode and the bulk solution. Φ(pH) represents the potential difference between the bulk solution and the sensing membrane surface, which is a function of pH in the solution. All parameters except for Φ(pH) are constants, and hence can be represented collectively as Φ_C.

In equation (1), the drain current is determined by (V_G-V_T). If we define this voltage as an effective gate voltage, the effective gate voltages of the ISFET and a MOSFET can be expressed respectively by

$$V_{EGI} = V_R - V_{TI} \quad (3)$$

$$V_{EGM} = V_G - V_T \quad (4)$$

where V_R is the applied voltage of the reference electrode. If we measure V_{EHI}, we can determine V_{TI} because V_R is a known value.

Figure 1 shows the structure of the chip and measurement system. The chip consists of a 4 to 16 decoder, the 16x15 pH-ISFET array, switches and comparators.

The input devices of the comparator are

composed of an ISFET and a MOSFET. The decoder systematically selects and switches on 16 ISFETs in the same column. At first, ISFETs, I(1,1)-I(16,1) are turned on and connection is made to comparator elements 1 - 16. The comparator compares the V_{EGI} which is a function of pH of the test solution with $V_{EGM}(=V_{th}-V_T)$, where V_{th}, the adjustable input threshold voltage is set at a specific value by the computer. If V_{EGI} is smaller than V_{EGM}, the output of the comparator will be "0" and if V_{EGI} is greater than or equal to V_{EGM}, the output will be "1". For example, if V_{th} is set at the value of pH 7, the output of the comparator will be "1" for a solution of pH below 7 and "0" for a solution of pH above 7, since V_{EGI} becomes larger as the pH in the solution decreases. Outputs of the comparators are sent to the data aquisition card via the register. After the interrogation of ISFETs in the first column, ISFETs in the next column, I2,1 to I2,16, are connected to comparator elements 1 - 16 and measurements again carried out. This process is completed when the ISFETs in the second to last column, I(1,15) - I(16,15), are measured. The last column is composed of MOSFETs instead of ISFETs for testing purposes.

If the measurement process mentioned above is carried out from V_{th}(pH 0) to V_{th}(pH 14) with a specific step, we can determine the pH of the solution by checking the V_{th} at/which the outputs of the ISFETs have switched. The resolution of the measurement depends on the step size of V_{th} which is controlled by the software. The more the steps, the higher the resolution. For higher resolutions, a larger measurement time is required. Therefore a compromise between measurement time and resolution needs to be considered according to the application. The same situation also applies in respect of the accuracy. If we increase the number of ISFETs which are to be interrogated and compared to one Vth step, then higher accuracy can be achieved. However, the measurement time will also be increased. Hence, a compromise should also be considered here.

Fig. 2 shows a distribution of the number of ISFETs when their outputs are switched. This distribution is caused by the variations in characteristics of the ISFETs, such as threshold voltage, sensitivity, stability and offsets in the circuitry. We are not sure exactly what type of distribution to expect, but it is clear that the shape

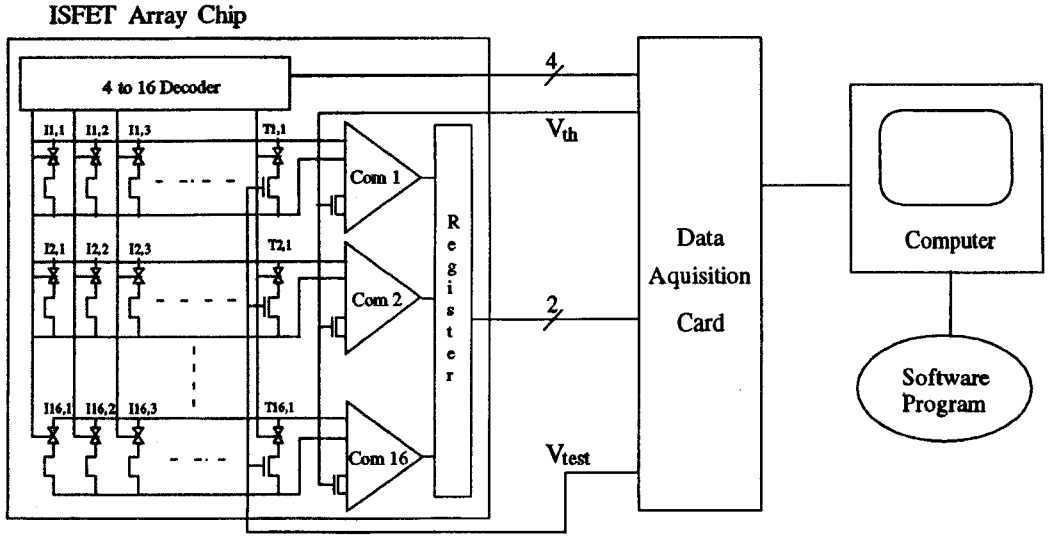

Fig. 1. The structure of the ISFET array chip and its measurement system.

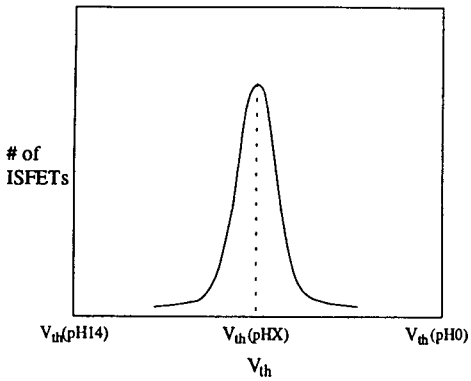

Fig. 2. A distribution of the number of ISFETs swiched in the pH X solution.

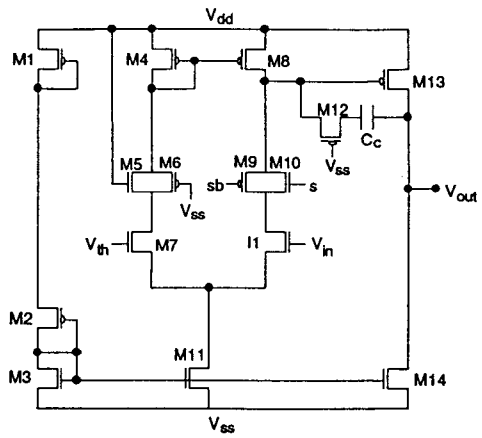

Fig. 3. Comparator circuit.

of the distribution would become sharper if the chip was fabricated more precisely. The pH of the solution will be determined at the peak value of the distribution. Even though there are 240 ISFETs on the chip, we can select the number of ISFETs which we want to employ. For example, just 16 or 32 ISFETs can be selected by the decoder in order to decrease the total measurement time.

Failed ISFETs can also be checked with the same technique. ISFETs that have been failed usually do not show any trend with the pH in the solution. During the measurement time, if there are any ISFETs which produce the same output, then they will be considered as failed and automatically excluded from the measurements.

4. Design and Simulation of The Circuitry

Fig. 3 shows a circuit of the comparator which is composed of a two stage CMOS operational amplifier and Table 1 shows the aspect ratios of the MOSFETs and capacitor used in the comparator. M9 and M10 are switches controlled by the decoder and M5 and M6 are used for matching purposes. The comparator should have a high open loop gain to give a clear and defined digital output. It should also have good phase and gain margins. The designed comparator showed high open loop gain

Table 1. Aspect ratios and capacitance of devices used in the comparator.

M1 2.4/2.4	M2 2.4/2.4	M3 2.4/2.4	M4 7.2/2.4
M5 4.8/2.4	M6 4.8/2.4	M7 17.1/4.8	M8 7.2/2.4
M9 4.8/2.4	M10 4.8/2.4	M11 4.8/2.4	M12 2.4/4.8
M13 13.2/2.4	M14 4.8/2.4	I1 48/4.8	Cc 1pF

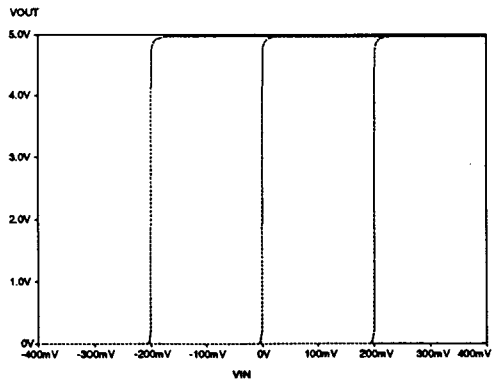

Fig. 4. Simulated outputs when V_{th} = -0.2V, 0V and 0.2V.

of 71 dB and large phase margin of 68 degrees. The power consumption was very small, being 0.12mW. Fig. 4 shows the simulation result of the designed comparator, which shows the digital outputs at V_{th}

of -0.2V, 0V and 0.2V.

The positive input of the comparator is an ISFET while the negative input is a MOSFET. The gate insulator of the ISFET will be composed of 300 Å thick SiO_2 and 500Å thick Si_3N_4, while the MOSFET will be composed of 200Å thick SiO_2. For matching of the two input transistors, the following equation must be established.

$$K_{MOSFET}(W/L)_{MOSFET} = K_{ISFET}(W/L)_{ISFET} \quad (5)$$

If we suppose that the dielectric constants of SiO_2 and Si_3N_4 are 3.9 and 7.5 respectively, the gate capacitance can be expressed as

$$C_g(MOSFET) = 1.73 \times 10^{-7}[F/cm^2]$$

$$C_g(ISFET) = 6.16 \times 10^{-8}[F/cm^2]$$

Hence, on the basis of equation (5), the aspect ratios of the input ISFET and MOSFET were decided as 48μm/4.8μm and 17.1μm/4.8μm respectively. Some deviation of the dielectric constant and thickness of the insulators could occur during the fabrication process. The result of such deviation could increase the offset voltage of the comparator. However, in our chip, the offset voltage is not important because it can be nullified during the calibration process.

Both the 4 x 16 decoder and the parallel-in serial-out register use standard structures[7].

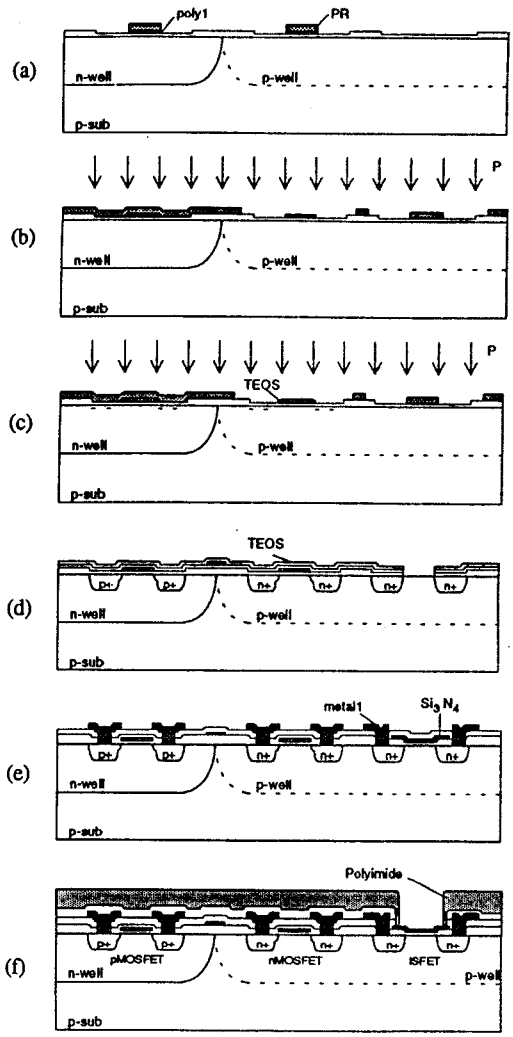

Fig. 5. A cross-section of the fabrication process.

5. Fabrication process design and layout

An ISFET does not have a polysilicon gate conductor and also has its own specific sensing membrane such as Si_3N_4 layer. Therefore, it is not possible for an ISFET and a MOSFET to be fabricated together according to the standard CMOS process[8]. Hence. we have designed a modified standard process which allow the integration of ISFETs and circuit. In the modified process, we tried to follow the standard process as much as possible to reduce pre and post processing. The chip will be fabricated by using the modified 1.2μm double poly, single metal, twin well CMOS process. Fig. 5 shows the cross-section of the fabrication process.

(a)(100) p-type silicon wafers of 5 inch diameter size will be used as starting material. The fabrication process will be carried out using the standard process up to the step where the polysilicon will be etched. All the polysilicon will be removed except for the MOSFET gate, capacitor and interconnection regions.

(b)Phosphrous atoms will be implanted to form n- regions for LDD (lightly doped drain) structure. At

this stage, the gate region of the ISFET will be protected by photoresist while that of the MOSFET will be protected by polysilicon.

(c)After Boron implantation to form p- region, Phosphrous implantation will be followed to form n+ region. At this stage, the gate region of the ISFET will also be protected by photoresist.

(d)Boron will be implanted to form p+ region. Oxide deposition for forming capacitor dielectric material, drive-in of implanted layer and polysilicon 2 formation will be followed. After another oxide deposition to protect polysilicon 2, the oxide in the ISFET gate region will be etched.

(e)The 300Å thick thermal SiO_2 and 500Å thick LPCVD Si_3N_4 will then be grown and patterned. Oxide deposition for protection of the Si_3N_4 sensing membrane and metallisation processes will be followed.

(f)Finally, the oxide of ISFET gate region will be etched and a polyimide passivation layer will be formed.

A set of 13 masks are needed for the complete process.

Fig.6 shows the layout of the chip. The whole chip size is 4mm x 4mm. For encapsulation purposes, there are no active devices for 60μm around an ISFET gate. There are 15 pads including 2 extra pads in the chip, 4 for the decoder, 4 for V_{dd} and V_{ss} in the digital and analog circuit, 2 for register control, 1 for the output, 1 for V_{th} and 1 for test voltage.

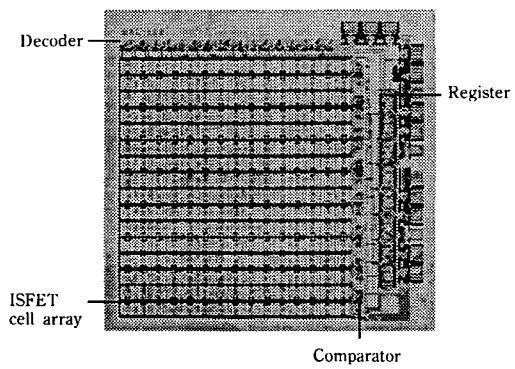

Fig. 6. Layout of the array chip.

6. Summary

A new ISFET array chip, which is based on the detection of threshold voltage of an ISFET by using an adjustable input, has been designed. The chip includes 240 pH-ISFETs and circuitry including comparators, a decoder and a register. The chip provides increased reliability and improved accuracy due to statistical treatment of the output data. It has other important advantages such as digital output capability, low power consumption and the possibility of multisensor implementation. For the fabrication, a chip layout and a modified CMOS process design allowing the integration of sensors and circuits, were used. We believe that the designed chip is the first ISFET array of its kind in the true sense. Futher research on the fabrication, evaluation and application of the chip will be continued.

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