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BiCMOS 선형 OTA

(A BiCMOS Linear Operational Transconductance Amplifier)

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要約

BiCMOS 선형 OTA를 설계했다. 설계된 OTA는 CMOS 트랜스컨덕터, 바이폴라 트랜스리니어 전류 이득셀, 그리고 세개의 CMOS 전류 미러로 구성된다.

설계된 회로의 선형성은 바이폴라 OTA에 필적한다. 그러나, 그것의 직류 특성은 바이폴라 OTA보다 우수하다. 47.3㎲의 트랜스컨덕턴스를 갖는 측정 회로를 시뮬레이션한 결과, -1.0 ~ 1.0V 사이의 입력 전압 범위에서 ±1%의 작은 선형 오차와 3.6nA보다 작은 출력 오프셋 전류가 얻어진다는 것을 알았다.

Abstract

Abstract—A linear BiCMOS operational transconductance amplifier(OTA) is described. It consists of a CMOS linear transconductor and a bipolar translinear current gain cell followed by three CMOS current mirrors. The proposed circuit has comparable linearity and temperature stability but superior dc characteristics to its bipolar counterpart. A test circuit with a transconductance of 47.3㎲ has been simulated. Simulation results show that a linearity error of less than ±1 percent over an input voltage range from -1.0 to 1.0 V and a output dc offset current as small as -3.6 nA can be obtained.

I. Introduction

Operational transconductance amplifiers (OTA's) are essential elements in the design of electrically tunable amplifiers, filters, oscillators, and current-mode signal processing systems. There are two important limitations with the commercial OTA's, like the LM3080 and CA3080: one is their severe harmonic distortion for larger input signals caused by the nonlinear characteristic of the emitter-coupled differential input pair, the other is their temperature dependency caused by the temperature-sensitive transistor parameters.[1-3] The simplest way of solving these problems is the use of the improved

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OTA's with on-chip diode linearization, like the LM13600 and CA3280.[14] In order to achieve the improved performance with these devices, however, exactly matched resistors or elaborate trimming of a potentiometer is required. Recently, the other solution which does not suffer from such requirements has been reported.[15] However, both circuits, being implemented with bipolar technology, exhibit a low input resistance and a large input bias current. In addition, it is difficult to adjust device parameters for maintaining a output dc offset current to within a desired low level. These factors result in limiting the usefulness of the circuits in dc applications.

In this paper, a BiCMOS linear OTA based on the bipolar linear OTA scheme[15] is presented. It features superior dc performance. The basic principle of the circuit is described in Section Ⅱ. Its deviation from linearity under nonideal conditions is discussed in Section Ⅲ. Simulation results are presented in Section Ⅳ.

Ⅱ. Circuit Description and Operation

Fig. 1 shows the complete circuit diagram of the BiCMOS linear OTA. It consists of a linear transconductor formed by transistors M_1 - M_{12}, a translinear current gain cell Q_{13} - Q_{16}, and three cascode current mirrors M_{17} - M_{28}. The transconductor converts the differential input voltage v_{IN} to its corresponding differential output currents i_{D1} and i_{D2}. Its operation can be explained as follows: For simplicity, we assume that all transistors are identical. Since the gate-source potentials of M_{1B} and M_{2B} are equal to those of M_{1A} and M_{2A}, respectively, we can write $i_{D1B} = i_{D1A} = i_{D1}$ and $i_{D2B} = i_{D2A} = i_{D2}$. The drain current i_{D2A} is reproduced at the source of M_3 through two current mirrors, formed by M_5, M_6, and M_9, M_{10}, respectively, to bias M_3. In the same manner, M_4 is biased by the drain current i_{D1A} which is reproduced at the source of M_4 through two current mirrors: One is formed by M_7 and M_8 and the other by M_{11} and M_{12}.

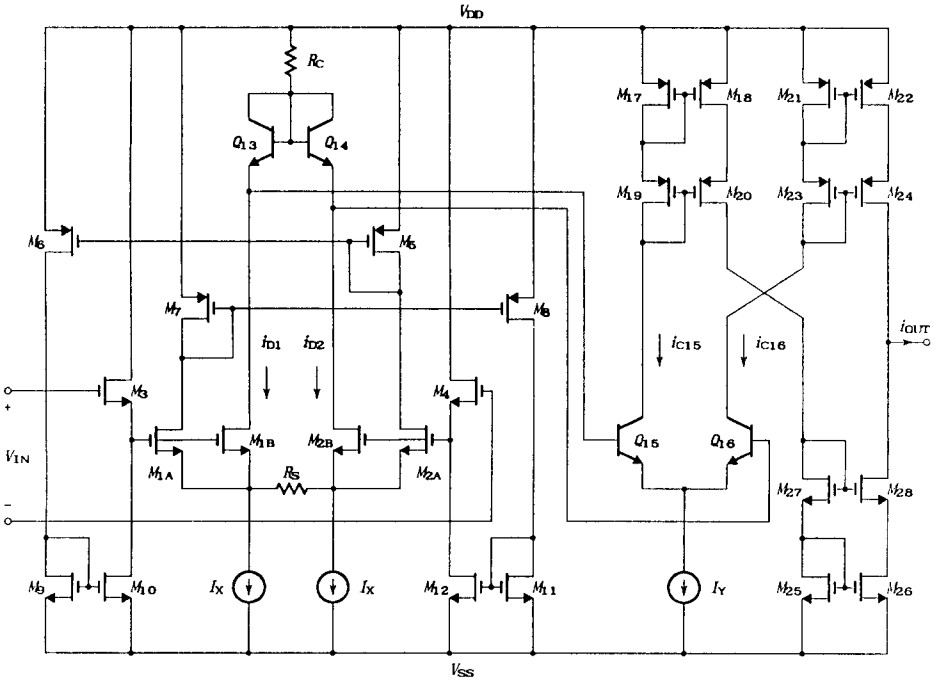

Fig. 1. The circuit diagram of the BiCMOS linear OTA.

Summing the voltages around the loop consisting of the input voltage source, the four transistors M_1- M_2, and the source degeneration resistor R_S, we obtain

$$v_{IN}=\left(\sqrt{\frac{i_{D2}}{K}}+V_t\right)+\left(\sqrt{\frac{i_{D1}}{K}}+V_t\right)+R_s(i_{D1}-i_{D2}) -\left(\sqrt{\frac{i_{D2}}{K}}+V_t\right)-\left(\sqrt{\frac{i_{D1}}{K}}+V_t\right) \quad (1)$$

where

V_t = threshold voltage

$K=\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)$

μ_n = electron mobility

C_{ox} = channel capacitance per unit aarea

W = channel width

L = channel length

which gives

$$i_{D1}-i_{D2}=\frac{v_{IN}}{R_s} \quad (2)$$

Since the sum of i_{D1} and i_{D2} is I_X, i_{D1} and i_{D2} will be given by

$$i_{D1}=\frac{I_x}{2}+\frac{v_{IN}}{2R_s} \quad (3a)$$

$$i_{D2}=\frac{I_x}{2}-\frac{v_{IN}}{2R_s} \quad (3b)$$

The differential output currents $i_{D1}$and i_{D2} of the transconductor drive the diode-connected bipolar transistor pair Q_{13} and Q_{14} of the translinear current gain cell. The current gain cell makes the current partitioning of the transistor pair Q_{13} and Q_{14} to be the mirror image of the current partitioning of the transistor pair $Q_{15}$and Q_{16}. Assuming that the four transistors are matched and their common-emmiter current gains are sufficiently large, one can write the following relation:

$$\frac{i_{D1}}{i_{D2}}=\frac{i_{C16}}{i_{C15}} \quad (4)$$

The output currents i_{C15} and i_{C16} of the current gain cell are differenced by three current mirrors formed by M_{17} - M_{20}, M_{21} - M_{24}, and M_{25} - M_{28}, respectively. Since the sum of i_{C15} and i_{C16} is I_Y and the difference is i_{OUT}, which denotes the single-ended output current of the OTA, currents i_{C15} and i_{C16} can be written as follows:

$$i_{C15}=\frac{I_Y}{2}-\frac{i_{OUT}}{2} \quad (5a)$$

$$i_{C16}=\frac{I_Y}{2}-\frac{i_{OUT}}{2} \quad (5b)$$

Combining (3a), (3b) and (5a), (5b) into (4), one can obtain

$$\frac{\frac{I_X}{2}+\frac{v_{IN}}{2R_s}}{\frac{I_x}{2}-\frac{v_{IN}}{2R_s}}=\frac{\frac{I_Y}{2}+\frac{i_{OUT}}{2}}{\frac{I_Y}{2}-\frac{i_{OUT}}{2}} \quad (6)$$

which gives the transfer function of the OTA expressed as follows:

$$i_{OUT}=\frac{I_Y}{I_X}\frac{1}{R_s}v_{IN} \quad (7)$$

The transconductance G_m is given by $(I_Y / I_X)(1/ R_S)$. It should be noted that in deriving (7) no numerical approximations have been made, and there are no temperature-dependent terms. Also, note that the transconductance of the OTA is determined by the ratio of the dc bias currents I_Y and I_x

Ⅲ. Second-Order Effects

The discussion up to now has been based on the ideal transistor models. However, in reality, nonidealities such as finite β effect for bipolar transistors and body effect and channel-length modulation effect for MOS transistors are present. These nonidealities represent the sources of linearity errors and temperature coefficients of the OTA. These second-order effects are considered in this section

1. Finite β Effect

The subcircuit which contributes to this

effect is the current gain cell. In the presence of finite β , the transfer function of the OTA is modified so that

$$i_{OUT} \cong \frac{I_Y}{I_X}\frac{1}{R_s}\left(1-\frac{2}{\beta_N}\frac{I_Y}{I_X}\right)v_{IN} \qquad (8)$$

where β_N is the common-emitter current gain of the npn transistors. The second term in the parenthesis represents the nonlinearity error in the transconductance against bias current ratio characteristics of the OTA.

2. Channel-Length Modulation Effect

The influence of channel-length modulation on the transfer characteristic is mainly caused by the changes in v_{DS} of M_1 and M_3 when the voltage signal source is applied at the positive input terminal and the negative terminal is connected to ground. Analyzing the OTA with the transistor large-signal model which incorporates this effect, we can obtain the transfer function modified as follows:

$$i_{OUT} \cong \frac{I_Y}{I_X}\frac{1}{R_s}\left[1-\frac{\lambda_N}{2}\sqrt{\frac{I_X}{2K}}\left(\sqrt{1+\frac{v_{IN}}{R_sI_X}}+\sqrt{1-\frac{v_{IN}}{R_sI_X}}\right)\right]v_{IN} \qquad (9)$$

where λ_N is a channel-length modulation parameter of the NMOS transistors. The second term in brackets represents the nonlinearity error in the transconductance against input voltage characteristic.

3. Body Effect

In Fig. 1, only the input transistors M_1 - M_4 may contribute to this effect. However, since each of body terminals has made to be connected to their respective source terminals, one can find no body effect occurs.

Ⅳ. Simulation Results and Discussion

The circuit shown in Fig. 1 was simulated using SPICE. The SPICE model parameters for bipolar and MOS transistors are given in table 1. W/L = 120/12 was used for all MOS devices. The resistors used were R_S = 40rm40k Ω and R_C = 200kΩ. The bais current I_X was set to 25 A for convenience. All measurements were performed at supply voltages of V_{DD} = 10 V and V_{SS} = -10 V. The dc transfer characteristic of the simulated circuit for a fixed I_Y of 50 A is plotted in Fig. 2 as the dotted line. The linearity error relative to the straight line of slope G_m = 47.3 μS is also plotted. The nonlinearity is seen to be less than ±1 percent over the input voltage range from -1.0 to 1.0 V.

Table 1. The SPICE model parameters for bipolar and MOS transistors.

PSPICE MODEL PARAMETER
NPN (Is=6.734f Ikf=3 Eg=1.11 Vaf=74.03 Bf=416.4 Ne=1.259 Ise=6.734f Ikr=86.78m Itb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1 Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75 Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)
NMOS (LEVEL=2 UO=521.3 VTO=917E-3 NFS=0.6E+12 TPG=1.0 TOX=22.5E-9 NSUB=5.7E16 UCRIT=50.0E3 UEXP=85.6E-3 VMAX=49.5E3 RSH=349.7 XJ=300.0E-9 LD=202.8E-9 DELTA=5.28 PB=0.8 JS=10E-6 NEFF=3.1 WD=222.7E-9 CJ=462.1E-6 MJ=421.2E-3 CJSW=4.5E-10 MJSW=169.0E-3 CGSO=310E-12 CGDO=310E-12 CGBO=340E-12 PC=500.0E-3 XQC=1.0)
PMOS (LEVEL=2 UO=167.5 VTO=-915E-3 NFS=0.65E+12 TPG=-1.0 TOX=22.5E-9 NSUB=3.7E16 UCRIT=10.0E3 UEXP=99.3E-3 VMAX=28.683 RSH=418.2 XJ=300.0E-9 LD=70.9E-9 DELTA=2.15 PB=0.8 JS=10E-6 NEFF=0.931 WD=408.2E-9 CJ=394.8E-6 MJ=454.3E-3 CJSW=4.5E-10 MJSW=210.8E-3 CGSO=108E-12 CGDO=108E-12 CGBO=625E-12 PC=500.0E-3 XQC=1.0)

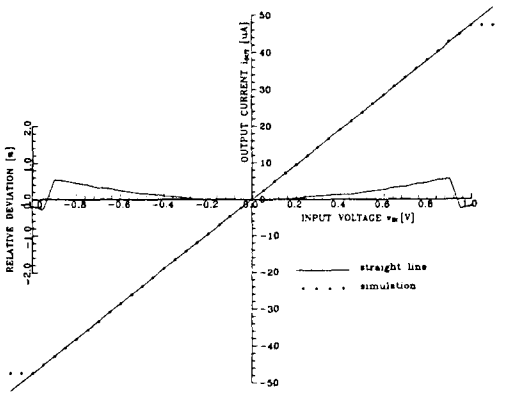

Fig. 2. Transfer characteristics of the OTA.

The relation between the transconductance and the bias current ratio was measured by fixing v_{IN} = 0 . 5 V and varying I_Y from 10 nA to 1 mA. The results are plotted in Fig. 3 and show that the transconductance is linearly dependent upon the bias current I_Y over the range of 0.01 ~ 100μA (four

decades) with a sensitivity of 1 S/A. The relation between the output resistance and the bias current I_Y is also measured. The results are plotted in Fig. 4.

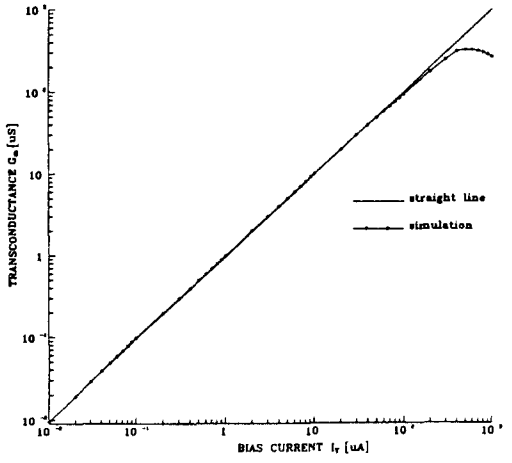

Fig. 3. The transconductance against bias current ratio characteristic of the OTA.

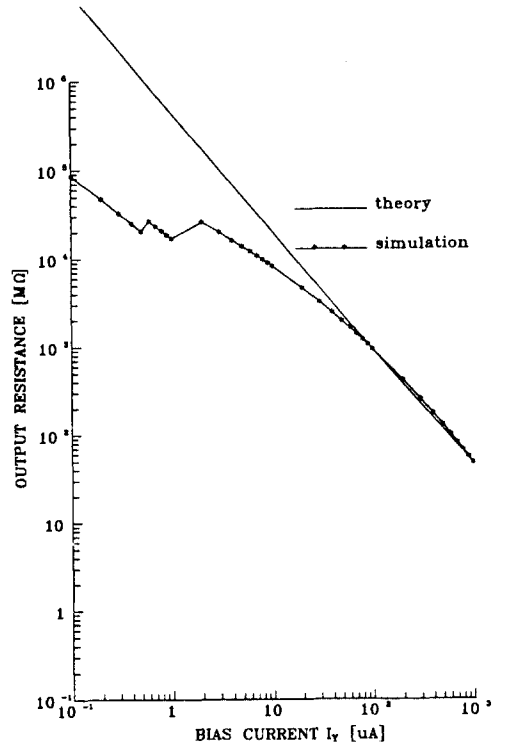

Fig. 4. The output resistance against bias current ratio characteristic of the OTA.

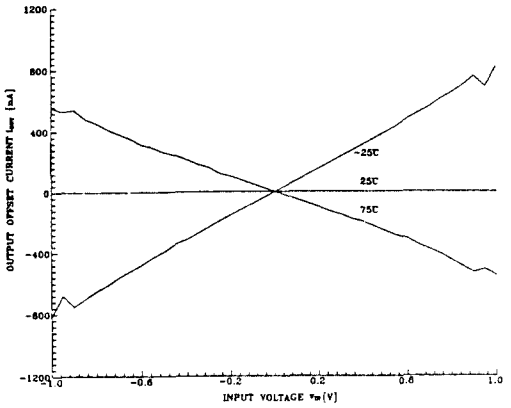

Fig. 5. Temperature characteristics of the OTA.

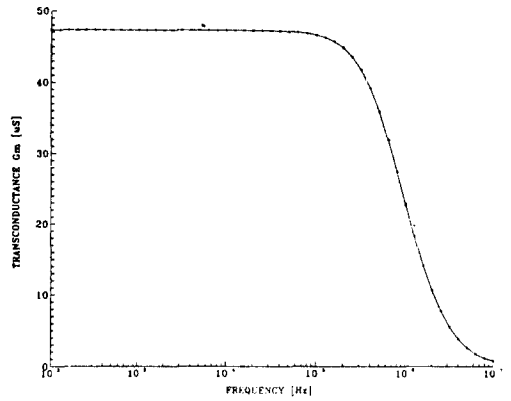

Fig. 6. Frequency characteristics of the OTA.

The dependency of output current on temperature was also simulated with a fixed I_Y of 50 A. The results are plotted in Fig. 5 in which output offset currents at -25℃ and 75℃ are estimated with reference to the output current at 25℃. The offset current is maintained to within ±16 nA/℃ over the entire input voltage range. The output dc offset current measured with I_Y = 50 A and grounded input terminals was -3.6 nA. This offset is about ten times lower than that of the bipolar OTA simulating under the same bias condition. Furthermore, if W/L = 107/12 is chosen for the M_{28} transistor, the output dc offset current can be reduced to -1.1 pA. The input dc current was found to

be 0 A. The measured power consumption was 4.13 mW. Finally, the frequency characteristics of the OTA was investigated. The results are shown in Fig. 6. The measured 3-dB cutoff frequency was about 500 kHz.

V. Conclusions

A BiCMOS OTA has been described. Its linearity and temperature stability are comparable to those of the bipolar counterpart. A significant advantage over the bipolar one is that the improved dc performance can be achieved by the appropriate choice of device dimensions. Therefore, the proposed BiCMOS OTA is expected to find wide applications in data conversion and precision measurement systems.

Acknowlegment

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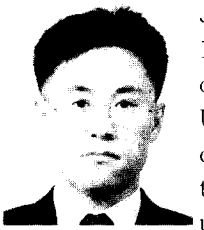

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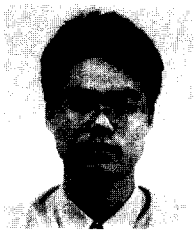

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