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반응성 이온 식각에 의해 손상된 실리콘의 세정에 관한 연구

논문 7-4-3

A Study on Cleaning Process of RIE Damaged Silicon

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요 약

$CHF_3/CH_4/Ar$ 플라즈마에 의해 형성된 산화막 식각 잔류물의 화학구조와 이 잔류물의 제거를 위한 세정방법을 x-ray photoelectron spectroscopy를 이용하여 조사하였다. 잔류물의 구조는 CF_x-polymer와 Si-C, Si-O 결합으로 이루어진 SiO_yC_z 이었다. CF_4/O_2 플라즈마에 의한 silicon light etch는 산화막 식각 잔류물인 SiO_yC_z층과 손상된 실리콘 표면을 제거하였으며 $NH_4OH-H_2O_2$과 HF 용액으로 완전히 제거되는 CF_x-polymer/SiO_x층을 남겼다. 100Å정도의 silicon light etch는 minority carrier life time과 thermal wave signal 값을 초기 웨이퍼 수준까지 회복시켰으며 접합누설 전류도 거의 습식 식각 공정 수준까지 감소시켰다.

Key Words(중요용어): RIE(반응성 이온식각), Etch anisotropy(식각 이방성), Leakage current(누설전류), Residual layer(잔류층), Post-RIE cleaning(식각후 세정).

I. Introduction

Reactive ion etching(RIE) is widely used for fine line pattern transfer in the manufacture of ultra large scale integration(ULSI) devices. RIE is a particular dry etching technique characterized by the fact that it combines physical sputtering with the chemical etching and offers high etch anisotropy and selectivity. The selectivity of SiO_2 etching over Si etching in CH_4/H_2 plasmas is attributed to fluorocarbon polymer film formation on the Si surface, while the highly anisotropic nature of SiO_2 etching is based on energetic ion bombardment of the etched surface[1,2]

For the CF_4/H_2 plasmas, apart from deposition of a thin fluorocarbon/silicon carbide film, near-surface damaged and contaminated layers are observed[3-5]. A large number of studies[6-7] have reported the degradation of electrical properties of Si, SiO_2 quality and metal to Si contact resulting from the direct exposure of Si to the reactive plasma. The thermal annealing treatment for post-RIE cleaning have been suggested to remove the RIE residues and the silicon lattice disorder[8,9]. However, the thermal annealing treatment could not recover the minority carrier life time of damaged silicon and reduce the junction leakage current. Furthermore, it was found that an oxide growth was retarded on the exposed area in a subsequent thermal oxidation step after the oxide etching using $CHF_3/CF_4/Ar$ plasma.

In this paper we reporte the structure and chemical composition of an oxide RIE residue on Si substrate when $CHF_3/CF_4/Ar$ plasma was used, and also present a new post-RIE cleaning method whitch is suitable for deep sub-micron device process.

II. Experimental

Silicon dioxide layers of 2000Å thickness

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were formed by chemical vapor deposition(CVD) on p-type Si(100) wafers, 9-12 ohm cm, pre-cleaned using NH_4OH-H_2O_2(SCI) and $50H_2O$-1HF (HF) solution. The dry etching experiments were performed in commercially available magnetic enhanced reactive ion etch(MERIE) system using $15CHF_3/8CH_4/60Ar$ plasma. The amount of overetching was varied from normal 10% to 100 %. The oxide layer on control sample was completely removed by wet etching in the HF solution.

Post-RIE cleaning steps, either wet or dry-wet cleanings, were applied to removing the oxide etch residue. Three wet cleaning processes were used: H_2SO_4-H_2O_2(SPM), SCI, and HF. Dry cleanings included O_2 remote plasma ashing (O_2 plasma), ultraviolet/O_3 ashing(UV/O_3), and CF_4/O_2 remote plasma(silicon light etch). The flow chart for sample preparation is shown in Fig. 1.

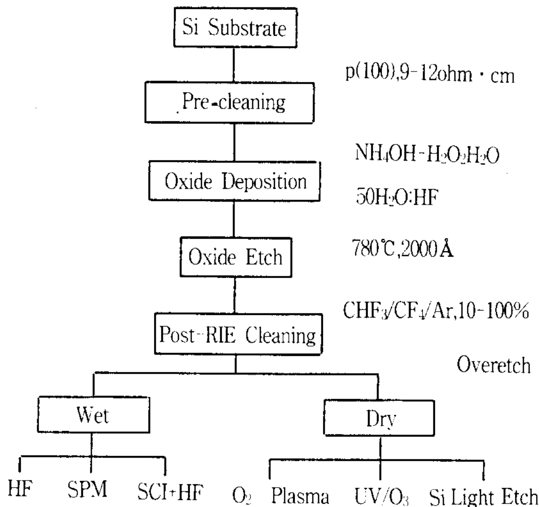

Fig. 1. Process flow chart for sample preparation.

The residual layer was examined using a Perkin-Elmer 5400 x-ray photoelectron spectroscopy(XPS). For electrical evaluation, minority carrier life time and n^+/p junction leakage current were measured using LEO life time measurement and HP4145 semiconductor parameter analyser, respectively. Thermal wave(TW) technique was performed to evaluate a degree of damage after RIE and post-RIE cleaning. TW signals of samples were measured with a Therma-Probe Model 200 system.

Ⅲ. Results and Discussion

Main residual elements by oxide RIE were silicon, carbon, oxygen, and fluorine as shown in Fig. 2. Major bonding states of Si_{2p} in Fig. 2(a) were Si-Si(99.5eV), Si-C(100.2eV), and Si-O(102.5eV). Si-O bond state was different from that of thermal oxide of which typical binding energy is 103.5eV. In C_{1s} peak(b), C-Si(283.4eV), C=O(284.9eV), C-F(287.4eV), C-F_2(290.0eV), and C-F_3(292.5eV) were observed. The last three bonding states were attributed to fluorocarbon (CF_x) polymer. F_{1s} peak (c) at 686eV was hard

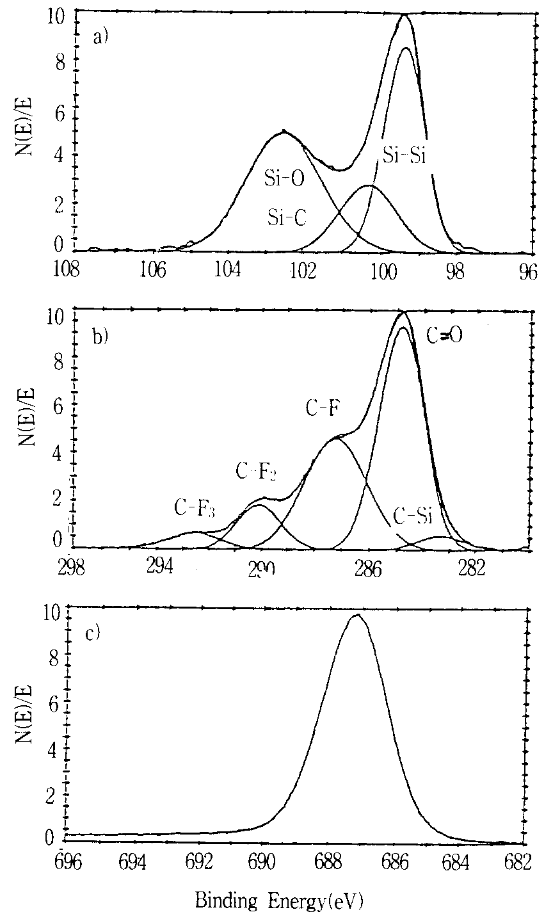

Fig. 2. XPS spectra of the oxide etch residue: (a) Si_{2p} peak (b)C_{1s} peak (c)F_{1s} peak

to identify the fluorine bond states in detail due to the highest electronegativity. The Si-O and Si-C bonds seemed to form one compound of SiO_yC_z. The reason why Si-O and Si-C bonds were not interpreted as SiO_2 and SiC, respectively is that the Si-O bond of the etch residue was chemically inert in HF acid so that there was no change in Si_{2p} peaks after HF treatment irrespective of dip time.

In order to examine the structure of residual layers, XPS analysis with various take off angle was carried out. Figure 3 shows that XPS data of Si_{2p} and C_{1s} with different take-off angle. It was found that the Si-O peak rapidly decreased with increasing the take-off angle comparing to Si-C peak, implying that Si-O bond is located toward top surface. The quantitative explanation of y and z in SiO_yC_z is as follows. With increasing the photoelectron take-off angle, the area ratio of Si-C to Si-O increased, which indicated that carbon content increased and oxygen content decreased with depth towards the Si substrate. Table 1 summarizes the dependence of the area ratio of Si-C to Si-O on photoelectron take-off angles. Therefore, the ratio of y to z in SiO_yC_z layer was monotonously changing with depth. The value of y/z was maximum at the interface between CF_x-polymer and SiO_yC_z, and minimum at the interface between SiO_yC_z and Si substrate.

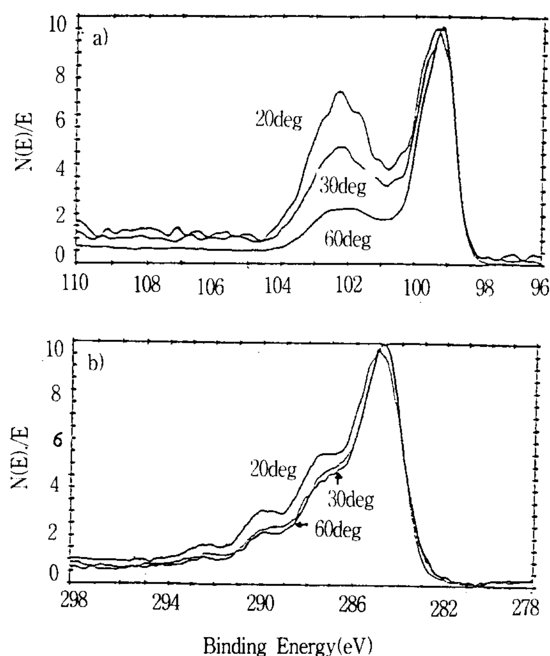

Fig. 3. XPS spectra with different photoelectron take-off angle:(a)Si_{2p} (b)C_{1s}

When wet cleaning methods were applied, C_{1s} and Si_{2p} peak were found to be unchanged, implying that wet cleaning methods were inactive in removing both the CF_x-polymer and SiO_yC_z. Since wet cleaning only was ineffective in removing the oxide etch residue, dry and wet cleaning was proposed. Three dry cleaning methods, O_2 plasma, UV/O_3, and silicon light etch(CF_4/O_2) were performed. SCI and HF were mainly used for the following wet cleaning process.

Table 1. Photoelectron take-off angle dependance of Si-C, Si-O peak(cps) and their ratio (Si-C/Si-O).

Take-off Angle	Si-C (100.2 eV)	Si-O (102.5 eV)	Ratio
20°	30	73	0.411
30°	80	150	0.533
45°	140	250	0.560
60°	306	347	0.862

Figure 4 shows that XPS data for the samples after dry-wet cleaning treatment. It was found that O_2 plasma and UV/O_3 had small

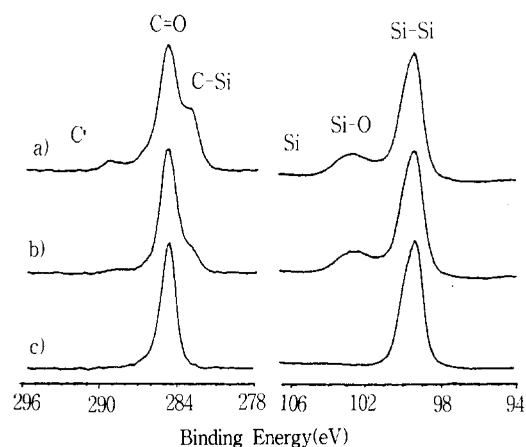

Fig. 4. XPS spectra after dry-wet cleanings: (a) O_2 plasma (b) UV/O_3 (c) silicon light etch.

C-Si bond in C_{1s} peak and Si-O bond in Si_{2p} peak. These cleaning methods almost completely removed fluorocarbon polymer film through oxidation but left the SiO_yC_z unremoved. When only silicon light etch was applied, the residual layer was changed to CF_x-polymer/SiO_2, that is, Si-C bond vanished even though the result is not shown. The silicon light etch residue, CF_x-polymer and SiO_2, was completely removed by SCI and HF dip. The XPS spectrum of wafer at this stage was exactly the same as that of an initial wafer which was just dipped into HF solution. Oxide etch residue was completely removed and no retardation of thermal oxidation was found when silicon light etch followed by SCI and HF dip was applied. This result suggests that SiO_yC_z layer is responsible for blocking further thermal oxidation.

Minority carrier life time value for the sample with different post-RIE cleaning treatment is shown in Fig. 5. Wet cleanings could not recover the damaged surface. Compared with initial minority carrier life time, silicon light etched wafer recovered minority carrier life time most effectively but UV/O_3, and O_2 plasma did not recover the etch damage that much.

In order to obtain the proper silicon etch condition, minority carrier life time and thermal wave signal are measured as a function of silicon light etch thickness and the results are shown in Fig. 6. It is observed that more than 100Å etched samples have almost the same values of minority carrier life time and thermal wave signal as control sample. This result suggests that 100Å silicon light etch is required to remove RIE residue and damage. Silicon consumption due to silicon light etch should be minimized to maintain surface doping concentration and improve shallow junction characteristics.

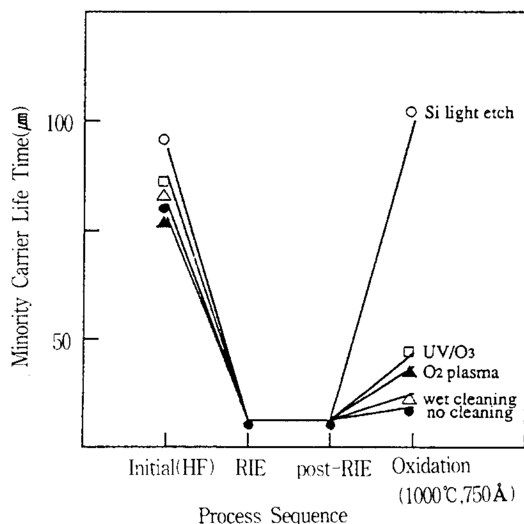

Fig. 5. Minority carrier life time of the samples with various post-RIE treatment.

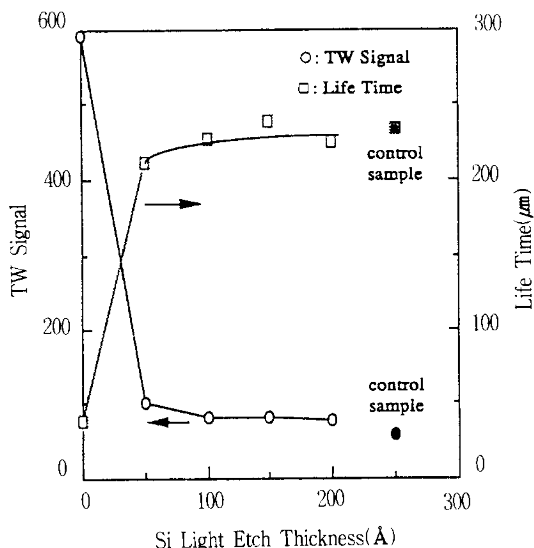

Fig. 6. Minority carrier life time and thermal wave signal as a function of silicon light etch thickness.

In order to verify the effect of silicon light etch on the quality of Si substrate, n^+/p junction with area of $5\times10^{-3}cm^2$ was fabricated and a leakage current was measured. Figure 7 shows that the leakage current for the samples with various amount of overetching and with and without silicon light etch. The junction leakage of control sample shows 4.5nA/pattern at 3.3V. When only wet cleaning was applied for post-RIE cleaning, junction leakage current sharply increases with increasing overetch amount. However, in case of silicon light etch, leakage current is almost independent of overetch amount upto 100%, resulting from the removal of RIE residue and damage.

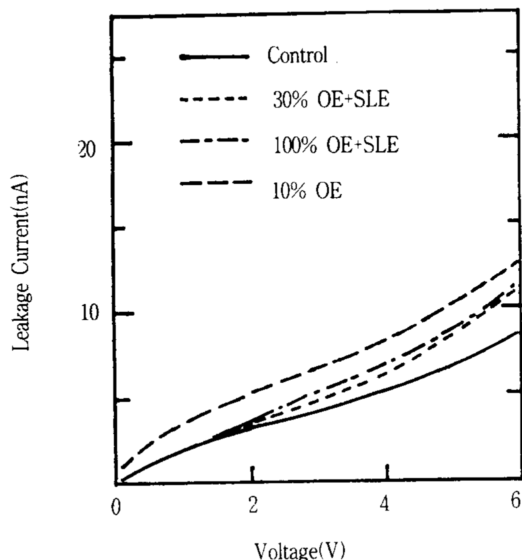

Fig. 7. Junction leakage current of samples with only wet etching(control) and different RIE overetching(OE) amount with and without silicon light etch(SLE).

Ⅳ. Conclusions

The chemical structure of oxide etch residue was found to be CF_x-polymer/SiO_yC_z. Silicon light etch completely removes RIE residue and damage and leaves CF_x polymer and SiO_2 layer, which is removed by NH_4OH-H_2O_2 mixture and $50H_2O$-HF treatment. The silicon light etch around 100Å followed by wet cleaning recovered the minority carrier life time and reduced the thermal wave signal and junction leakage current nearly to that of oxide wet etch process. From the consideration of minority carrier life time, thermal wave signal, leakage current and silicon consumption, silicon light etch is suitable for deep sub-micron device process.

Acknowledgments

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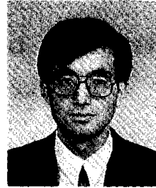

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