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Short Note

Low temperature growth of silicon thin film on sapphire substrate by liquid phase epitaxy for solar cell application

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사파이어 기판을 사용한 태양전지용 실리콘 박막의 저온액상 에피탁시에 관한 연구

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Abstract Deposition of silicon on pretreated sapphire substrates has been investigated by the liquid phase epitaxy method at low temperatures. An average 14 μm thickness of silicon was grown over a large area on sapphire substrate originally coated with a much thinner silicon layer [0.5 μm (100) Si/(1$\bar{1}$02) sapphire] at low temperature from 380°C to 460°C.

요 약 [0.5 μm (100) Si/(1$\bar{1}$02) sapphire] 기판상에 액상 에피탁시 방법으로 태양전지용 실리콘 박막형성을 시도하여, 평균 14 μm 두께의 실리콘 박막을 아주 낮은 온도범위 (380°C ~ 460°C)에서 성장시켰다.

With conventional chemical vapour deposition (CVD) techniques, the deposition temperature of silicon on sapphire is in the range of 900 ~ 1200°C. From these growth temperatures, when it is cooled to room temperature, stress forms in the silicon film because of the large difference of thermal expansion coefficients of silicon and sapphire [1]. Also in this temperature range, contaminants from the substrates are introduced into the silicon films.

By employing the lower temperature liquid epitaxy method, it may be possible to relieve residual stress, to reduce contamination and to make much thicker silicon film above 10 μm.

As grown CVD silicon on sapphire wafers purchased from Union Cabide were used as substrates which was originally coated a 0.5 μm thickness silicon layer. In this work, the original idea was to use this thin silicon layer as a seed to deposit a thick layer at much lower temperature. To clean silicon on sapphire wafers, RCA solution was used [2], and boiling aqua solution [3] was employed for the sapphire side to clean the resistant surface. Ultrasonic cleaning also provides an efficient method of removing the more strongly adherent contaminants.

By using the standard sliding boat system [4], nucleation patterns on sapphire substrate were studied and the growth of a large area Si layer (14 μm thickness) was achieved. This boat, containing both a source wafer and a substrate, is placed in a furnace with a flowing nitrogen gas ambient. Prior to heating to melt saturation temperature, the furnace was evacuated to 0.01 pascals. The vacuum assists in reducing the amount of oxygen in the tube and allows the operater to check that all the fittings and end caps are tightly closed. The boat is machined from high graphite which avoids contamination of the melts. A hole was drilled through the base of the boat to accomodate a Type R (Pt-Pt.Rh) thermocouple sheathed in a quartz tube.

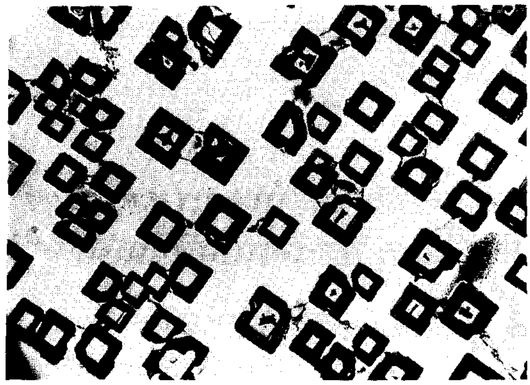

Fig. 1. SEM. Nucleation pattern of silicon on sapphire substrate. Mag. ×90, Growth temperature : 380 ~ 460℃.

The melts for the LPE was gold-60 wt % bismuth alloy. Solubilities in this and related melts are summarized in an other reference [5]. The growth temperature was from 380℃ to 460 ℃.

A typical nucleation pattern of Si is shown in Fig. 1. Each crystallites formed a pyramidal shape. This is basically the same as the nucleation pattern of Si on (100) oriented Si substrates. This is not surprising , since this sapphire substrate has an epitaxially grown CVD (100) Si layer on top of it. This substrate has also a high density of defects at the silicon/sapphire interface because of lattice mismatch effect between the two layers. The lattice mismatch between the (100) silicon on (1102) sapphire is 12.5 % in the (1120) direction and 4.2 % in the (1101) direction [6]. The silicon located on highly defected regions of the interface between silicon and sapphire may be easily etched away upon contact with the metallic solvent, especially during the melt-back step.

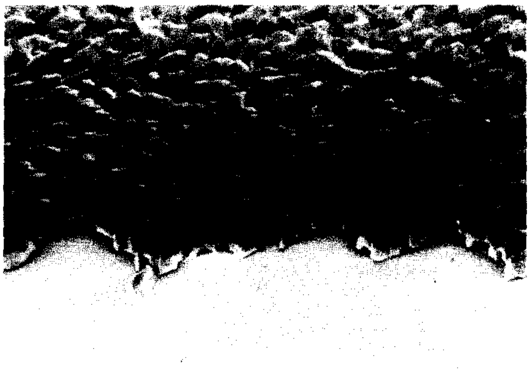

Fig. 2. SEM. The surface morphology of silicon layer on sapphire substrate. Growth temperature : 380 ~ 460℃.

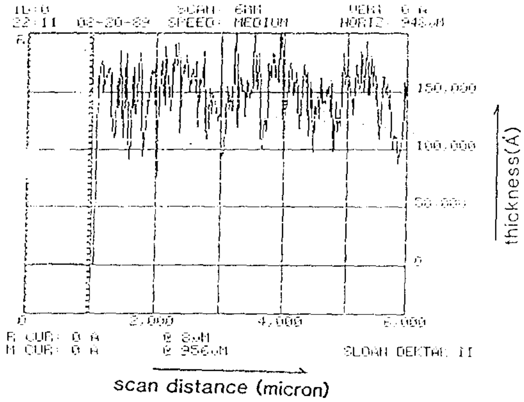

Fig. 3. The thickness of silicon layer on sapphire substrate (SLOAN DEKTAK Ⅱ) ES-9.

This could explain the bare regions between crystallites in Fig. 1.

With more prolonged growth, coalecing layers were formed. The surface morphology of these thin coalescing layer was observed by scanning electron microscope with results shown in Fig. 2. The surface morphology of these thin layer looks rough. The reasons for this rough appearance comes from the coalescing of pyramids with a flat top surface. The rough surface thin film could be applied to trap light into cells processed on such films. The thickness of LPE layer was measured by SLOAN DEKTAK II. The average thickness is 14 μm in this case (Fig. 3).

This appears to be the first time that thick silicon layer has been deposited on sapphire substrate by the liquid phase epitaxy method at very low temperature.

Acknowledgements

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