論 文

Design of a New CMOS Differential Amplifier Circuit

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새로운 구조를 갖는 CMOS 차동증폭회로 설계

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ABSTRACT

All of the CMOS analog and analog-digital systems have composed with several basic circuits, and among them, a important block, the amplifier part can affect the system's performance. Therefore, according to the uses in the system, the amplifier circuit have designed as various architectures(high-gain, low-noise, high-speed circuit, etc…).

In this paper, we have proposed a new CMOS differential amplifier circuit. This circuit is differential to single ended input stage comprised of CMOS complementary gain circuits having internally biasing configurations. These architectures can be achieved the high gain and reduced the transistors for biasing. As a results of SPICE simulation with the standard 1.5㎛ processing parameter, the gain of the proposed circuit have a doubly value of the typical circuit's while maintaining other charateristics(phase margin, offset, etc…). And the proposed circuit is applicated in a simple CMOS comparator which has the settling time in 7nsec(CL=1pF) and the high output swing(±4.5V).

要 約

CMOS아날로그 및 아날로그-디지탈시스템은 여러개의 기본회로로 구성되어지며 그중에서도 증폭회로 부분은 시스템의 성능을 결정할 수도 있는 중요한 블럭중의 하나이다. 증폭회로는 시스템에서 사용되어지는 용도에 따라서 여러가지 구조(고이득, 저전력, 고속회로등)를 가지며 이러한 증폭회로를 설계하기 위하여 증폭기내의 입력증폭단의 설계 방법도 다양하다.

본 논문에서는 CMOS 상보형 차동이득 구조를 갖는 새로운 형태의 입력 차동증폭 회로를 제안하였다. 제안된 회로는 CMOS 상보형 회로에 의하여 고이득 특성을 가지며, 바이어스 전류를 내부적으로 공급하여 전체 시스템 구성시, 바이어스회로를 구성하기 위한 트랜지스터의 수를 줄일 수 있다. 이 회로를 표준 1.5㎛ 공정파라메타를 이용한 SPICE 시뮬레이션을 통하여 광범위하게 이용되고 있는 CMOS 차동증폭회로와 비교해 본 결과, 오프셋, 위상마진등의 특성이 그대로 유지된 상태에서 이득이 배가 되었다. 또한 제안된 회로를 이용하여 높은 출력스윙(−4.5V − +4.5V)과 함께 7nsec(CL=1pF)이하의 세틀링시간을 갖을 수 있는 CMOS비교기를 설계하였다.

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Ⅰ. Introduction

The implementation of the high performance analog functions in MOS technology has become increasingly important. Thus great strides have recently been made in implementing functions such as high speed ADC/DAC systems, sampled data analog filters, voltage references, instrumentation amplifier, high speed voltage comparator, and so forth, voltage references, instrumentation amplifier, high speed voltage comparator, and so forth, in CMOS and NMOS technology. These developments have been well documented in the literature. These high performance amplifier circuits play key roles in most of analog subsystems[1-7].

The CMOS differential amplifier circuits widely used in the CMOS analog subsystems have designed as many architecture to improve the circuit's performance, among them several types of the typical amplifier architectures are referred as follows[1-3] :

(i) The type having the current mirrors in the input stage.

(ii) The type having the cascode loads to achieve the high voltage gain.

(iii) The type which comprised of the fully differential architecture.

The type (i) require the other gain stages to improve the high voltage gain, because its input voltage gain is small. And, the type (ii) can be earned the high gain by the cascode loads, but a disadvantage of this configuration is that it can make the circuit's size large. Next, the type (iii) has good characteristics(high CMRR, PSRR and low offset, etc…), but this configuration should be used many transistors for composing the fully differential architecture.

After all, above-mentioned amplifier circuits have strong and weak points, and the merits of these circuits can be applied to many analog and analog-digital systems. However, their drawback should be improved for using in the high performance circuit design.

In this paper, we have proposed a new CMOS differential amplifier circuit which can be improved the voltage gain. And the primary emphasis on designing is placed on the gain enhancement. The proposed differential amplifier circuit is composed of the CMOS complementary circuit for achieving the high voltaga gain, and internal biasing circuit for the high speed operation. The performance of the proposed circuit is compared with that of the typical CMOS differential amplifier circuit(type (i)) which widely used in the analog subsystems.

Section Ⅱ in particular deals with the new CMOS differential amplifier circuit architecture, and the characteristics of this circuit are compared with a typical CMOS differential amplifier circuit by SPICE simulation. Section Ⅲ describes the simple high speed CMOS comparator composed of the improved CMOS amplifier circuit.

Ⅱ. A new CMOS differential amplifier circuit

1. The high gain characteristics

The designed CMOS differential amplifier circuit is the high gain amplifier circuit which makes full use of the complementary device symmetry available in CMOS technology. In this circuit(Fig.2), the MOS transistors M1, M2, M3 and M4 are comprised of push-pull devices, and, the drains of M1 and M2 are connected with the gates of M5 and M6, for biasing current supply. The gain of the circuit can be made larger than that of a typical CMOS differential gain circuit (Fig.1).

Assume that the designed complementary CMOS amplifier circuit is compared to a typical CMOS differential amplifier circuits. First, we consider the differential gain of the typical CMOS differential amplifier circuit. The Fig.1(a), shows the typical CMOS differential to single ended amplifier circuit with current mirror loads and the Fig. 1(b) is the small signal equivalent circuit.

An apprioximate analysis of the circuit can be readily performed as follows. Assuming that the current source I_0 is ideal, the incremental drain

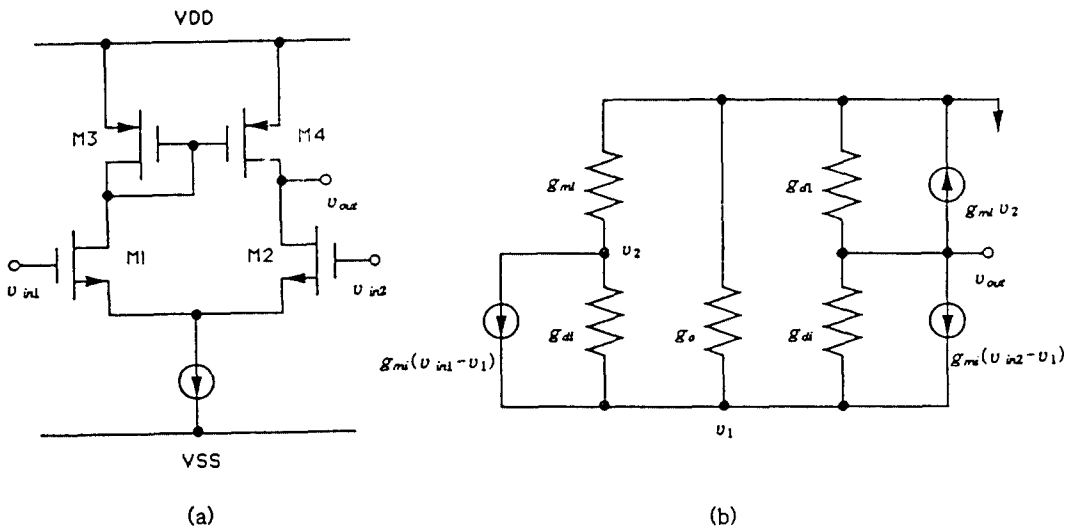


Fig. 1. (a) Typical CMOS differential to single ended amplifier circuit.
(b) The small signal analysis equivalent circuit.

currents of M1 and M2 must satisfy

$$i_{d1} + i_{d2} = 0 \tag{1}$$

Also, if both M1 and M2 are in saturation, then

$$i_{d1} \cong g_{mi}(v_{in1} - v_1), \text{ and} \tag{2}$$
$$i_{d2} \cong g_{mi}(v_{in2} - v_1).$$

Combining these equations,

$$v_1 \cong \frac{v_{in1} + v_{in2}}{2} \tag{3}$$

results. Hence,

$$i_{d1} = i_{d2} \cong \frac{g_{mi}(v_{in1} + v_{in2})}{2} \tag{4}$$

The current i_{d1} is easily imposed M3 by M1, since the impedance at the common terminal of the gate and drain of M3 is only $1/g_{m3}$. Transistors M3 and M4 form a current mirror, and hence the current through M4 satisfies $i_{d4} = i_{d3} = i_{d1}$. Thus, both M2 and M4 supply the current $i_{d1} = g_{mi}(v_{in1} - v_{in2})/2$ into the output terminal. Since the output is loaded by the drain resistances of M2 and M4, the output voltage is

$$v_{out} \cong \frac{2\,i_{d1}}{(g_{di} + g_{dl})} \cong \frac{g_{mi}(v_{in1} + v_{in2})}{(g_{di} + g_{dl})} \tag{5}$$

The differential gain is thus

$$A_{dm} \cong \frac{v_{out}}{(v_{in1} - v_{in2})} \cong \frac{g_{mi}}{(g_{di} + g_{dl})} \tag{6}$$

Analysis shows the differential gain for the typical differential to the single ended amplifier is expressed by Equation (6).

We next define the differential gain of the new CMOS amplifier circuit using the small signal analysis. The designed new CMOS differential amplifier circuit and the small signal equivalent circuit representation are shown in Fig.2.

Let us assume that the current source I_0 is ideal, and the sum of the drain currents of the M1, M2 and M3, M4 is zero as follows,

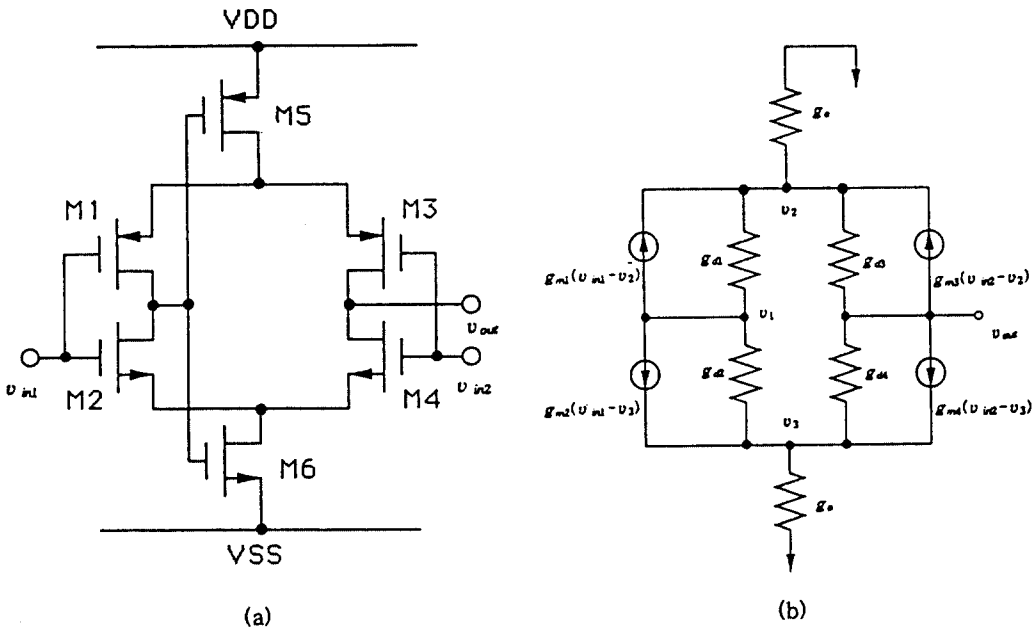


Fig. 2. (a)The proposed new CMOS differential amplifier circuit.
(b)The small signal analysis equivalent circuit.

$$i_{d1} + i_{d2} = 0 \tag{7}$$

where

$$i_{d1} \cong g_{m2}(v_{in1} - v_3) + g_{m1}(v_{in1} - v_2), \tag{8}$$
$$i_{d2} \cong g_{m4}(v_{in2} - v_3) + g_{m3}(v_{in2} - v_2)$$

Combining above two equations we have

$$i_{d1} + i_{d2} \cong g_{m2}(v_{in1} - v_3) + g_{m1}(v_{in1} - v_2) \tag{9}$$
$$+ g_{m4}(v_{in2} - v_3) + g_{m3}(v_{in2} - v_2) \cong 0$$

Here, because the size of the duplicated MOS transistors are symmetrically composed, we can set the transconductances the same as ; $g_{m1} \cong g_{m3}$, $g_{m2} \cong g_{m4}$.

And also, the voltages v_2 and v_3 can be set to the same values in the circuit design. Hence, we can rewrite the equation (9) as follows.

$$i_{d1} + i_{d2} \cong g_{m2}(v_{in1} - v_3) + g_{m1}(v_{in1} - v_3) \tag{10}$$
$$+ g_{m2}(v_{in2} - v_3) + g_{m1}(v_{in2} - v_3) \cong 0$$

Therefore,

$$v_3 = \frac{v_{in1} + v_{in2}}{2} \tag{11}$$

Then, the current

$$i_{d1} \cong (g_{m1} + g_{m2})v_{in1} - (g_{m1} + g_{m2})v_3 \tag{12}$$
$$\cong (g_{m1} + g_{m2})v_{in1} - (g_{m1} + g_{m2})\frac{v_{in1} + v_{in2}}{2}$$
$$\cong \frac{(g_{m1} + g_{m2})}{2}(v_{in1} - v_{in2})$$
$$\cong -i_{d2}$$

Since the output is loaded by the drain resistances of M3 and M4, the output voltage is

$$v_{out} \cong \frac{2\,i_{d1}}{(g_{d3}+g_{d4})} \cong \frac{(g_{m1}+g_{m2})\,(v_{in1}-v_{in2})}{(g_{d3}+g_{d4})} \quad (13)$$

The differential voltage gain of the designed new CMOS amplifier can be defined simiarly as

$$A_{dm} \cong \frac{v_{out}}{v_{in1}-v_{in2}} \cong \frac{(g_{m1}+g_{m2})}{(g_{d3}+g_{d4})} \quad (14)$$

Now let's check gain in actural design. This gains are calculated using the 1.5㎛ processing parameters.

$\lambda = 0.1\,\frac{1}{V}$ $\qquad \mu_n = 700\ cm^2/V\ \text{sec}$

$\mu_p = 350\ cm^2/V\ \text{sec}$ $\qquad C_{ox} \cong 1.4\times10^{-7}\ fF/cm^2$

$I_D = 25\ \mu A$

As the above results indicate the gain of the designed CMOS complementary amplifier circuit is twice as large as the gain of the typical CMOS differential amplifier circuit.

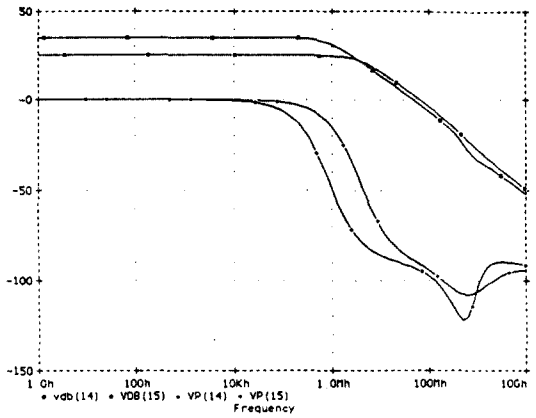
Fig.3. shows the characteristics(voltage gain, phase margin, input offset, CMRR, PSRR) between proposed new amplifier circuit and the typical CMOS differential amplifier circuit which are simulated by SPICE. And these results are presented table 2.

2. The current switching speed enhancement.

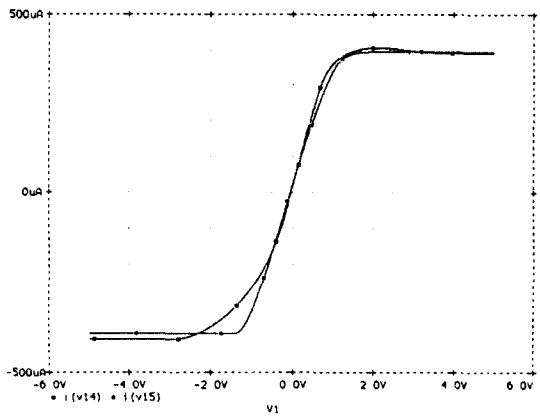
In modern CMOS system design, many analog circuits have employed external biasing circuit which supplies accurate voltage levels. But, some circuits use internal biasing circuits to earn a low-power wide-band state during the slewing or settling period[15].

Table 1. Calculation the gains of two differential amplifier circuits.

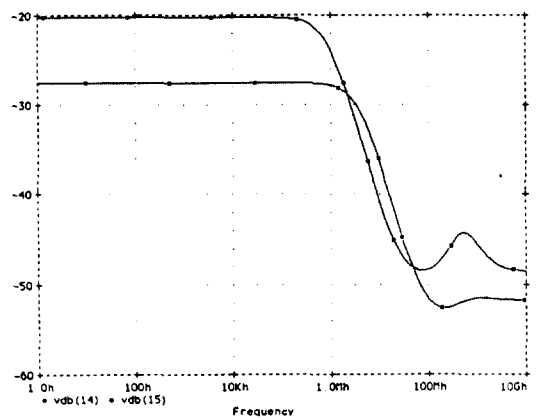
Typical Circuit	New Circuit
$A_{dm} = \frac{g_{m1}}{g_{d2}+g_{d4}} \cong g_{m1}\frac{r_{o4}}{2}$	$A_{dm} = \frac{g_{m1}+g_{m2}}{g_{d3}+g_{d4}} \cong (g_{m1}+g_{m2})\frac{r_{o4}}{2}$
$g_{m1} = \sqrt{2\,\mu_n C_{ox}\frac{W}{L} I_D}$	$g_{m1} = \sqrt{2\,\mu_p C_{ox}\frac{W}{L} I_D}$
$= \sqrt{2\times100\times10^{-6}\times\frac{9.5}{3}\times25\mu A}$	$= \sqrt{2\times50\times10^{-6}\times\frac{20}{3}\times25\mu A}$
$= \frac{1}{7.9\ k\Omega}$	$= \frac{1}{7.7\ k\Omega}$
$r_{o2} \cong r_{o4} = \frac{1}{0.1\times25\mu A} \cong 400\ k\Omega$	$g_{m2} = \sqrt{2\,\mu_n C_{ox}\frac{W}{L} I_D}$
	$= \sqrt{2\times100\times10^{-6}\times\frac{9.5}{3}\times25\mu A}$
	$= \frac{1}{7.9\ k\Omega}$
	$r_{o3} \cong r_{o4} = \frac{1}{0.1\times25\mu A} \cong 400\ k\Omega$
$Gain = g_m\frac{r_{o2}}{2}$	$Gain = (g_{m1}+g_{m2})\frac{r_{o4}}{2}$
$= \frac{200\ k\Omega}{7.9\ k\Omega}$	$= \left(\frac{1}{7.7\ k\Omega}+\frac{1}{7.9\ k\Omega}\right)200\ k\Omega$
$= 25.3\ (28\ dB)$	$= 51.28\ (34\ dB)$



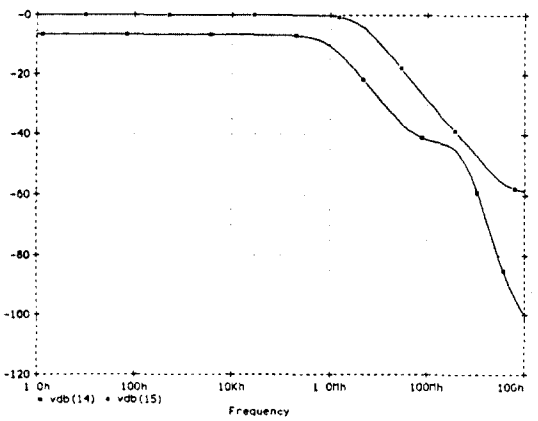
(a)Open Loop Gain, phase margin, unity gain frequency



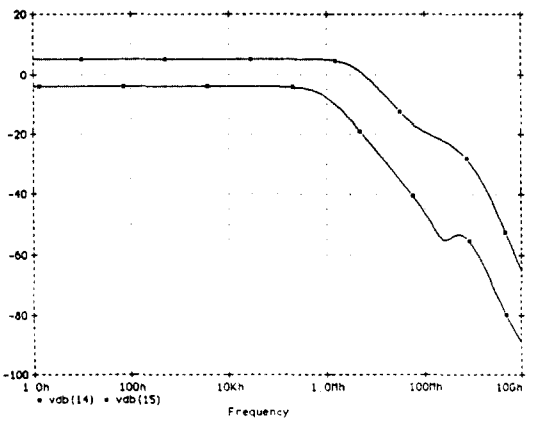
(b)Input offset voltages



(c)Common mode rejection ratio(CMRR)



(d)Power supply rejection ration of vdd(PSRR VDD)



(e)Power supply rejection ratio of vss(PSRR VSS)

Fig. 3. SPICE simulated results of two differential amplifier circuits.

Table 2. Transistors' Dimensions

Characteristics	Typical(CL=1pF)	New(CL=1pF)
Open Loop Gain	25 dB	35 dB
Phase Margin	89 °	92 °
Uniy gain Frequency	60 MHz	54 MHz
CMRR	42 dB	45 dB
PSRR VDD	25 dB	41 dB
PSRR VSS	30 dB	40 dB
Input Offset voltage	30 mV	10 mV

We have designed a biasing circuit that its biasing voltage is internally supplied. In Fig.2, the biasing voltages of the MOS transistors M5 and M6 are supplied by the drain voltages of the M1 and M2. Then, the MOS transistors M5 and M6 are not saturated by the biasing voltages, for operating in linear range.

This architecture has the property that it operates in the class AB mode, that is, when large input voltages are applied, the current flowing to the output increases to a value much larger than quiescent bias current in the circuit. This feature makes it particularly suitable for the high speed comparator applications.

Ⅲ. The design of the simple high speed CMOS comparator

When we design an n-bit flash ADC, 2^n-1 comparators are required. For medium-resolution ADC's, the amount of power and area assigned per comparator is of the utmost importance. Therefore, when evaluating different comparator topologies for use in flash ADC, it is desirable to minimize the power and area.[6,7]

The simple high speed CMOS comparator with the CMOS differential amplifier circuit advanced in Section Ⅱ, meets the above terms. This architecture has an appended MOS transistors M7, M8, and two CMOS gain stages made of MOS transistors M9-M12 are attached to the designed amplifier circuit(Fig.2). The Fig.4. shows the proposed simple CMOS comparator.

In this circuit, because the MOS transistors M5, M6 and M7, M8 are biased as a linear range, the voltages of the node ⓐ, ⓑ comparatively approached the power supply voltages VDD, VSS. And, when the input positive voltages are applied at node ①, and the negative voltage at node ②, the M2 and M3 are saturated. Therefore, the node ⓒ is negatived by the saturated transistor M2. Then the drain currents of the M5, M7 increase at node ⓐ. As a results, the switching current flowing to the output increases to a value much larger than quiescent bias current. This comparator has a high speed characteristics.

The dimensions of MOS transistors are presented in Table 3.

Table 3. Transistors' Dimensions

	MOS	L(㎛)	W(㎛)		MOS	L(㎛)	W(㎛)
M1	PMOS	3	20	M7	PMOS	2	3
M2	NMOS	3	9.5	M8	NMOS	6	3
M3	PMOS	3	20	M9	PMOS	3	22
M4	NMOS	3	9.5	M10	NMOS	3	10
M5	PMOS	2	3	M11	PMOS	3	22
M6	NMOS	6	3	M12	3	10	

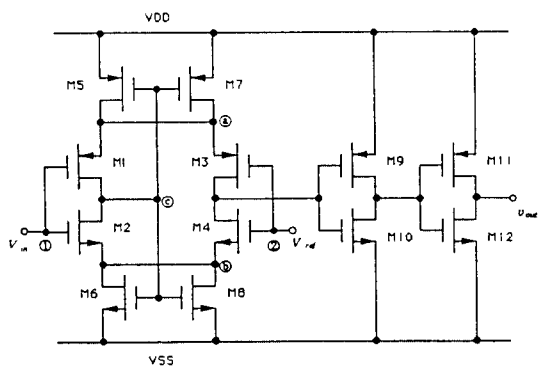


Fig. 4. The proposed CMOS high speed comparator

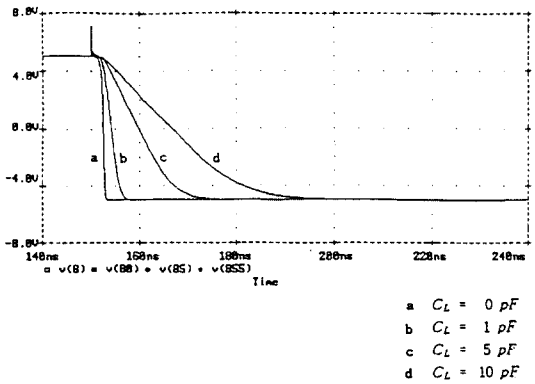


Fig. 5. Settling time of the comparator.

Table 4. Performances of the simple Comparator

Power Dissipation	$3\,mW$
Settling Time	$< 3\,nsec$, $C_l = 0\,pF$
	$< 7\,nsec$, $C_l = 1\,pF$
	$< 30\,nsec$, $C_l = 5\,pF$
	$< 80\,nsec$, $C_l = 10\,pF$
Comparison Capability $V_{in} = \pm 0.05\,V_{p\text{-}p}$ $V_{ref} = 0\,V$	Swing $-4.5V \sim +4.5V$, for $3\,nsec$, $C_l = 0\,pF$
	Swing $-4.5V \sim +4.5V$, for $7\,nsec$, $C_l = 1\,pF$
	Swing $-4.5V \sim +4.5V$, for $30\,nsec$, $C_l = 5\,pF$
	Swing $-4.5V \sim +4.5V$, for $80\,nsec$, $C_l = 10\,pF$
Output Swing	$-4.5V \sim +4.5V$

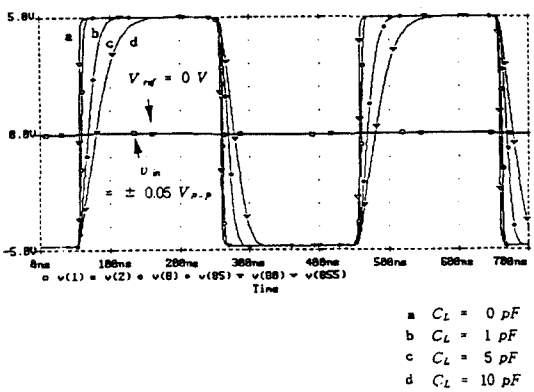


Fig. 6. Comparison capability of the comparator.

Ⅳ. Conclusions

The high performance amplifier circuits are key elements of most analog subsystems, particularly in operational amplifiers, high frequency switched capacitor filters, high speed comparator and AD/DAC system. And the charateristics of many systems is strongly influenced by the performance of the amplifier circuits used in those.

In this paper, a CMOS differential amplifier circuit with a new architecture has been designed. The proposed new amplifier circuit is composed with internal biasing circuits and the CMOS complementary gain stage for the performance improvement. And also, this circuit is compared with the typical CMOS differential amplifier circuit. As a SPICE simulation results of the comparing with the same MOS dimensions, we know that the gain of the proposed circuit have a doubly value of the typical circuit's while maintaining other charateristics(phase margin, offset, etc…). In addition, we have been designed a high speed simple CMOS comparator using the improved CMOS differential amplifier circuit. SPICE simulation shows that it has the settling time in 7nsec(CL=1pF) and the high output swing (±4.5V).

The proposed new differential CMOS amplifier circuit and the high speed simple CMOS comparator will be applicated in the high speed analog subsystem, especially the flash A/D converter.

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本 論文을 指導하여주신 故 金炯甲 先生님의 冥福을 비옵니다.

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