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IBM-PC를 위한 다목적용 데이타 수집 및 컨트롤 장치의 개발

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Disign and Evaluation of a Versatile Data Acquisition and Control Adaptor for IBM Personal Computers

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요 약. IBM-PC를 위한 다목적용 데이타 채집 및 컨트롤 장치를 개발하였다. 개발된 데이타 채집 및 컨트롤 장치는 컴퓨터를 이용한 데이타 채집 및 기기 컨트롤에 필요한 주요 기능을 대부분 보유하고 있다. 아날로그 신호는 최고 4쌍의 차동신호를 받을 수 있으며 실험조건에 따라 두 개의 12-bit A/D 컨버터를 선택하여 처리할 수 있다. 또한 2개의 12-bit D/A 컨버터와 3채널의 16-bit 카운터/타이머, 그리고 24-bit 디지탈 입출력장치 등 실험실에서 컴퓨터를 이용한 실험자동화에 필요한 대부분의 기능을 가지고 있어 다목적용으로 사용될 수 있다.

ABSTRACT. A versatile data acquisition and control adaptor for IBM personal computers has been developed. The data acquisition and control adaptor developed contains major components necessary for computerized data acquisition and control instrumentaions. Up to 4 differential analog signals can be acquired through a choice of dual 12-bit analog-to-digital converters depending on the experimental requirements. Also, dual 12-bit digital-to-analog converters, three 16-bit programmable counter/timers, and a programmable 24-bit digital input/output lines enable the adaptor versatile in most computerized laboratory data acquisition and control instrumentations. The design principle and its applications are described.

Key Words: Data acquisition, computer application.

Introduction

Progress in computer industry revolutionized scientific laboratory.[1] Personal computers are moving into the laboratory and into the factory to act as data acquisition and industrial process control systems. The applications of the microcomputers in the laboratory include data acquisition, data analysis and signal processing, instrument control, and automated process monitoring. For real world applications of microcomputers an interfacing adapter, data acquisition and control adapter, is necessary. Although, microcomputers are available at low cost and the needs for a dedicated computer system for real world interfacing are increasing, commercially available data acquisition and control adapters are still expensive.

The open architecture of the IBM personal computers which use IBM standard bus system allowed many IBM compatible personal computers built around at low cost. Today, almost all IBM compatible personal computers in the market adapt the standard IBM bus, although the IBM uses their new microchannel bus system. We have developed a versatile data acquisition and control adapter for IBM or compatible personal computers using easily accessible components in the market at reasonable cost. It can be used with personal computers which have the IBM standard bus system.

In this paper, we describe the design principle of the versatile data acquisition and control adapter, and the software requirements for successful applications. Also, evaluation results with some applications of the adapter are discussed.

Experimental Section

Hardware Description

The block diagram of the data acquisition and control adapter is shown in *Fig*. 1. It consists of two parts, host and daughter boards. The host board occupies one expansion slot of the computer and is connected to the daughter board through a 50 pin ribbon cable for real world interfacing. The major components of the host board are 12-bit dual analog-to-digital converters (ADCs), 12-bit dual digital-to-analog converters (DACs), three 16-bit programmable counter/timers, and 24-bit digital input/output (I/O) lines (*Table* 1). The daughter board consists of a programmable gain instrumentation amplifier with a 4 channel multiplexer, 4 analog inputs, 2 analog outputs, 3 channel counter/timer I/O ports, and 24 digital I/O lines.

All the data and control signals are buffered using $\overline{IOR}$ from the expansion bus of the IBM-PC and the chip select signals from the onboard address decoder as shown in *Fig*. 2. Each device is assigned to a specific memory address by the memory mapped I/O design.[2] Addresses are decoded by two steps. Base address is switch selectable in the 200-3FF (hex) address range using a dip switch and a 74LS688 open collector output 8-bit comparator. Chip select signals are generated by decoding address lines A10-A12 and A0-A2 with $\overline{IOR}$ and $\overline{IOW}$ signals. Thus, a unique chip select signal can be selected by combining the base address and the offset address. These chip select signals are used to control the devices on the board.

Analog interfacing

The data acquisition and control adapter's analog I/O device consists of two systems. The ADC part for analog input and the DAC part for analog output. Two 12-bit resolution ADCs are used for analog input which are jumper selectable. For fast data input, an industry standard AD574[3] is used. The AD574 is a type of successive approximation ADC. The analog input signal is jumper selectable and can accept up to ±10V or ±20V signals. For low intensity signals and slow data input, an integrating type ADC, ICL7109[4] is used. The integrating type ADCs have better noise immunity

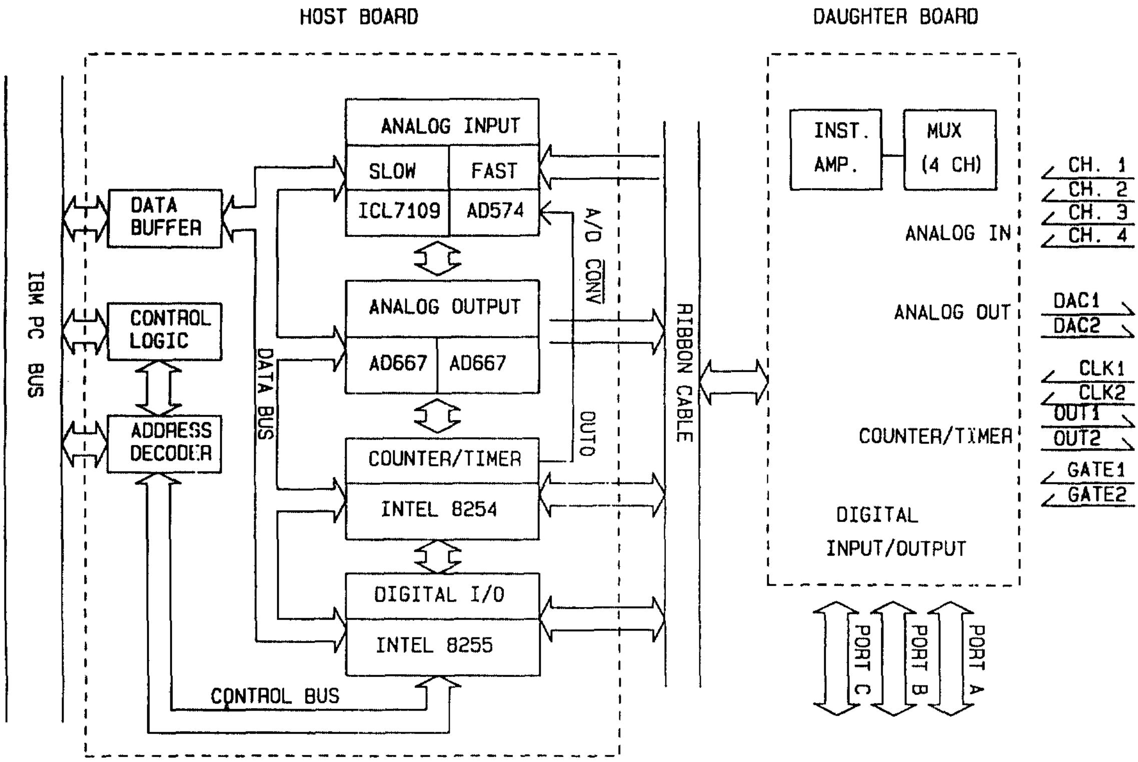

Figure 1. Block diagram of the data acquisition and control system.

Table 1. Major Components of the Data Acquisition Board

1. Analog-to-Digital Converter (12 bit)	4 Channel
A. Successive Approximation Fast ADC	AD574
Conversion time : 25 μs	
Input range : ±10V, ±20V	
B. Integrating Slow ADC	ICL7109
Conversion time : 20 ms	
Input range : ±0.5V, ±1.0V, ±2.5V, ±4.0V	
2. Digital-to-Analog Converter (12 bit)	AD667
No. of channels : 2 channel	
Conversion time : 10 μs	
3. Counter/timer	Intel 8254
No. of channels : 3 channel	
Internal clock rates : 1 Mhz	
4. Digital Input/output	Intel 8255
No. of ports : three 8-bit ports	
Programmable 24 digital I/O pins	
5. Signal Input Amplifier	AD524
Gain : 1, 10, 100, 1000 (pin programmable)	
Differential input instrumentation amplifier	

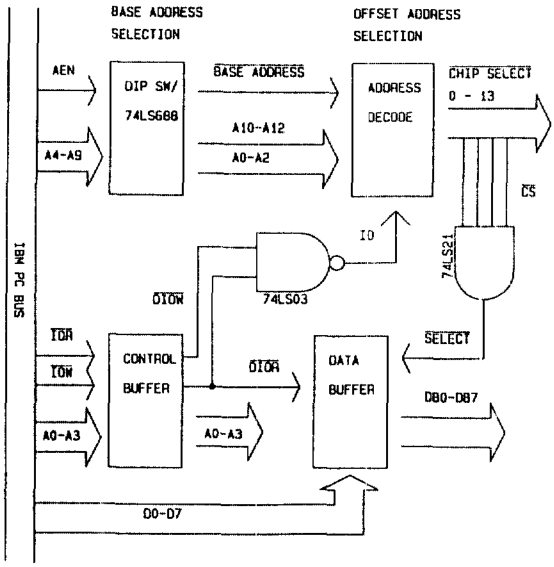

Figure 2. Simplified circuit diagram of the address decoding and control signals.

than the successive approximation type at the expense of speed.

The fast ADC, AD574, is configured as 12 bit data output and stand alone mode. Therefore, data conversion is controlled only by the state of the R/$\overline{W}$ signal and all 12 bits of data are latched when a conversion is complete. The status control circuit monitors A/D conversion status and checks data overrun or underrun. When data are overrun (multiple conversion/read) or underrun (multiple read/conversion) a flag is set to indicate invalid data. The conversion of ADCs can be triggered either by software or hardware. The hardware trigger sources, which are jumper selectable, can be either an onboard counter/timer output or an external pulses as shown in *Fig*. 3.

The maximum conversion times of the AD574 and

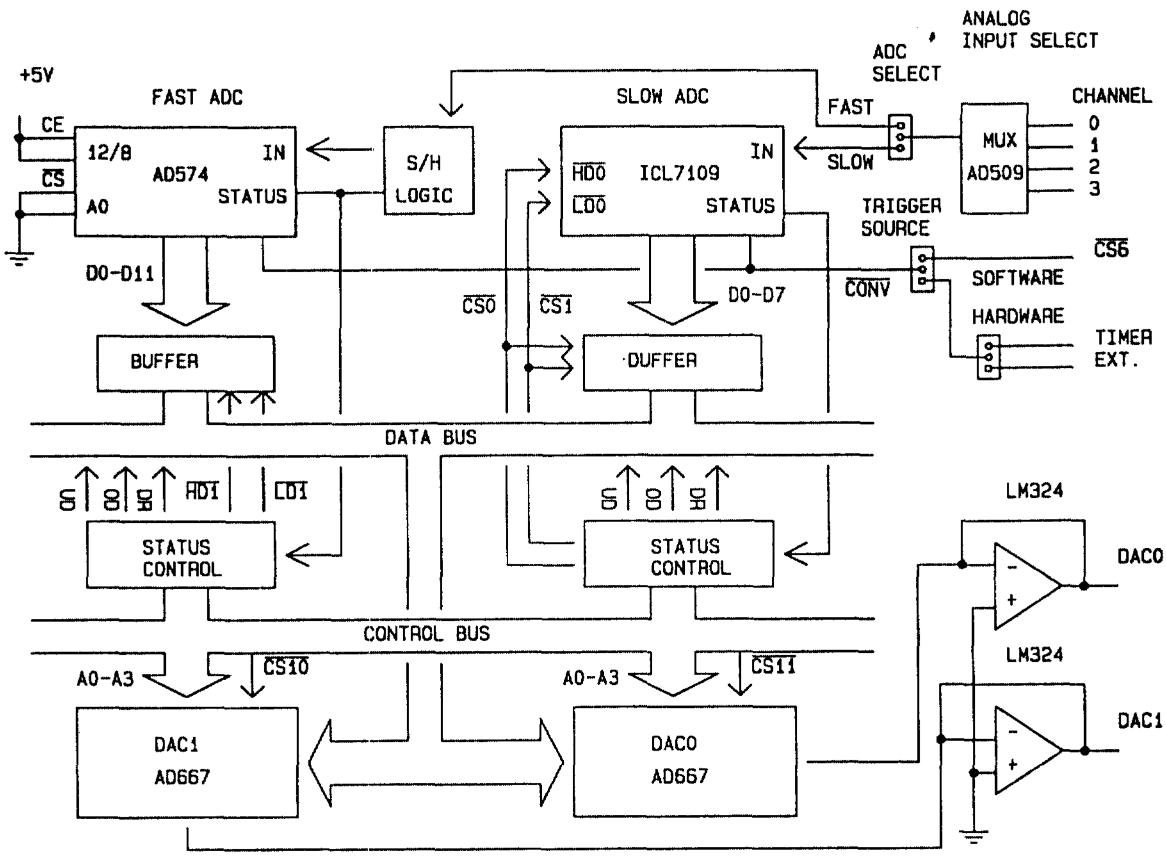

Figure 3. Block diagram of the analog interfacing circuit.

ICL7109 are 25 us and 20 ms, respectively. An mA at 1.5V. The individual bits of the three ports can sink 1.7 mA when in output mode and all digital 24 I/O lines are available on the daughter.

Software Description

In order to explore the detail functions of the data acquisition and control board, the board must be configured properly by placing jumpers. To access various devices on the board, the addresses of chip select signals must be set by determining the base address. A unique device address is obtained by adding the fixed offset address to the jumper selectable base address. The 12 bit data from the ADCs and to the DACs must be treated as two separate bytes, The data format of the slow ADC and the two DACs is right justified format (D0-D7 and D8-D11) and that of the fast ADC is left justified format(D0-D3 and D4-D11). A complete 12 bit datum is obtained by combining the two bytes. The unique status monitoring circuit of the ADCs prevent inputting the invalid data. This is accomplished by checking overrun or underrun flags before data read.

Results and Discussion

The primary output of any experiment in which chemical information is to be extracted, is the signal which measures the phenomenon under observation. In most cases, the signal measured has some superimposed noise which arises from various sources. Noise can be distinguished from the signal by its frequency characteristics and by the time of occurrence of phase coherence of their frequency component. Noise can not be eliminated completely, but it can be reduced either by hardware or software filtering.[6]

The most important thing when measuring signals with computerized data acquisition system is the proper shielding of the signal from noise sources. The noise sources include radio frequency interferences, other instruments operating near by, magnetic fields, and even improperly connected ground wires and shielding.[7] The hardware passive filtering is the easiest one to try when the speed and the time constant are not critical. One of the advantage of instrumentation amplifier (AD524) on the daughter board allows the user to change signal gains by setting jumpers. Also, a multiplexer (ADG509A) can accept up to 4 differential analog input signals for ADCs. For analog output, we used two 12-bit resolution DACs (AD667). The DACs with buffer amplifiers at the end can output analog signals in 10 μs and can be accessed separately. Since the data bus is 8 bit wide, the data from ADCs and to DACs must be treated in two read or write cycles to carry low and high byte of the data separately.

Counter/timer and digital I/O

Counter/timers are indispensable in modern data acquisition and control systems. Generation of pulses at regular time intervals, counting external events, complex waveform generation, and the measurement of accurate timing are the major functions of the counter/timers. We used a programmable counter/timer, Intel 8254[5], which is very popular in IBM personable computers. The first channel of the counter/timer is dedicated to the ADC for hardware triggered conversion. The rest two channels are available on the daughter board for user configuration. By writing a control word to the control port of the counter/timer with a combination of gate inputs, the counter/timer can operate in various modes.

For digital I/O we used a programmable peripheral interface chip, Intel 8255. The Intel 8255 is a general purpose programmable digital I/O device designed for implementing a variety of parallel port configuration. It has 24 I/O lines which may be individually programmed in two groups of 12-bit ports and used in 3 major modes of operation. The 8255 contains three 8 bit ports. The port A has data input latch and port B can source 1 the computerized data acquisition is the fast data acquisition rate and the obtained data can be stored in digital form for later manipulation.

Noise can be reduced in semi-real time by signal averaging. Multiple measurements of the signal and taking the average the signal-to-noise ratio can be increased by the square root of the number of measurements. With an optimized assembly code, up to 30,000 data can be acquired using the fast ADC, AD574. With the slow ADC, ICL7109, maximum 40 data/sec rate is possible. The accuracy and nonlinearity of the ADCs are adjustable to 0.05% full scale but no better than ±1 LSB (the least significant bit) because the ADCs have their own nonlinearity error ±1 LSB. The performances of the ADC and DAC are shown in *Fig*. 4. The first DAC and the slow ADC are configured to +5V and +4V full scale, respectively. The output of the DAC is digitized by the slow ADC as increasing the DAC data bits every second. Although, the DAC and ADC data are not the same due to their different full scale, it showed a linear increase in the full scale range.

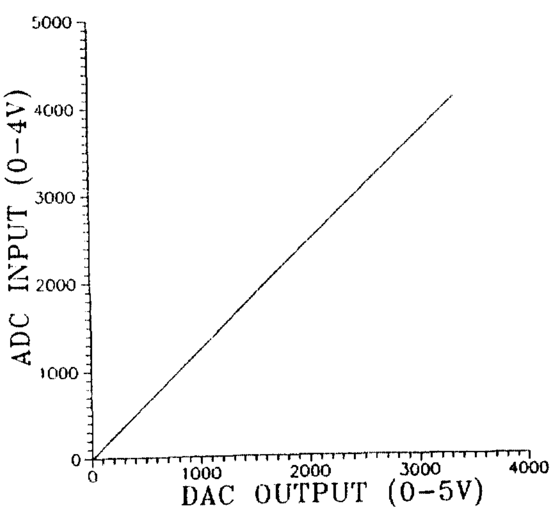

Figure 4. A plot of the DAC output *vs* ADC input. The DAC and the slow ADC are configured to +5V and +4V full scale, respectively. The unit of the ADC and DAC data are 12 bit binary values.

The applications of the data acquisition and control adaptor developed are munerous. The ADCs can be used to record signals of various analytical instruments. Also, the DACs output can be used to control various instruments which require precise and accurate analog signals. The programmable counter/timer may generate complicated timing waveforms or count external events during experiment. The digital I/O lines can be used for parallel data transfer between instruments and computer. The data acquisition and control adaptor with a low cost computer may perform convenient but powerful task without sacrificing time and money.

Conclusions

A versatile data acquisition and control adaptor for IBM personal computers has been developed. The data acquisition and control adaptor developed contains major components necessary for computerized data acquisition and control instrumentations. The analog signals can be digitized at the maximum speed of 40 kHz and the dual ADC design allows the user to choose the proper ADC, either sucessive approximation or integrating type, depending on the experimental requirements. Also, the data acquisition and control adaptor has two DACs, three 16-bit programmable counter/timers, and a 24-bit programmable digital input/output lines to aid the computerized experiments versatile. The data acquisition and control adaptor runs on an IBM-PC or low cost compatible personal computers. It was designed for the computerized experiments which require accurate analog input/output, real-time instrument control, automatic process monitoring and control.

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