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A Resolver-to-Digital Converter Using a Bang-Bang Type Phase Comparator

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Abstract - In this paper, we propose a new resolver-to-digital(R/D) conversion method, in which a bang-bang type phase comparator is employed for fast tracking. We eliminate from the R/D conversion loop the low-pass filter which is needed to reject carrier signal and noise. Instead, we employ two prefilters outside the R/D conversion loop that take the role of the low-pass filter. Thereby, we can construct a fast and accurate tracking R/D converter. Some simulation and experimental results as well as mathematical performance analysis are presented to demonstrate the superior tracking performance of our R/D converter over conventional tracking R/D converters.

Key Words : bang-bang type phase conpaator

Nomenclature

θ : resolver shaft angle
ϕ : digital angular position output
e : tracking error($\theta-\phi$)
V : amplitude of resolver format signal
A : integrator gain
B : (bang-bang type) phase comparator gain
ω : frequency of carrier signal
a_i : coefficients of bandstop filter
b_i : coefficients of 3rd order low-pass filter
c_i : coefficients of phase lead/lag circuit
a, b, c : coefficients of loop filter in RDC 19200-304
V_{s1}, V_{s2} : resolver format signals
η : internal noise
ζ : additive noise to input
K : error signal gain

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Ⅰ. Introduction

Resolvers are transducers used to sense the angular position of rotational machines. They resemble small motors and have magnetically coupled rotor and stator windings. Operation of tracking resolver-to-digital(R/D) converters is based on the resolver format signals induced on the stator windings of the resolvers.

It has been known that tracking R/D conversion is a most robust method for obtaining high resolution information from the resolver format signals. The tracking performance of tracking R/D converters depends mainly on the dynamic, and not static, characteristics of resolvers and R/D conversion loops. In this paper, we assume that the nonideal characteristics of resolvers have been properly compensated and we attempt to improve the dynamic characteristics of R/D conversion loops. The results presented in [6, 7, 8] treat the problems associated with the nonideal characteristics of resolvers.

The prior works closely related to ours can be found in [1, 2, 11]. These papers concern phase-locked loop(PLL) but not R/D converters. However, the operation of tracking R/D converters is exactly the same as that of PLL's in synchronous mode. Ahmed and Wong[2] show that the optimum nonlinear device used in the feedback path of the PLL, which attains synchronization in the shortest possible time, is the on-off device. In [2], however, the dynamics of low-pass filter located in the PLL are assumed to be fast enough to be neglected. Ahmed and Aboud[1] consider the practical situation where the dynamics of the low-pass filter are significant and show that the optimal solution is to place a polynomial type of static nonlinearity with finite power between the low-pass filter and the VCO. Williamson[11] proposed the nonlinear loop filter that can enhance acquisition performance without significant degradation due to the effects of noise.

The results on PLL in[1, 2, 11] can provide fast tracking performance but cannot guarantee zero steady state tracking error, and thus cannot be directly used for tracking R/D conversion. In the method proposed in [2], the time lag due to the dynamics of the low-pass filter causes limit cycles in the output signal even when the low-pass filter is a brickwall ideal low-pass filter. The schemes proposed in [1, 11] are basically the Type I systems and produce constant tracking error for a ramp input.

Our tracking R/D converter adopts the on-off device considered first in [2] as the phase comparator. However, we eliminate from the R/D conversion loop the low-pass filter which was needed [1, 2, 11] to reject carrier signal and noise. We employ, instead, two prefilters outside the R/D conversion loop that take the role of the low-pass filter. We can, thereby, eliminate the source of limit cycles in the output and construct a fast and accurate tracking R/D converter.

Since our tracking R/D converter attains the ideal situation considered in [2], it can provide fast tracking. We prove, via Lyapunov's direct method, that the tracking error converges to zero if the input rate does not exceed the converter maximum tracking rate specified by the physical limitation such as the saturation voltage of op amps. We propose the design of the two prefilters and a method of reducing the effect of noise on tracking accuracy. In order to demonstrate the practical use of our conversion method, we also present some experimental results that show the superior tracking performance over the conventional tracking R/D converters.

Ⅱ. New Resolver-to-Digital Conversion Scheme

We first describe at some length the tracking operation of a widely used conventional tracking R/D converter. Suppose that the current angular position of the resolver is at angle θ. Then, the resolver format signals induced on the secondary windings of an ideal resolver will be

$$V_{s1} = V\sin\theta\cos\omega t$$
$$V_{s2} = V\cos\theta\cos\omega t \qquad (1)$$

if the primary winding is excited with an AC reference signal $V\cos\omega t$.

As can be seen from Fig. 1, these resolver format signals V_{s1} and V_{s2} are multiplied by cosine and

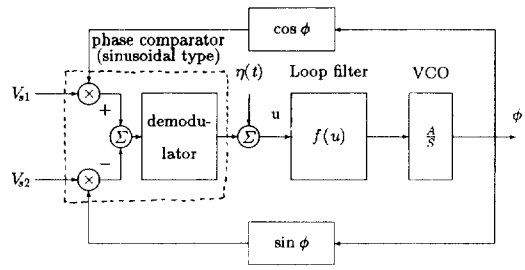

Fig. 1 Block diagram of a conventional tracking R/D converter, where $u \triangleq K\sin(\theta-\phi)-\eta(t)$.

sine of the current state of the up/down counter, respectively. Subtraction of the resulting signals gives the modulated error signal $V\sin(\theta-\phi)\cos\omega t$. This signal is then demodulated by the phase sensitive detector which utilizes the AC reference signal $V\cos\omega t$. An analog DC error signal is therefore produced, which is proportional to $\sin(\theta-\phi)$. This DC error signal is delivered through a loop filter to the VCO. The VCO internally consists of an analog integrator and an up/down counter. The analog integrator outputs a pulse to the up/down counter when the integrated value reaches a specified quantity and then the integrator is reset. It is clear from the above discussion that the integrator in the VCO outputs pulses to the up/down counter until the final state of the up/down counter equals to the resolver shaft angle, i.e. $\phi=\theta$. [3, 9]

In the situation when the tracking error is small, the DC error signal is positively proportional to the tracking error since $\sin e \cong \frac{2}{\pi}e$ if $|e|<\frac{\pi}{2}$. However, in the case of large tracking error, the DC error signal becomes negatively proportional to the tracking error since $\sin e \cong -\frac{2}{\pi}(e-\pi\mathrm{sgn}(e))$ if $\frac{\pi}{2}<|e|\leq\pi$. Therefore, the nonlinear characteristics of the sinusoidal phase comparator result in poor tracking performance in the case of large initial tracking error.

In the PLL schemes proposed in [1, 11], the loop filter in Fig. 1 consists of a low-pass filter and a polynomial type of static nonlinearity with finite power. As the result, these schemes have the dynamic characteristics of a Type I system and cannot exactly track even a ramp input signal. In most of conventional tracking R/D converters(for instance, see[3, 9], the loop filter in Fig. 1 has the form:

$$\text{Linear loop filter: } \mathcal{L}[f(u)]=\frac{c(bs+1)}{s(as+1)}$$

Therefore, the conventional tracking R/D converters are the Type II systems and hence can track a ramp input exactly but with poor transient performance due to the integral action of the linear loop filter.

To overcome such drawbacks of the conventional tracking R/D converters and the PLL schemes, we eliminate the demodulator and the loop filter from the R/D conversion loop and instead adopt a bang-bang type phase comparator as is shown in Fig. 2. The rejection of the carrier signal and the noise, usually of high frequency, is performed by two prefilters, each of which consists of a demodulator and a linear filter. Such a R/D conversion method has two important advantages over the previous methods.

First, this approach allows for digital implementation of the conversion loop. That is, the VCO can be implemented by digital circuits since the output of the bang-bang type phase comparator has only two states. The resulting digital VCO has excellent performance in linearity and furthermore makes the conversion loop more insensitive to the environmental disturbances such as humidity, temperature, drifts or offsets of op amps.

Second, this approach provides good tracking performance. As will be shown soon, we can prove under some reasonable assumptions that the new tracking R/D converter always drives the tracking error to zero if the input rate does not exceed its maximum tracking rate(AB in Fig. 2).

Now, we present the mathematical performance analysis of our converter. For the simplicity of performance analysis, we make two ideal assumptions:

(A1) two prefilters are identical and produce negligible time lags,

(A2) there exists no noise, i.e. $\eta=0$.

Under these ideal assumptions, the R/D con-

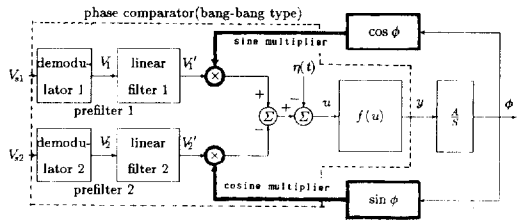

Fig. 2 Block diagram representation of the new tracking R/D converter, where $f(u)\triangleq B\,\mathrm{sgn}(u)$ and $u\triangleq K\sin(\theta-\phi)-\eta(t)$.

verter in Fig. 2 can be simplified to the one in Fig. 3 and can be described by the following simple equation.

$$\dot{\phi}=Af(u),\quad u=K\sin(\theta-\phi), \tag{2}$$

where

$$f(u)\triangleq B\,\mathrm{sgn}(u) \tag{3}$$

The signum function in (3) is a discontinuous device and can be approximated by a continuous device,

$$f(u)\triangleq\begin{cases}\dfrac{Bu}{\sin\delta} & \text{if } |u|\le\sin\delta\\ B\,\mathrm{sgn}(u) & \text{if } |u|\ge\sin\delta\end{cases} \tag{4}$$

which is well known as the saturation function. Our performance analysis is performed only on the continuous system given by (2) and (4) since the saturation function in (4) approaches the signum function in (2) and (3) as δ tends to zero.

Finally, we assume that

(A3) $\mu\triangleq AB-\sup_{t\ge0}|\dot{\theta}(t)|>0$

This condition simply requires that the input rate must not exceed the product of the phase comparator gain and the integrator gain. This is quite a natural requirement since $\sup_{t\ge0}|\dot{\phi}|=AB$. Now, we are in order to state Theorem 1.

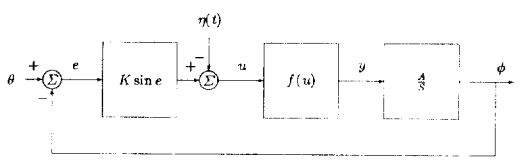

Fig. 3 Equivalent representation of the new tracking R/D converter with ideal prefilters, where $f(u)\triangleq B\,\mathrm{sgn}(u)$.

Theorem 1. (Zero Tracking Error Theorem) Suppose that (A1)-(A3) hold for the new tracking R/D converter shown in Fig. 2. Then, the tracking error is "ultimately bounded," so that

$$|e(t)|\le\epsilon+\sin^{-1}\left(\frac{\sin\delta}{K}\right),\quad t\ge T(\epsilon,\ e(t_0))+t_0 \tag{5}$$

for any ϵ such that

$$0<\epsilon<\pi-2\sin^{-1}\left(\frac{\sin\delta}{K}\right) \tag{6}$$

where

$$T(\epsilon,\ \delta,\ e(t_0))\triangleq$$

$$\begin{cases}0 & \text{if } |e(t_0)|\le\epsilon+\sin^{-1}\left(\dfrac{\sin\delta}{K}\right)\\ \left(\dfrac{2}{\mu}\right)\ln\left[\dfrac{1-\cos\left(\dfrac{e(t_0)}{2}\right)}{1-\cos\dfrac{\epsilon+\sin^{-1}\left(\dfrac{\sin\delta}{K}\right)}{2}}\right] & \\ \text{if } \epsilon+\sin^{-1}\left(\dfrac{\sin\delta}{K}\right)<|e(t_0)|<\pi-\sin^{-1}\left(\dfrac{\sin\delta}{K}\right)\end{cases}$$

Proof of Theorem 1 See (e.g., [12])

The above theorem states that, if (A3) is satisfied, the tracking error is kept smaller than "the ultimate bound" $\epsilon+\sin^{-1}\left(\frac{\sin\delta}{K}\right)$ after a finite time T depending on the positive constants ϵ, δ and the initial tracking error $e(t_0)$. Note that the choice of ϵ and δ is completely free. Therefore, we can make the ultimate bound of the tracking error as small as possible by reducing the linear region of the saturation function in (4) and, if (A3) is satisfied, then our tracking R/D converter in Fig. 2 or Fig. 3 assures that

(B1) $\lim_{t\to\infty}|e(t)|=0$ if $|e(t_0)|<\pi$,

(B2) for any ϵ such that $0\le\epsilon<\pi$, $|e(t)|\le\epsilon$, $t\ge t_0$ if $|e(t_0)|\le\epsilon$.

Finally, we discuss at some length the prior works closely related to ours. As mentioned earlier, the bang-bang type phase comparator and its continuous approximation were first considered by Ahmed and Wong [2]. They placed these nonlinear devices between the brickwall ideal low-pass filter and the VCO. Under the assumption that the dynamics of the brickwall ideal low-pass filter are fast enough to be neglected, they showed

that these nonlinear devices minimize exactly or approximately the first time to acquire lock-in.

However, the dynamics of the low-pass filter can not be, in practice, neglected since the filter has to reject the carrier signal and noise. In fact, the responses of their PLL scheme can involve limit cycles or steady state error due to the dynamics of the low-pass filter. Recall that, in our new R/D conversion method, the low-pass filter is removed from the R/D converter does not have such a drawback. Furthermore, our Theorem 1 assures that the tracking error always converges to zero if the input rate satisfies (A3). Of course, two prefilters must not produce significant distortion and time lag in the input signals. The compensation method to resolve this problem is presented in[12].

Ⅲ. Design of Asymptotically Ideal Prefiler

In order for the new tracking R/D converter proposed in Section Ⅱ to have the desired performance stated in Theorem 1, the two prefilters must not cause significant time lag in the input signal but have to reject effectively the carrier signal and the noise. Furthermore, the gains of two prefilters are required to be identical. To meet such requirements for prefilters, we propose the linear filter which consists of three bandstop filters, one low-pass filter, and one phase lead/lag compensator.

Bandstop filter :

$$G_1(s)=\frac{s^3+a_1s^2+a_2s+a_3}{s^3+a_4s^2+a_5s+a_3}$$

Low-pass filter :

$$G_2(s)=\frac{1}{b_1s^3+b_2s^2+b_3s+1}$$

Phase lead/lag compensator :

$$G(s)=\frac{c_1s^2+c_2s+1}{c_3s^2+c_4s+1}$$

The three bandstop filters are used to eliminate the carrier signal. The bandstop frequency of each bandstop filter is chosen to be twice that of the carrier signal. The low-pass filter is used to reject the noise and the phase lead/lag compensator is required to compensate for the time lag of the input signal caused by the bandstop filters and the low-pass filter. As will be seen from the simulation and experimental results in Seciton Ⅳ, the prefilters designed as above meet all requirements for prefilters and hence assure that our R/D converter has the properties stated in Theorem 1.

Ⅳ. Simulation and Experimentation

In this section, we investigate through simulation and experimentation the practical use of the methods developed in the previous sections. In simulation and experimentation, we compare the tracking performance of our new converter with that of a conventional R/D converter which is popularly used in industries. The data used for simulation and experimentation are listed in Table Ⅰ. The numerical values of A, a, b, and c represent the data of the typical conventional tracking R/D converter RDC 19200-304 manufactured by

Table 1 Data used in simulation and experimentation

coefficients of bandstop filter	a_1	44642.96
	a_2	9.96492E8
	a_3	8.93E13
	a_4	223214.0
	a_5	9.9649E9
coefficients of low-pass filter	b_1	1.794E-13
	b_2	3.18E-9
	b_3	1.392E-4
coefficients of phase lead/lag circuir	c_1	8.454E-8
	c_2	4.95E-4
	c_3	1.0292E-9
	c_4	5.56E-5
integrator gain	A	125.8
phase comparator gain	B	9.99
frequency of carrier signal	ω	18850
coefficients of loop filter in RDC 19200-304	a	1.6667E-4
	b	1.6667E-3
	c	17.5

DDC Co.

In the simulation results shown in Fig. 4, the input signal was chosen as a triangular wave with the period 7.04msec and the amplitude 0.943 radian. Note that this input signal satisfies the condition (A3) in Section Ⅱ since $\sup_{t\geq 0}|\dot{\theta}(t)|=$ 535.8rad/sec. When the asymptotically ideal prefilters are used, the output response of our R/D converter tracks the input signal exactly and hence is overlapped with the input signal.

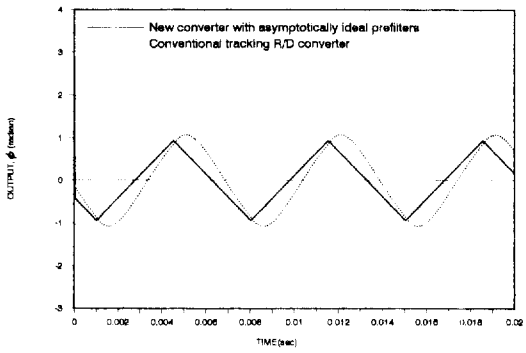

Fig. 4 Simulation results for the triangular input.

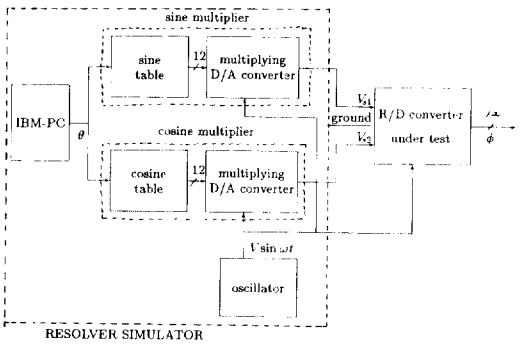

Fig. 5 Schematic diagram of experimental system.

For our experimental study, we have constructed a prototype of our new converter with asymptotically ideal prefilters. For a fair comparison, it was designed to have a resolution of 12 bits per revolution and a maximum tracking rate of 200rps(which corresponds to $AB=1256.64$rad/sec, here), just as the RDC 19200-304.

Fig. 5 shows the schematic diagram of experimental system. As the tracking R/D converter receives the resolver format signals, we need resolver simulator which produces the resolver format signals. Resolver simulator is so called the digital-to-resolver converter. As shown in Fig. 5, resolver simulator provides a 3 wire resolver format signals(V_{s1}, V_{s2}, and ground). The sine/cosine multipliers which consist of sine/cosine tables and multiplying D/A converters take digital inputs from IBM-PC in parellel binary form representing the angle θ and produce outputs in resolver format at any standard frequency ω and voltages V.

Fig. 6 shows the block diagram of the implemented R/D converter. Detailed descriptions of prefilter design are given in Section Ⅲ. The construction of sine/cosine multipliers is the same as that of resolver simulator and is shown in Fig. 5. Subtracting amplifier with gain K' generates error signal u by subtracting cosine multiplier output from sine multiplier output. Therefore, we obtain a clear description of error signal as

$$u=K'V\sin(\theta-\phi)$$

In Section Ⅱ, Ⅳ, we denoted $K'V$ as error signal gain K. So we can easily increase the error signal gain K by simply increasing the subtracting amplifier gain K' without increasing the resolver

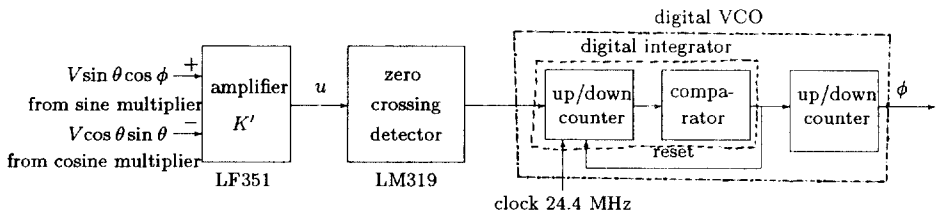

Fig. 6 Block diagram of implemented R/D converter.

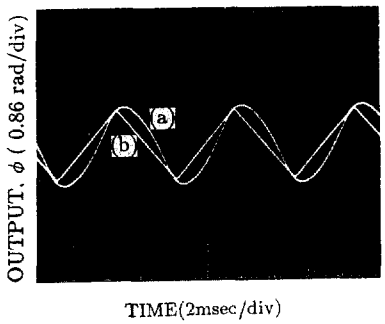

Fig. 7 Experimental results for the triangular input ((a) conventional converter, (b) new converter with asymptotically ideal prefilters)

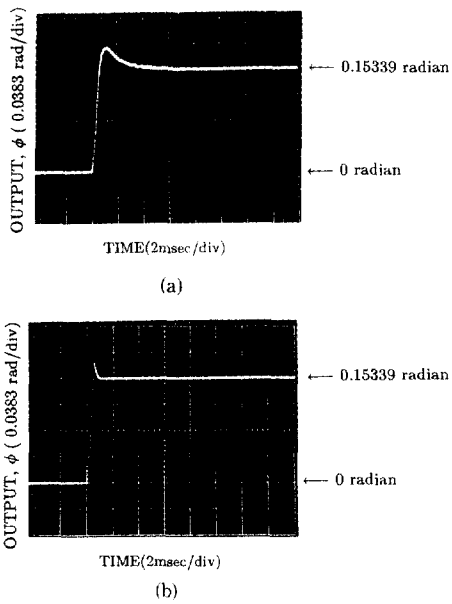

Fig. 8 Experimental results for the 0.15339 radian(100LSB) step input((a) conventional converter, (b) new converter with asymptotically ideal prefilters)

format signal gain V. Zero crossing detector needs simple comparating circuits but needs careful choice of comparator which should have fast comparating performance. In the prototype of our R/D converter, high speed comparator, LM 319 is chosen, Digital VCO can be easily implemented with only digital circuits. The clock frequency of the first up/down counter determines the VCO

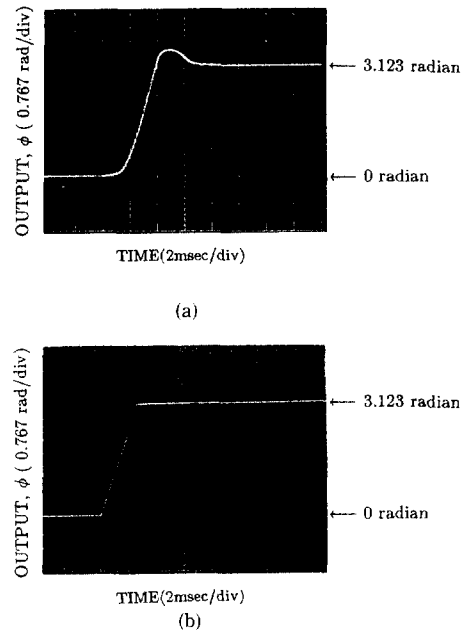

Fig. 9 Experimental results for the 3.123radian (2036LSB) step input((a) conventional converter, (b) new converter with asymptotically ideal prefilters)

gain and the number of bits in the second up/down counter is the resolution of R/D converter. A detailed description of the operation of VCO is given in Section Ⅱ.

In the first experiment, the input signal was chosen to be the same triangular wave as was used in the simulation. The output responses of our new R/D converter with the asymptotically ideal prefilters and the conventional R/D converter RDC 19200-304 are drawn in Fig. 7. The experimental result in Fig. 7 is a good match with the simulation result in Fig. 4 and exhibits the superior tracking performance of our converter over the conventional converter. In the second experiment, the input signal was chosen as the step input. The output responses of the conventional converter and our converter with asymptotically ideal prefilters for small and large step inputs are shown in Fig. 8 and 9, respectively. From Fig. 8 and 9, we observe that the settling time of our new converter is a factor of 6 shorter than that of the conventional converter. In both experiments, we checked through use of a logic analyzer that the tracking

error of our converter was kept within 1 LSB.

Finally, we discuss the effects of noise on tracking performance of our new converter. The noise which can affect the tracking performance can be divided into kinds. One is the high frequency noise which accompanies the input signal and the other is the internal noise which is independent of the input signal. The high frequency noise accompanying the input signal can be effectively eliminated by the prefilters proposed in the preceeding sections.

The internal noise which is independent of the input, however, is added directly to the error signal and cannot be prefiltered. This noise is denoted by η as is shown in Fig. 2 and 3. To investigate the effect of this internal noise on the output, we choose a rectangular wave input signal with period 6.5msec and amplitude 0.0153radian (10 LSB). From the experimental result in Fig. 10(a), we see that when $K=150$ the tracking error exceeds 1 LSB due to the internal noise. However, the experimental result in Fig. 10(b) shows that, by simply increasing the error signal gain K sufficiently, we can reduce the effect of the internal noise on the output to less than 1 LSB. This can be explained as follows.

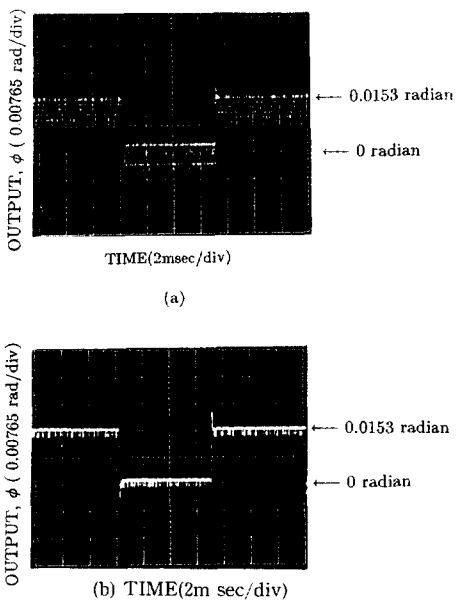

Fig. 10 Output responses of the new R/D converter for the rectangular input when (a) $K=150$ and (b) $K=780$

If we include the noise term in the equations (2) and (3), we have

$$\dot{\phi}=AB\text{sgn}[K\sin(\theta-\phi)-\eta(t)] \tag{7}$$

Let $\bar{\eta}$ be the function of time such that

$$\sin(e-\bar{\eta})=\sin e-\frac{\eta}{K} \tag{8}$$

If K is large and e is small, the equation (8) uniquely determines $\bar{\eta}$ for each e and η and furthermore $\bar{\theta}=\theta-\bar{\eta}$ satisfies the assumption (A3). By (8), we can write (7) as

$$\dot{\phi}=AB\text{sgn}[K\sin(\bar{\theta}-\phi)] \tag{7}'$$

By (7)' and the property (B1), we have $|\phi-\bar{\theta}| \to 0$ as $t\to\infty$. This with (8) assures that

$$|\sin e-\frac{\eta}{K}| \to 0 \text{ as } t\to\infty \tag{9}$$

Consequently, if $|\eta(t)|<N$, $t\geq 0$ and K is large, there will be a finite time $t_0>0$ such that

$$|e(t)|\leq\sin^{-1}\left(\frac{N}{K}\right),\ t\geq t_0 \tag{10}$$

Note from Theorem 1 that, in the case of our converter, excessive increase in the error signal gain K does not degrade tracking performance. Therefore, the error signal gain K can be increased freely for the reduction of the effects of noise. However, in other PLL or R/D converters which use linear loop filters, very large error signal gain may reduce the effects of noise significantly but may result in oscillatory or unstable output responses.

V. Conclusions

Through mathematical performance analysis, simulation, and experimentation, we have shown that the proposed R/D converter can track any arbitrary input quickly and precisely as long as the input rate does not excceed its maximum tracking rate AB and has superior tracking performance over conventional converters. The analysis on the effect of noise shows that the position error due to noise can be reduced to less than 1 LSB by increasing the error signal gain K sufficiently

large without deteriorating tracking performance. For the industrial use of our new converter, however, we have to add some circuits which can automatically control the offsets and drifts of op amps and multipliers. We also need to build a hysteresis type threshold into the conversion loop in order to eliminate the jitter around the null (zero-error) point, due primarily to quantizing noise.

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