論 文
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저전압 VDMOS의 ON-저항 모델

An Advanced Model of on-Resistance for Low Voltage VDMOS Devices

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Abstract - An advanced on-resistance model of VDMOS devices in the low voltage regimes is proposed and verified by 2-D device simulations. The model considers the lateral gaussian doping profiles in the channel region and exact current spreading angles in the epitaxial layer for both linear and cellular geometries by employing the conformal mapping, It is found out that the on-resistance of low voltage VDMOS may be overestimated considerably if it is analyzed by the conventional method. The 2-D device simulation results show that the proposed model is valid for the VDMOS devices in the low voltage regimes.

1. Introduction

Low voltage power MOSFETs, of which the breakdown voltage is usually less than 100Volts, are widely used in various power electronic circuits such as switch mode power suppy and electronic ballasts. Although, the switching speed, thermal stability, driving circuits, and input resistance of power MOSFET are fairly better than those of bipolar power transistors, the minimization of the relatively large on-resistance of power MOSFETs has been a considerable problem to designers. However, the on-resistance modeling in low voltage power MOSFET has not been well established yet. The purpose of this work is to present an accurate analytical model of on-resistance in the low voltag VDMOS.

The on-resistance of VDMOS devices has been generally analyzed by means of four components models[1, 2] : channel resistance, accumulation resistance, JFET resistance, and bulk epi-layer resistance. One of these models reported by Hu group [2] is widely used because it is simple, can be applicable to all cell geometries, and agrees quite well with experimental results in high voltage regime. However, this model may not be suitable for the low voltage VDMOS. It has assumed the uniform doping profiles in the channel region

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and has not considered the two dimensional nature of current flows in the accumulation and JFET region under the gate electrode. Furthermore, this model has assumed the fixed spreading angle of current flows in the epitaxial region as a constant 45 degrees for degrees for all cell geometries. Those simplifications may be fairly acceptable in the high voltage VDMOS, of which the on-resistance is dominated by lightly doped expitaxial layer, but may induce considerable errors in the low voltage VDMOS, of which the on-resistnace is not dominated by epitaxial layer only[1]. In this work, a fairly accurate analytical model of on-resistance in the low voltage VDMOS is presented. The results of our model are verfied by 2-D device simulation in both high and low voltages regimes.

2. Analysis

The structure of VDMOS considered for the present analysis is shown in Fig. 1. The S and A are the width and the spacing of p body region, respectively. The lateral and vertical junction depths of n^+ region are denoted by x_s and t_s, those of p region by x_p and t_b, and thickness of n epi-layer by t_{epi} in Fig. 1

2.1 Channel Resistance

Starting from 2-D gaussian profiles, we evaluate the distributed channel resistance analytically by calculating channel length, peak concentration and its position, total concentrations, and inversion layer mobilites.

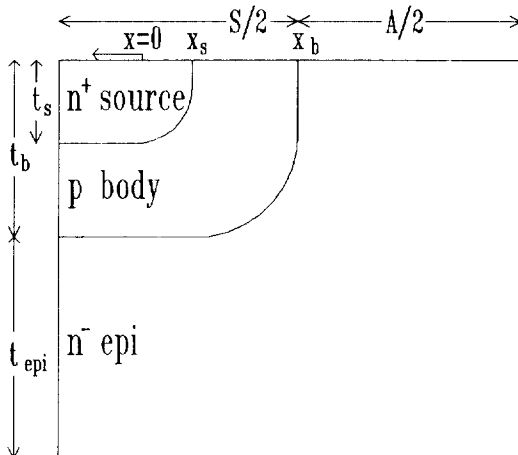

Fig. 1 crossectional view of the VDMOS structure

The doping profiles of double-diffused channel surface are taken as follows[3, 4].

$$N_{tot}(x)=\frac{N_s}{2}\exp\left[-\delta\left(-\frac{x}{\sqrt{4D_sT_s}}+\Delta\right)^2\right] \quad (1)$$
$$+\frac{N_b}{2}\exp\left[-\delta\left(-\frac{x}{\sqrt{4D_bT_b}}+\Delta\right)^2\right]-N_{epi}$$

where,

N_s : the maximum surface concentrations of diffused atoms in n^+ region

N_b : the maximum surface concentration of diffused atoms in p region

$\sqrt{D_sT_s}$: characteristic length associated with n^+ diffusion

$\sqrt{D_bT_b}$: characteristic length associated with p diffusion

N_{epi} : constant n epitaxial layer concentrations

Δ : 0.387[4]

δ : 0.935[4]

The lateral junction depths(x_s, x_b) and channel length(L) should be known in order to estimate the channel resistance, which can be derived as a function of both vertical junction depths (t_s, t_b) and process parameters(D_sT_s, D_bT_b).

$$x_s=\frac{1}{a}\left[b-\left[\frac{1}{\delta}\ln\frac{N_s}{N_b}+b^2\right]^{\frac{1}{2}}\right] \quad (2)$$

$$x_b=\sqrt{4D_bT_b}\left[\Delta-\left[\frac{1}{\delta}\ln\frac{N_b}{2N_{epi}}\right]^{\frac{1}{2}}\right] \quad (3)$$

$$L=x_s-x_b \quad (4)$$

where,

$$a=\left[\frac{1}{4D_sT_s}-\frac{1}{4D_bT_b}\right]^{\frac{1}{2}}$$

$$b=\Delta\frac{\sqrt{D_bT_b}-\sqrt{D_sT_s}}{\sqrt{D_bT_b-D_sT_s}}$$

$$D_bT_b=\frac{t_b^2}{4\ln\frac{N_b}{2N_{epi}}}$$

$$D_sT_s=\left[\frac{4}{t_s^2}\ln\frac{N_s}{N_b}+\frac{1}{D_bT_b}\right]^{-1}$$

The channel region is divided into small segments laterally (in this work, 100 segments) and each divided segment is considered to be uniformly

doped. The threshold voltage ($V_{th,t}$), inversion layer mobility ($\mu_{in,i}$), and resistance ($R_{ch,i}$) of i-th segment are calculated.

$$R_{ch,i}=\frac{L_i}{\phi_{ni,i}C_{ox}(V_g-V_{th,i})} \tag{5}$$

where,

$$V_{th,i}=\phi_{ms}-\frac{Q_f}{C_{ox}}+2\psi_{B,i}+\frac{\sqrt{4\varepsilon_s qN_{tot,i}\psi_{B,i}}}{C_{ox}} \tag{6}$$

$$\psi_{B,i}=\frac{kT}{q}\ln\frac{N_{tot,t}}{n_i}$$

$$\mu_{ni,i}=\mu_{\max,i}\left[\frac{E_{c,i}}{E_{eff,i}}\right]^{\beta_i} \tag{7}$$

$$E_{eff,i}=\frac{1}{2}\left[E_{ns}+\frac{\sqrt{4qN_{tot,i}\psi_{B,i}}}{\sqrt{\varepsilon_s}}\right]$$

where, n^+ polysilicon gate is assumed and $\mu_{\max,i}$, $E_{c,i}$ and β_i are the empirical parameters depending on the fixed oxide charge density Q_f and doping concentrations of i-th segment $N_{tot,i}$ [5]. The peak surface electric field E_{ns} is assumed to be constant ($3\times10^5\,V/\text{cm}$) in all segments.

Now, the channel resistance may be evaluated easily by the summation of resistance in each segment.

$$R_{ch}\cdot A=\frac{S+A}{2}\sum_{i=1}^{n}R_{ch,i}\quad[\Omega\cdot\text{cm}^2][\text{linear}] \tag{8}$$

$$=\frac{[S+A]^2}{4S}\sum_{i=1}^{n}R_{ch,i}[\Omega\cdot\text{cm}^2][\text{cellular}] \tag{9}$$

For the comparison with the four component model [1, 2] which assumes the channel region to be uniformly doped, the peak concentration and its position (denoted by x_{peak}) in channel region are also derived analytically.

$$x_{peak}=\left[\frac{4D_bT_bD_sT_s}{D_bT_b-D_sT_s}\ln\left[\frac{N_s}{N_b}\cdot\frac{\sqrt{D_bT_b}}{\sqrt{D_sT_s}}\right]\right]^{\frac{1}{2}} \tag{10}$$

The peak concentration can found from both eqs. (1) and (10).

2.2 Accumulation and JFET Resistance

The conventional model for accumulation and JFET resistnace has neglected the two dimensional nature of current flow under the gate electrode. Recently, the access resistance model, which is obtained analytically from the differential equation for the surface current distribution and agrees well with 2-D simulation and experimental results even for the lagre cell spacings, is reported[6]. This access resistance model is substituted in this work for the accumulation and JFET resistance model.

$$R_{acc}\cdot A=\frac{\beta\rho_{epi}t_1}{2}[S+A]\,cth\frac{\beta A}{2}\quad[\text{linear}] \tag{11}$$

$$=\beta\rho_{epi}t_1\frac{[S+A]^2}{4S}\frac{C_1K_0\left[\frac{\beta S}{2}\right]+I_0\left[\frac{\beta S}{2}\right]}{C_1K_1\left[\frac{\beta S}{2}\right]-I_1\left[\frac{\beta S}{2}\right]}\quad[\text{cellular}] \tag{12}$$

where,

$t_1=\max[t_b\sin45,\ \text{depletion width}]$

$\beta=\frac{\rho_s}{\rho_{epi}t_1}[\rho_s$: surface resistivity$]$

$C_1=I_1\left[\frac{\beta}{2}[S+A]\right]/K_1\left[\frac{\beta}{2}[S+A]\right]$

I_0, I_1, K_0, and K_1 : the Bessel's function

2.3 Epitaxial Layer Resistance

The epi-layer resistance has been estimated by use of the trapezoidal model [2] which assumes a constant current spreading angle α (generally 45 degrees) and calculates the resistance of resulatant trapezoidal area as shown in Fig. 2(a). However, various values of epi-layer thickness (t_{epi}), cell sizes (S), and cell spacings (A) may not allow α to be a constant.

In the case of linear cell geometry, it is possible to estimate an exact epi-layer resistance by conformal mapping which assumes that the accumulation layer is an equipotential. The region shown in Fig. 2(a) can be conformally mapped into the rectangular region shown in Fig. 2(b) by use of the Jacobian elliptic function [7]. It has been known that the results of trapezoidal model are within 5 percent of this exact solutions[2]. However, this error rate may be larger in the low voltage regimes and the cellular cell geometries have not been analyzed. In this work, these conformal mapping and trapezoidal model are applied simultaneously to estimate an exact epi-layer resistance of the cellular cell geometries as follows.

In cellular cell geometries, a central crossection is the same as one shown in Fig. 2(a). The conformally mapped resistance (denoted by R_{epi1}) and the trapezoidal area resistance (denoted by R_{epi2}) are given as follows.

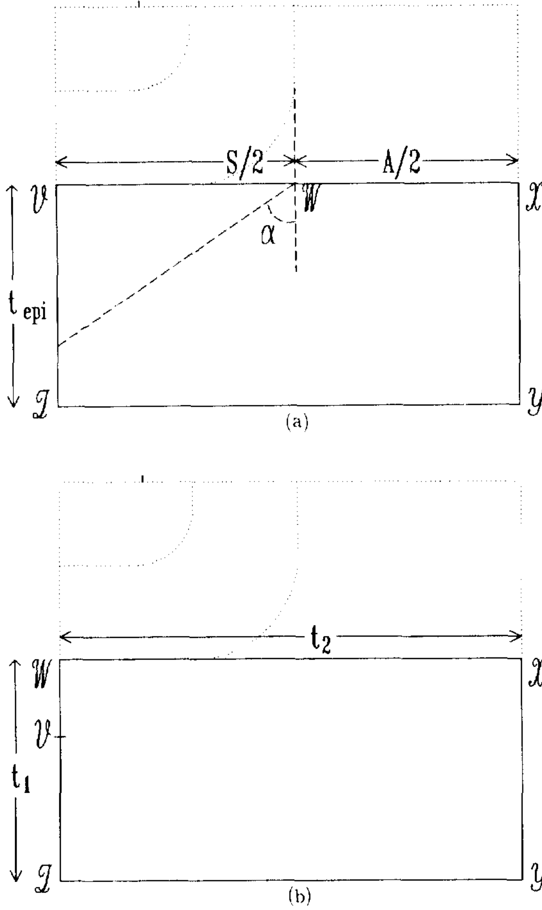

Fig. 2 crossectional view of the VDMOS structure for conformal mapping
(a) trapezoidal model
(b) conformal mapping

$$R_{epi1}=\frac{\rho_{epi}}{Z}\frac{t_1}{t_2} \tag{13}$$

$$R_{epi2}=\frac{\rho_{epi}}{Z2\tan\alpha}Ln\left[1+\frac{2t_{epi}\tan\alpha}{A}\right],\quad \tan\alpha\leq\frac{S}{2t_{epi}} \tag{14}$$

$$=\frac{\rho_{epi}}{Z2\tan\alpha}\left[Ln\left[1+\frac{S}{A}\right]+\frac{2t_{epi}\tan\alpha-S}{S+A}\right],\quad \tan\alpha\geq\frac{S}{2t_{epi}} \tag{15}$$

The current spreading angle may be found by equating the conformally mapped resistance and the trapezoidal area resistance : ($R_{epi1}=R_{epi2}$).

After finding α as a function of t_{epi}, S, and A, the epi-layer resistance of cellular cell geometries can be evaluated by simple integration as follows.

$$R_{epi}\cdot A=\frac{\rho_{epi}[S+A]}{4\tan\alpha}Ln\left[\frac{A+2t_{epi}\tan\alpha}{A+2S-2t_{epi}\tan\alpha}\frac{2S+A}{A}\right],\quad \tan\alpha\leq\frac{S}{2t_{epi}} \tag{16}$$

$$=\rho_{epi}\left[t_{epi}-\frac{S}{2\tan\alpha}\right]+\frac{\rho_{epi}[S+A]}{4\tan\alpha}Ln\left[\frac{2S+A}{A}\right],\quad \tan\alpha\geq\frac{S}{2t_{epi}} \tag{17}$$

2.4 Total on-Resistance

The total on-resistance is simply the sum of three resistances which can be evaluated respectively as described in the previous sections. For comparison, the on-resistance is also calculated by use of the four components model[2].

$$R_{on}\cdot A=[R_{ch}+R_{acc}+R_{epi}]\cdot A \tag{18}$$

2.5 2-*D* Device Simulation

In order to verify the proposed model, two dimensional device simulation, which solves the Poisson's equation and continuity equation simultaneously by FEM method, is performed. The all input parameters are fitted for both the proposed and conventional analytical models as accurately as possible. The parameters used for present work are as follows : $S=15\mu m$, $t_s=2\mu m$, $t_b=5\mu m$, $t_{epi}=6\mu m$ and $\rho_{epi}=2.4\Omega\cdot cm$ (for 100V breakdown voltage), $t_{epi}=30\ \mu m$ and $\rho_{epi}=14.8\Omega\cdot cm$ (for 400 V breakdown voltage), $N_s=1\times10^{20}cm^{-2}$, $N_b=1\times10^{18}cm^{-2}$, $t_{ox}=1000$ Å, $V_g=10$V, and $9\times10^{10}cm^{-2}$ fixed oxide charge densities for (100) orientation. The t_{epi} and ρ_{epi} are chosen according to the design procedure proposed by *Hu* et al[2]. The 25% safety margins are also considered for the breakdown of planar junctions.

3. Results and Discussion

The on-resistance area products of Hu's model [2], our analytical model and 2-D simulation, when the breakdown voltage is 100 volts, are compared in Fig. 3 and Fig. 4 for both linear and cellular (square well in square cell) geometries respectively. It is shown in Fig. 3 that the proposed

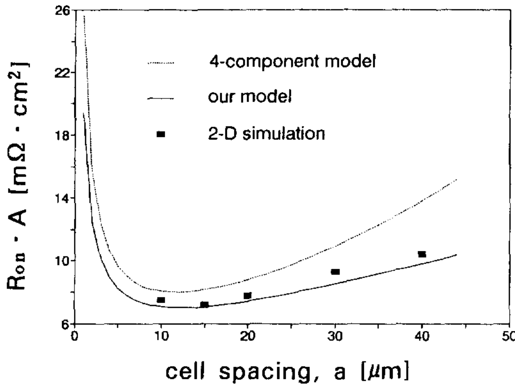

Fig. 3 on-resistance area product (BV=100V, linear geometry)

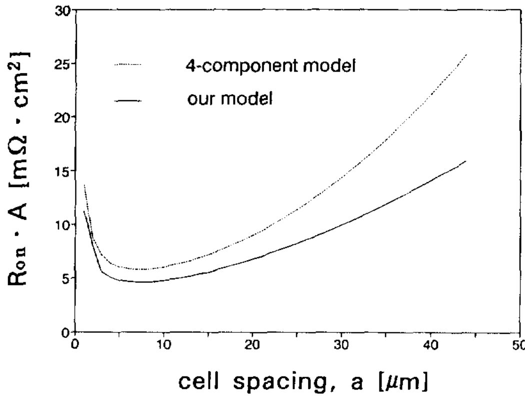

Fig. 4 on-resistance area product (BV=100V, cellular geometry)

model agrees fairly well with 2-D simulation but four components model [2] does not. In both figures, it is found out the the minimum on-resistance can be seen at the nearly same *p* body cell spacing in both models, While 14% and 26% discrepancies of the minimum on-resistance can be found for both linear and cellular geometries respectively. Moreover, in our model at Fig. 3 and Fig. 4, the changes of on resistance with cell spacing are more gradual, which implies less sensitivity of on-resistance to cell spacings. It is a desirable result in the optimun design of VDMOS where the quasi-saturation effects are also considered. These results show that the conventional four components model [2] is not suitable for the estimation of on-resistance in low voltage VDMOS.

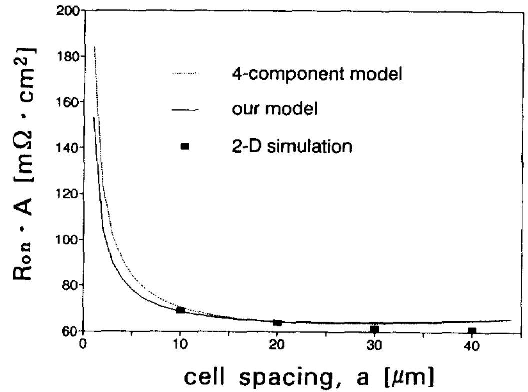

Fig. 5 on-resistance area product (BV=400V, linear geometry)

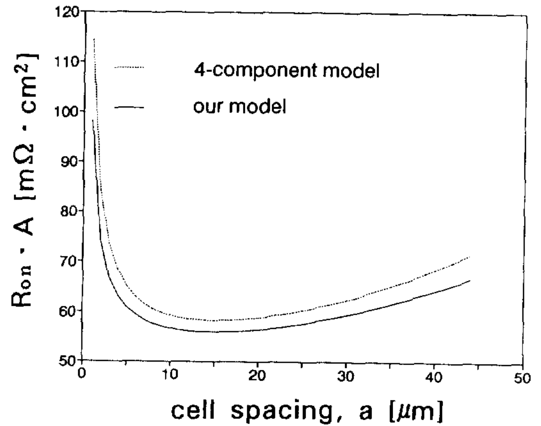

Fig. 6 on-resistance area product (BV=400V, cellular geometry)

The on-resistances, when the breakdown voltage is 400 volts, are compared in Fig. 5 and Fig. 6 for both linear and cellular geometries respectively. In Fig. 7, the resistance components of two models are also shown for the linear geometry. The validity of the proposed model is clearly shown in Fig. 5, where the proposed model agrees well with both 2-D simulation and four components model [2] in high voltage regime. However, the four components model underestimates the *epi* resistance and overestimates the other resistances, which can be clearly observed in Fig. 7.

The discrepancies of two models at the minimum on-resistance for the above figures are analyzed and summarized in Table 1. The differences

Table 1 The discrepancies of our and conventional models at the minimum on-resistance

		$\frac{R_{x,c}-R_{x,p}}{R_{x,p}}$ [%]			$\frac{R_{x,c}-R_{x,p}}{R_{on,p}}$ [%]			$\frac{R_{on,c}-R_{on,p}}{R_{on,p}}$ [%]
BV[V]	GEOMETRY	R_{ch}	R_{acc}	R_{epi}	R_{ch}	R_{acc}	R_{epi}	R_{on}
100	linear	30.58	30.80	−14.35	6.17	13.27	−5.40	14.04
	cellular	30.58	42.87	4.39	6.16	18.45	1.62	26.23
400	linear	27.43	32.54	−8.89	0.86	5.89	−7.04	−0.29
	cellular	27.43	41.10	−2.43	0.70	6.30	−1.99	5.01

$R_{x,c}$: converntional resistance component($x=ch$ or acc or epi)
$R_{x,p}$: proposed resistance component($x=ch$ or acc or epi)
$R_{on,c}$: conventional on-resistance($R_{on,c}=R_{ch,c}+R_{acc,c}+R_{epi,c}$)
$R_{on,p}$: proposed on-resistance($R_{on,p}=R_{ch,p}+R_{acc,p}+R_{epi,p}$)

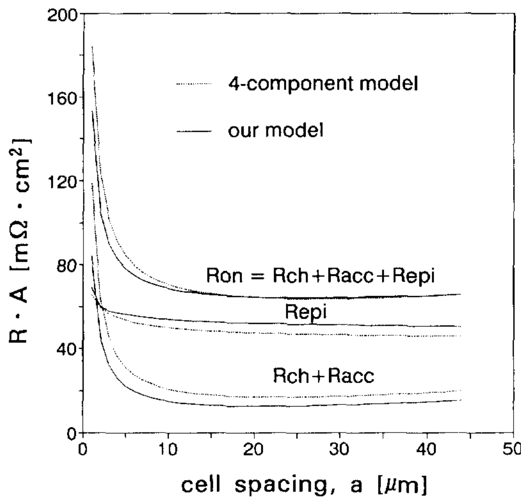

Fig. 7 on-resistance area product (BV=400V, linear geometry) (the resistance components of two models are shown)

of the minimum on-resistance and each resistance component between the two models are compared. It is also listed that how much errors of each resistance component result in the discrepancies of the minimum on-resistance. When the breakdown voltage is 100 volts and the cell geometry in linear type Fig. 5, for example, the discrepancies of channel, access, and epi resistances at the minimum on-resistance are 30.58%, 30.8%, and −14.35% respectively. Therefore, the 14% dicrepancies of the minimum on-resistance results from 6.17%, 13.27%, and −5.4% differences of channel, access, and epi resistances respectively. However, in reality, the errors of the minimum on-resistance are not 14% but 24.84%, because conventional four components model underestimates the epi resistance and overestimates other resistances. It is found out in Table 1 that the errors resulted from trapezoidal epi resistance model exceed 5% in low voltage regime and even in high voltage regime for the linear geometry. A relatively much contribution of access resistance errors to the minimum on-resistance discrepancies in cellular geometry may be due to the increase of accumulation areas. But, as the breakdown voltage decreases below 100 volts, the channel resistance effects may be more important[1].

It is certain from the results of present work that the conventional four components model should overestimate the on-resistance of low voltage VDMOS and the proposed model is appropriate for evaluating the on-resistance of low voltage VDMOS.

4. Conclusion

Based upon simple analytical models, it is shown in this paper that it is necessary to estimate on-resistance of low voltage VDMOS accurately because conventional four components on-resistance model is not adequate in low voltage

regime. An advanced on-resistnace model, which considers the lateral gaussian doping profiles in the channel region and accurate current spreading angles in the epitaxial layer for both linear and cellular geometries, is proposed and proved to be appropriate for low voltage regimes through 2-D device simulation of 100 V breakdown voltage VDMOS.

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