論 文

Data Bit Jitter가 Data 동기회로의 Bit Slip Rate에 미치는 영향에 관한 연구

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Effect of Data Bit Jitter on the Bit Slip Rate of the Data Tracking Loop

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要 約 본 논문은 Data Bit Jitter(DBJ)가 Data 동기수신회로의 Bit Slip Rate (BSR)에 미치는 영향에 관하여 고찰하였다. 특히 이 논문에서는 BSR치를 계산하는데 필요한 특성 jitter parameter들을 부각시켰으며 또한 DBJ에 관한 새로운 규격설정을 제시하였다. 새로이 제시된 방법에 의하면 종래의 방법에 비하여 복잡해진 점은 있으나, 반면 보다 현실적이고 보다 더 정확하게 DBJ의 BSR에 관한 영향을 예측할 수 있는 장점이 있다고 생각된다. 새로이 제시된 방법에서는 수신기에 의존하는 parameter들이 부각되었으며 jitter spectrum의 각 부분(저주파, 고주파 부분등)에 대한 적절한 비중이 고려되었다.

ABSTRACT This paper analyzes effect of Data Bit Jitter (DBJ) on the Bit Slip Rate (BSR) of the receiver Data Tracking Loop (DTL). In particular, we point out the characteristic jitter parameters that can be used to estimate the BSR performance for the low frequency and high frequency parts respectively. We also propose a new format for the DBJ specification, which is more sophisticated than the conventional method but is believed to be more practical and accurate in predicting DBJ effect on the receiver BSR performance. In the proposed method, receive dependent parameters are identified and weighting between different parts of jitter specturm are properly considered.

I. Introduction and Background

This paper investigates the relationship between Data Bit Jitter (DBJ) and Bit Slip Rate (BSR). DBJ is the timing jitter at each data transition epoch associated with the baseband digital data stream (or data clock) [1 3]. It corresponds to the so called 'phase noise' [2 3] in CW carrier. Bit slip is an insertion of a bit into the data stream or a deletion of a bit from it due to the cycle slip of the

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associated data clock. It corresponds to the 'cycle slip' in CW carrier [4 5 6]. BSR is usually expressed in number of bit slips per second.

The control of DBJ is important in the digital communication link to assure the design link performance [1 3]. When coherent modulation technique is involved, tracking receiver may make occasional bit slips when jitter value is not properly controlled. BSR will disrupt the deinterleaving and decoding as well as the frame synchronization. In general, BSR effect becomes more serious as the data rate increases. Its occurance is quite catastrophic and therefore its probability of occurrence must be kept to a minimum.

The current DBJ specification is based on the frequency modulation (FM) theory and is typically specified in terms of maximum jitter frequency (f_m) and peak deviation (Δf) for sunusoidal modulation ; and peak jitter rate (B_m ; 3σ value) and rms deviation (σ_f) for random (Gaussian) modulation respectively.

The problems with the current specification is that it is too much simplified and thus neglects to include (i) effect of receiver tracking loop (type of loop, loop BW, and other loop parameters) on the BSR, and consequently ignores (ii) the fact that BSR is sensitive to the spectral location of the jitter spectrum (i. e., low and high frequencies).

In this paper, we will start reviewing the problems associated with the current specification, investigate the relationship between DBJ and BSR and propose a new specification based on practical considerations.

The organization of this paper is as follows. In section 2, we present analysis of bit slip in terms of phase error of the clock recovery loop. Section 3 analyzes effect of jitter at frequencies outsied the tracking loop BW (high frequency region). Section 4 does the same for jitter components inside the tracking loop BW (low frequency region). In Section 5, the efect of data transition density on the BSR is discussed. Based on the results of the previous sections, a new DBJ specification is proposed in section 6. Finally, a summary is provided in Section 7.

Ⅱ. Modeling of Bit Slips

To analyze the effect of DBJ, to be considered here as phase modulation on the data clock, on the receiver detector performance for BSR, we consider two different types of receiver architecture.

In a reclocking type of circuit, a single sample detection of an unfiltered data stream is performed. Here, a bit slip occures when the phased difference between the transmitter clock and the receiver clock exceeds half a symbol time or π radians. However, its deleterious effect only manifest itself if the phase difference does not return below π radians for many bits. The # of bits required depends on the response time of the lock detectors in the receiver system (deinterleaver, decoder, frame sync, etc.).

In a matched filter type of receiver, the situation is more complicated. If the phase error exceeds π radians by only a small amount, the situation may be described as a loss of signal energy for some bits rather than as a cycle slip. Only a phase error considerably larger than π radian will come out as a true bit slip. For bit jitter components inside the tracking loop BW (low frequency region), this distinction is of little consequence, since it will cause cycle slip anyway as soon as the error

exceeds π radians and the loop will pull towards the next stable lock points at $\pm 2\pi$ radians. However, the high frequency jitter components do not affect the pulling behavior of the loop since they cannot be tracked ; thus they can increase the phase error well above π radians and then reduce it again instantaneously. Based on the above considerations a bit slip is declared whenever the fast (high frequency) components carry the phase error beyond π radians (worst case approximations) or when the slow (low frequency) components cause a cycle slip. Therefore, in the following two sections, we consider the effect of high frequency jitter and low frequency jitter separately. The separate analysis provides similer results in the intermediate frequency range so that the division between the two regions is considered to be not critical.

Ⅲ. Effect of High Frequency Jitter Components

In the following discussions, jitter can be conveniently divided into two components : sinusoidal (spurious) jitter and random jitter. It will be shown that each component affects the BSR in a different manner.

3. 1 Spurious Jitter

If the frequency of a jitter spur is considerably higher than the loop BW, it is not tracked by the loop. The variations of the local clock phase are, therefore, the same as they would be in the absence of that spur. Hence, the transmitter phase variation due to the spur is simply added to the phase error without the spur. Thus we partition the phase error process as

$$\phi(t)=\phi_n(t)+\phi_h(t) \tag{1}$$

where $\phi(t)$ is the total phase error process, $\phi_h(t)$ is the spurious jitter process outside the loop BW (untracked jitter), and $\phi_n(t)$ represents effect of thermal noise (the receiver clock oscillator instability is neglected).

If the process $\phi_h(t)$ has a peak value of $\hat{\phi}_h$, the process $\phi(t)$ is very likely to exceed $\pm\pi$ whenever the process $\phi_n(t)$ exceeds $\pm(\pi-\hat{\phi}_h)$ since ϕ_h varies much faster than ϕ_n. Hence, the bit slip rate can be computed as the rate at which the porcess $\phi_n(t)$ crosses boundaries at $\pm(\pi-\hat{\phi}_h)$.

Fig. 1 is the BSR computed from this model as a function of the loop SNR for various values of $\hat{\phi}_h$. First, we note that ϕ is inversely proportional to the loop SNR, SNR_L.

$$\phi^2 \sim 1/SNR_L \tag{2}$$

We also note that BSR is obtained by using the equation of cycle slips of the generic PLL[4, 5].

$$BSR=4B_L/[\pi \cdot \exp(2 \cdot SNR_L)] \tag{3}$$

where B_L is the one-sided loop BW of the tracking loop. Then Figure 1 is obtained by using Equations (1), (2) and (3).

Fig. 1 does not reflect the fact that the loop SNR is reduced by the sinusoidal phase modulation. From the FM theory, we know that the residual carrier strength is proportional to the Bessel function of the jitter value, $Jo(\phi_h)$ [10]. Fig. 2 takes this effect into account by showing the bit slip rate as a function of the total carrier power, including modulation sidelobes due to spurs. Fig. 2 is considered to be

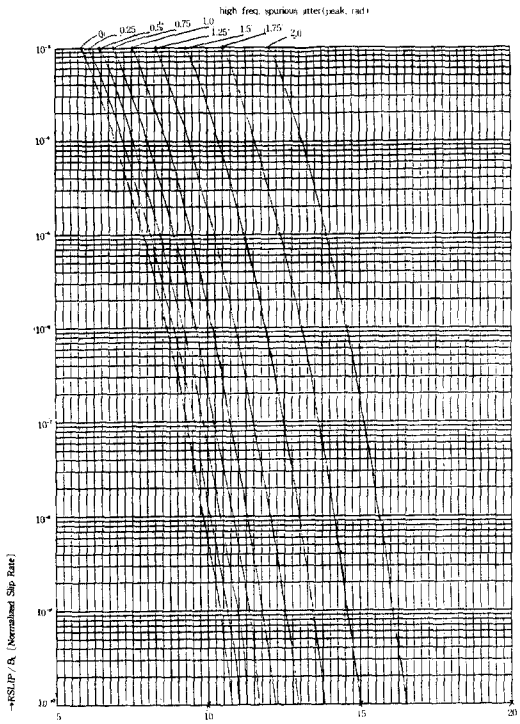

Fig. 1 Bit Slip Rate due to High Freq. Spurious Clock Jitter.

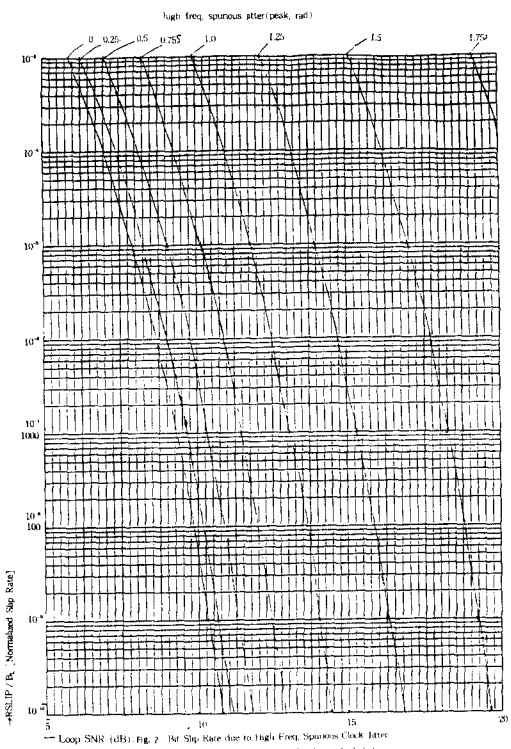

Fig. 2 Bit Slip Rate due to High Freq. Spurious Clock Jitter with Loop SNR loss due to Modulation Included

more realistic than Fig. 1.

3. 2 Random Jitter

For Gaussian jitter components outside the loop BW, the problem is complicated since there is no finite value for the peak of the jitter. The probability of this process to exceed a certain value during a given time interval depends not just on the variance of the process, but on its whole spectrum.

For the computation of this probability we model the process $\phi_n(t)$ and $\phi_h(t)$ as piecewise constant process. Let's assume that $\tilde{\phi}_n(t)$, takes on a new value every B_L^{-1} seconds, and $\tilde{\phi}_h(t)$ takes on a new value every f_{max}^{-1} seconds, where f_{max} is the highest frequency in the jitter process. By assuming that the values taken on by $\tilde{\phi}_h(t)$ are independent and Gaussian, we can compute the PDF of the maximum of the process $\tilde{\phi}_h(t)$ during a time interval of duration B_L^{-1}, $P_{max}(\hat{\phi}_h)$. Let $F_{max}(\hat{\phi}_h)$ be the CDF of $\phi_h(t)$ process (i. e., the integral of $P_{max}(\hat{\phi}_h)$.) and $F_i(\tilde{\phi}_h)$ be the CDF of the i-th $\phi_h(t)$ process during B_L^{-1} interval. Then we know that $F_{max}(\hat{\phi}_h)$ can be expressed by [11, Ch.6]

$$F_{max}(\hat{\phi}_h)=F_1(\tilde{\phi}_h)\cdot F_2(\tilde{\phi}_h)\cdots\cdots\cdot F_N(\tilde{\phi}_h) \quad (4)$$

where we have assumed $B_L^{-1}/f_{max}^{-1}=N$. For Gaussian $F_i(\tilde{\phi}_h)$, $F_{max}(\hat{\phi}_h)$ can be computed numerically by using Eq.(4).

Then, the mean time between slips can be computed by using the equation

$$\bar{S}=\int_{-\pi}^{\pi} \bar{T}^{-1}(\hat{\phi}_h)P_{max}(\hat{\phi}_h)d\hat{\phi}_h \quad (5)$$

where $\bar{T}^{-1}(\hat{\phi}_h)$ is the mean time to reach the boundary at $\pm(\pi-\hat{\phi}_h)$, which can be computed by using the Equation (1) or can be

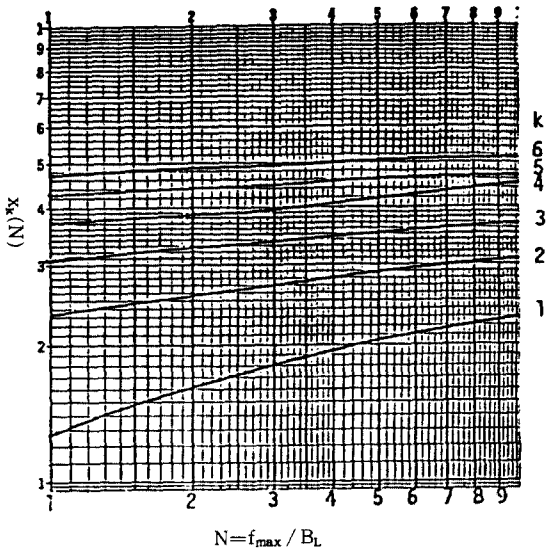

Fig. 3 Plot of Function $x_k(N)$

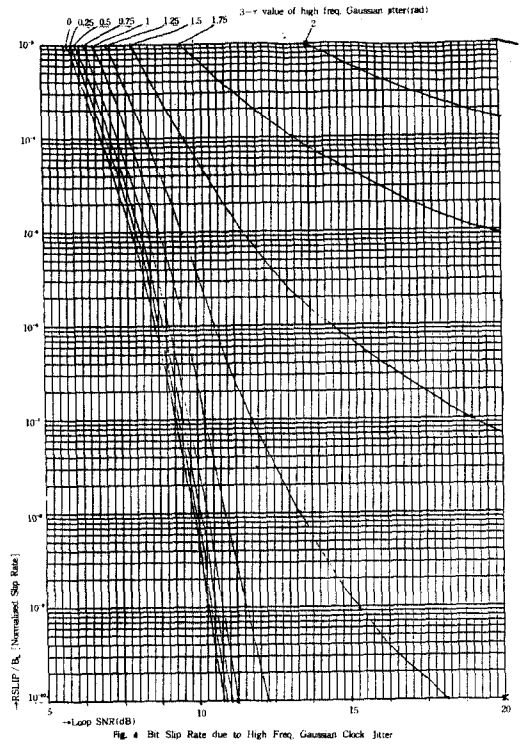

Fig. 4 Bit Slip Rate due to High Freq. Gaussian Clock Jitter

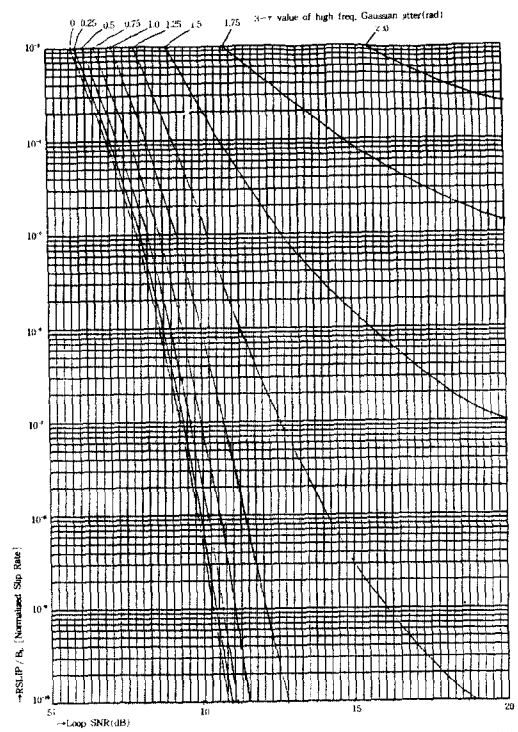

Fig. 5 Bit Slip Rate due to High Freq. Gaussian Clock Jitter with Loop SNR Loss due to Modulation Included

obtained from Fig. 1 or Fig. 2.

According to this expression, the bit slip rate depends on the maximum frequency of the jitter, f_{max}. However, as pointed out in Sec. 2, a bit slip can only occur if the phase error exceeds π radians for a time larger than what the sync detectors in the combined receiver need to respond. For a decoder, for example, the response time is typically a few hundred symbols. Hence, the cutoff frequency f_{max} could typically be set to approximately a few percent of the symbol rate R_s. Since the slip rates of interest are very low, only the behavior of $P_{max}(\hat{\phi}_h)$ for high values of $\hat{\phi}_h/\sigma_h$, where σ_h is the rms variation of ϕ_h, needs to be considered for only then is $\overline{\Psi}^{-1}(\hat{\phi}_h)$ very large to contribute to the above integral.

On the other hand, the function is very insensitive to f_{max} in the range of high $\hat{\phi}_h/\sigma_h$. This point can be verified in Fig. 3 for $x_k(N)$ plot where $x_k(N)$ is defined as

$x_k(N)=x$ such that $\int_{-\infty}^{x_k} P_{max}(s)\,ds=1-10^{-k}$ (6)

and is plotted for various values of $N=f_{max}/B_L$ and $1\leqq k\leqq 6$.

BSR due to high frequency Gaussian jitter is obtained by numerically evaluationg Eq. (5) for $f_{max}=10\cdot B_L(N=10)$ and is shown in Fig. 4 for various 3-sigma jitter values. This result can approximately be applied to other values of f_{max} (or N) also since the result is relatively insensitive to N.

Just as in the previous case, Fig. 4 did not account for the carrier power loss due to the random modulation. From FM theory, we know that the power spectrum density of Gaussian modulation is also Gaussian[12] ; thus the carrier power rolls off at the rate of $\exp(-\sigma_h^2)$. Fig. 5 shows the corresponding results when the carrier suppression factor $\exp(-\sigma_h^2)$ is included. Fig. 5 is considered to be more realistic than Fig. 4.

Ⅳ. Effect of Low Frequency Jitter Components

For slow varying (low frequency) components of the jitter process, it can be assumed that bit slip corresponds to cycle slips of the general tracking loop. Theoretical analysis of the phase modulation limits of PLL at which cycle slips occur is extremely difficult. In this section, we will use primarily the available experimental results [9] for the cycle slipping behavior of phase locked loops to predict the bit slip performance of the data tracking loops. This extension is possible since data tracking lolp can be viewed as a generalized PLL[8]. Here we take the second order loop case only since this is by far the most popular choice[4].

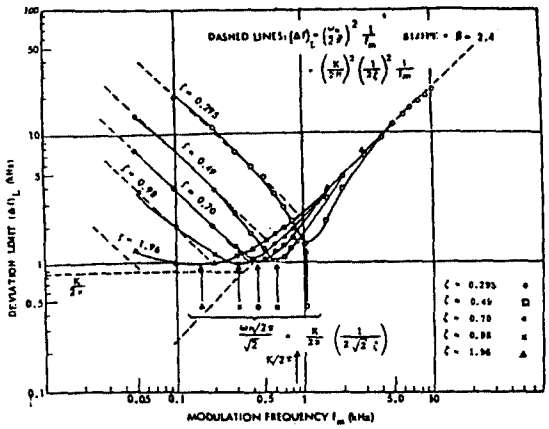

Fig. 6 Maximum Sinusoidal Frequency Deviation.

4. 1 Spurious Jitter

Fig. 6 is the deviation limits for sinusoidal FM modulation tracked by a second order PLL from Reference [9]. It can readily be seen that the curves can be approximated by high frequency and low frequency asymptotes. These asymptotes are replotted in Fig. 7 for phase modulation limits using a normalized frequency scale ($(\Delta f)_L/f_m$ and f_m/f_n, where f_n is the loop damping frequency) to make the curves independent of the loop damping. Also shown is the asymptotic approximation of the transfer function $|1-H(f)|$ for a second order tracking loop with a prefect integrator in the loop filter (Type Ⅱ loop). Multiplying the modulation limit and the transfer function results in a curve that is flat every where except for a short ramp near f_n. Thus, this result indicates that the loop can accept one radian of peak untracked sinusoidal phase jitter inside the tracking BW or 2.4 radians outside the tracking loop BW in the absence of thermal noise.

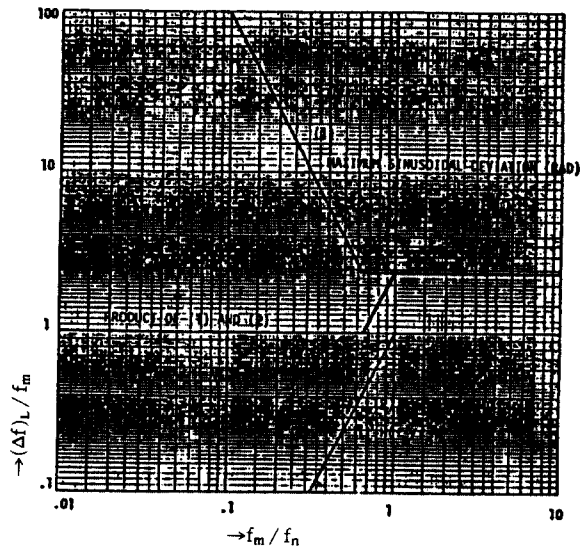

Fig. 7 Maximum Sinusoidal Phase Modulation and Untracked Phase Modulation.

4. 2 Random Jitter

The theory for low frequency random jitter can also be developed from the experimental data taken from[9], which is replotted in Fig. 8. These measurements were made with a frequency jitter which has a flat spectral density from DC to f_{max}. The asymptotic boundaries for the rms frequency modulation limit can be obtained by manipulating the results of [9] ;

for Low Frequency : ($f_{max}<f_n=f_o$)

$$\sigma_f \leqq \frac{\sqrt{3}\, f_n^2}{\tau f_{max}}$$

for High Frequency ; ($f_{max}>fo$)

$$\sigma_f \leqq \frac{\sqrt{\pi f_n \xi f_{max}}}{\tau} \qquad (7)$$

where τ is the crest factor[9], and ξ is the loop damping factor.

For our purpose, we modify the above results to model the jitter power spectral density as a bandlimited white process such that

$$S_J(f)=\begin{cases} N_o, & o \leqq f \leqq f_{max} \\ o, & \text{otherwise} \end{cases} \qquad (8)$$

Then it can easily be verified that equivalent N_o must be set to

$$N_o=\frac{\sigma_f^2}{f_{max}}=\begin{cases} \dfrac{3f_n^2}{\tau^2 f_{max}^3}, & f_{max} \leqq f_o \\ \dfrac{\pi f_n \xi}{\tau^2}, & f_{max} \geqq f_o \end{cases} \qquad (9)$$

By manipulating this result, we find that an alternative way to specify the maximum allowable frequency jitter is

$$\int_o^\infty S_J(f)g(f)df \leqq A \qquad (10)$$

where the weighting function g(f) is defined as

$$g(t)=\begin{cases} f^2, & f \leqq f_o \\ 0, & f > f_o \end{cases} \qquad (11)$$

and $A=f_n^4/\tau^2$. We can readily verify that Eq. (10) in conjunction with Eq.(11) is equivalent to Eq.(8). In addition, Eq.(10) is generalized in the sense that includes both the high frequency and low frequency asymptotes in a single expression by introducing a weighting function.

This result indicates that phase jitter at frequencies higher than f_n has no effect on cycle slips. This is true for CW carrier since the high frequency components are not being tracked and thus cannot affect the slipping behavior. But bit slips can still occur at high frequency, as described in section 2.

If the spectrum of the clock phase jitter is considered, rather than the frequency jitter,

the weighting function should be replaced by a new function $\tilde{g}(f)$ which is defined by

$$g(f)=\begin{cases} f^4, & f\leqq f_o \\ o, & f>f_o \end{cases} \qquad (12)$$

The conversion from $g(f)$ to $\tilde{g}(f)$ is straightforward from the knowledge that the phase power spectrum can be obtained by multiplying f^2 to the frequency power spectrum[11 ch 10].

V. Transition Density Cosiderations

When the data transition density varies, several parameters of the clock recovery loop are affected. We will take Data Transition Tracking Loop (DTTL) [7 8] as a representative data tracking loop and investigate how the loop BW, clock jitter, bit slip rate and loop SNR change in a DTTL as a function of the transition density. For other tracking loops, similar conclusions can be made with minor modifications [8].

(a) CNR_L variation : Since the tracking loop performs a nonlinear operation on the received signal, the CNR in the loop is not equal to the link CNR. The ratio between the two is given by $S_L=CNR_{loop}/CNR_{link}$ and is called the squaring loss. In general, the loop CNR decreases with transition density (S_L increases with transition density).

(b) B_L variation : when computing the bit slip rate, we have to consider that the loop BW varies as a function of the transition density and E_s/N_o, i. e.,

$$B_L=2P_tB_{Lo}\,f(E_s/N_o) \qquad (13)$$

where B_{Lo} is the nominal loop BW(which is

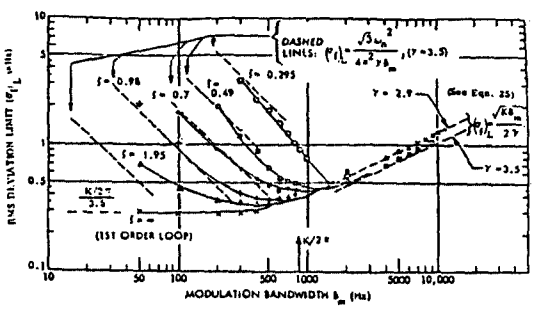

Fig. 8 Maximum Noise Frequency Deviation.

defined for $P_t=0.5$ and $E_s/N_o=\infty$) and f (E_s/N_o) is a scaling function which accounts for the E_s/N_o correction factor.

(c) The combined effect of the above is that for high values of E_s/N_o the loop SNR is insensitive to the transition density P_t wihille for low values of E_s/N_o, it degrades quite fast with a reduction in P_t.

VI. Proposed DBJ Specifications

In previous sections, we have considered the following two cases ; (a) the combined effect of thermal noise and high frequency jitter,and (b) the effect of low frequency bit jitter on a noise-free tracking loop. While the former results provide quantitative relationships between the tracking loop SNR, the data bit jitter and bit slip rate, the latter results can be used to extend these relationships to frequencies inside the tracking loop bandwidth.

Based on the above concept, we suggest a new format for the data bit jitter specification. Here, we take a huristic approach rather than a rigorous treatment so that further improvement can be made later on this subject. It differs from the conventional specification in the following aspects ; (a) It combine the

results on low frequency and high frequency and present a unified treatment, (b) phase jitter rather than frequency jitter is specified, (c) spurious and random components are treated separatly, and finally (d) weighting functions are introduced for spurious and random jitter components to account for the interaction between DBJ spectrum and tracking loop behavior.

The proposed algorithm is as follows :

To meet the BSR requirement of $BSR<BSR_{max}$, Combined jitter must be less than A (radian), where Combined jitter, DBJ_{com}, is defined as

$$DBJ_{com}=C_s+C_n \le A \tag{14}$$

and the combined jitter is the sum of the weighted spurious component C_s and random phase jitter component C_n.

The weighted spurious component is defined as

$$C_s=\sum_{k}^{J} a_k W_s(f_k) \tag{15}$$

where a_k is the amplitude, f_k is the frequency of the k-th spur and $W_s(f)$ is the weighting function. The sum is taken over all spurs.

The weighted random component is defined as

$$C_n=\sqrt{\int_0^{\infty} S_j(f)W_n(f)df} \tag{16}$$

where $S_j(f)$ is the spectrum of the phase jitter and $W_n(f)$ is the weighting function.

The weighting function for the random jitter, $W_n(f)$, and spurious jitter, $W_s(f)$, is shown in Fig. 9 and Fig. 10 respectively. The value of A, as well as the exact shape of the

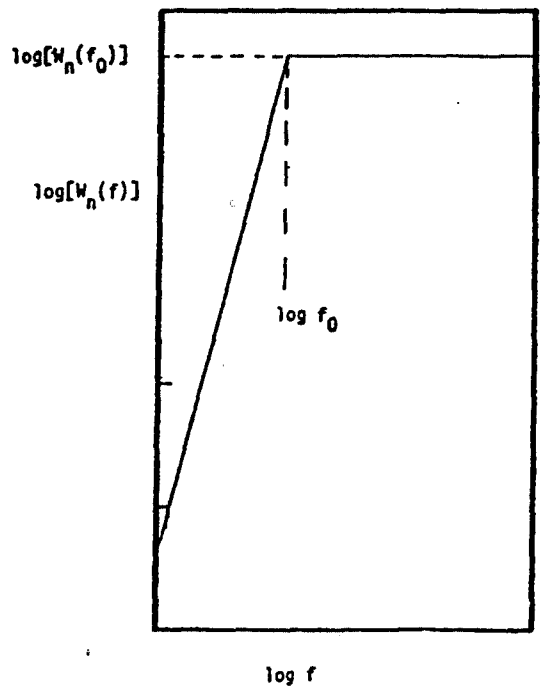

Fig. 9 Proposed Weighting Function for Random Bit Jitter.

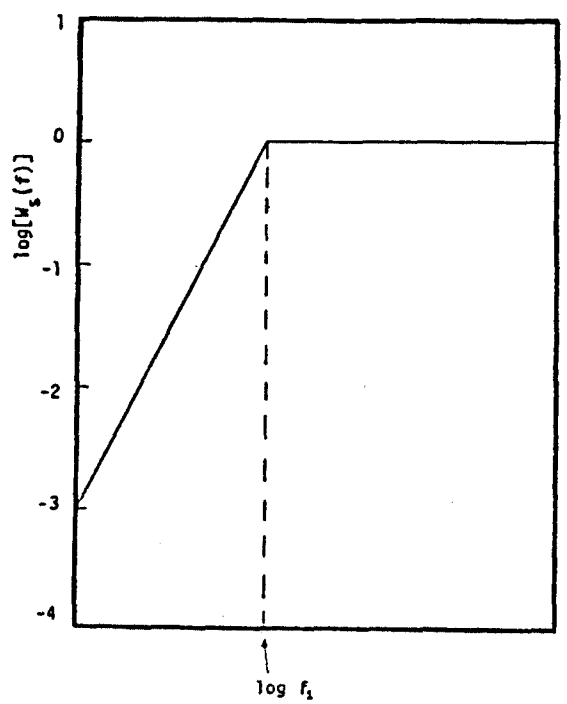

Fig. 10 Porposed Weighting Function for Spurious Bit Jitter.

weighting functions $W_s(f)$ and $W_n(f)$ must be determined from the maximum allowable bit slip rate BSR_{max}, the range of permissible data transition densities, the minimum E_s/N_o and the ratio of tracking loop BW and data rate.

The weighting function $W_s(f)$ and the breakpoint are suggested by the result of Sec. 4.1 or by curve (1) in Fig. 7 : since Fig. 7 is for the maximum allowable jitter, the derating curve must be the inverse of if. For the weighting function $W_s(f)$, the break point f_1 is defined as $f_1=f_n/\sqrt{2.4}$ (f_n in this case is the tracking loop natural frequency for the worst transition density in the permissible range and the lowest nominal value of E_s/N_o). The scaling of W_s is arbitrary at this point : for convenience, the horizontal part is set to unity.

The weighting function $W_n(f)$ is suggested by the result of Sec.4.2 or by function $\tilde{g}(f)$ in Eq.(12) ; it is proportional to f^4 for low frequencies and is constant for high frequencies. The proper scaling for the high frequency asymptotes can be found from Fig. 5 while the proper scaling for the low frequency asymptote is not obvious. However, the breakpoint should be f_o, so the two asymptotes will be joined at this frequency. The value of $W_n(f)$ must be computed for the specific link conditions and desired BSR_{max}.

Ⅶ. Conclusions and Discussions

In this paper, we have investigated the effect of DBJ on BSR from a practical point of view and proposed a new method of DBJ specification. In the proposed method, receiver dependent parameters are identified and the weighting between different parts of jitter spectrum are properly considered. The new DBJ specification is given in a huristic manner so that further discussions and critiques can be made on this subject.

Although this method is more sophsticated than the conventional method, it is believed that it will give more insight into the effect of jitter on the coherent reveive and generate more accurate predictions on the effect of DBJ on BSR performance. In addition, the graphical information provided in Figures 1 to 8 can be used as a valuable data for the desing of the digital receiver to minimize the jitter effect on BSR.

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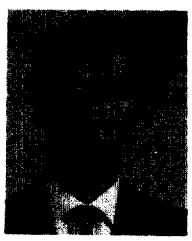

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