A Generalized Coding Algorithm for m Input Radix p Shadow-Casting Optical Logic Gate

(다중입력 Shadow-Casting광 논리게이트를 위한 코딩방식의 일반화)

崔 道 亨**, 權 元 鉉,* 朴 漢 奎*

(Do Hyung Choi, Won Hyun Koun and Han Kyu Park)

要 約

본 논문에서는 shadow-casting 논리 게이트에 있어서의 S. Kozaitis 등이 제안한 코딩 알고리즘에 대한 문제점을 고찰하고 입력의 갯수가 2N(N은 자연수)이 아닌 경우 발생하는 불필요한 pixel의 수를 최소화 시킬 수 있는 일반화된 코딩 방식을 제안하였다.

제안된 코딩 방식의 유효성을 입증하기 위하여 코딩 효율등과 같은 시스템 성능을 이론적으로 분석하였고 64개의 데이타량을 갖는 세 개의 이진 입력을 선정해 논리동작을 수행하고 이 결과를 사진으로 제시 하였다.

Abstract

A generalized coding algorithm for multiple inputs multiple-valued logic gate based on shadow-casting is proposed.

Proposed algorithm can minimize the useless pixels in case the number of inputs is not 2N (N is a natural number).

A detailed analysis of advantages of proposed algorithm is presented and its effectiveness is demonstrated in case of three input binary system using inputs of 8 x 8 data.

I. Introduction

In comparison with the existing computer systems, the optical computing system has several advantages such as large capacity, high speed, high parallelism, and its immunity to the electromagnetic interference [1,5].

Until now, many studies have been carried out for optical logic gates which are essential element for optical computing, utilizing such devices as LC (liquid crystal), LCLV (liquid crystal light valve), MSLM (microchannel spatial light modulator), and shadow casting method, Since D.R. Maure Suggested Shadow-Casting method for

*正會員, **準會員, 延世大學校 電子工學科
(Dept. of Elec. Eng., Yonsei Univ.)
接受日字 : 1988年 2月 12日

logic operation[1], Y. Ichioka and J. Tanida performed 16 logic operations using shadow-casting method for two binary inputs in 1983[2.3].

And in 1985, S. Kozaitis and R. Arrathoon performed multiple inputs and multiple-valued logic operation[4], but it has disadvantage of increasing useless pixels when the number of inputs is not 2N (N is a natural number)[6].

This paper proposes a generalized coding algorithm which can minimize the unnecessary pixels for logical operations when the number of inputs is not 2N, and theoretical analysis of system performance is presented.

In order to demonstrate the feasibility of proposed coding algorithm for multiple inputs and multiple-valued logic gate operation, logic operations of three input binary system such as $F_0(A)$, $F_1(B)$, $F_2(C)$, $F_6(A\dot{B}C)$ . . . are performed and output results are presented in photographs.

II. Multiple inputs and Multiple valued Logic Gate

In general, m input radix p system has p^m possible input combinations and p^{p^m} possible output combinations. Multiple inputs and multiple-valued logic operation can be performed by using proper coding method and by altering LED radiation patterns.

As an example, coding patterns of S. Kozaitis and R. Arrathoon for 2 input radix 2, 2 input radix 3 and 4 input radix 2 system are illustrated in Fig.1(a), Fig.1(b), and in Fig.1(c), respectively [4,5].

Fig.2 shows the geometrical configuration of 3 input radix 2 system.

As shown in Fig.2, the necessary number of LEDs for m input radix p system is generally equal to the number of possible input combination, and the intensities of each LEDs should be properly selected from one of p levels.

In general, shadow-casting system operates efficiently for a small input numbers m because necessary number of pixels for logic operation increases with p^m.

As previously mentioned[6], S. Kozaitis and R. Arrathoon's coding method generates unnecessary pixels in m input radix p system when the number of inputs is not an even number.
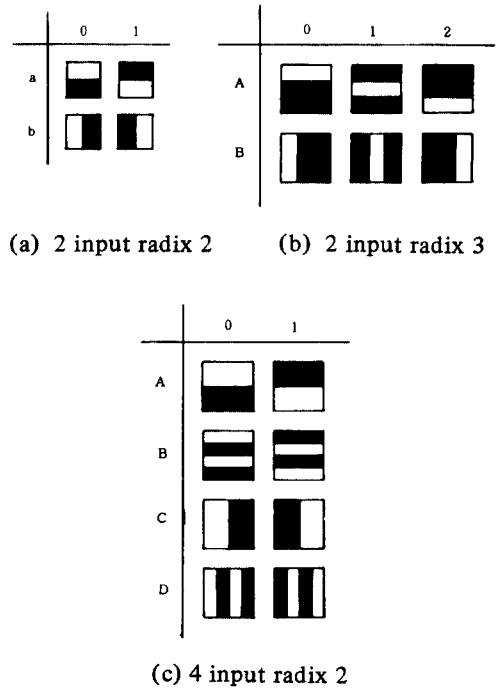

(a) 2 input radix 2   (b) 2 input radix 3

(c) 4 input radix 2

Fig.1. Coding patterns for multiple inputs and multiple-valued logic gate.
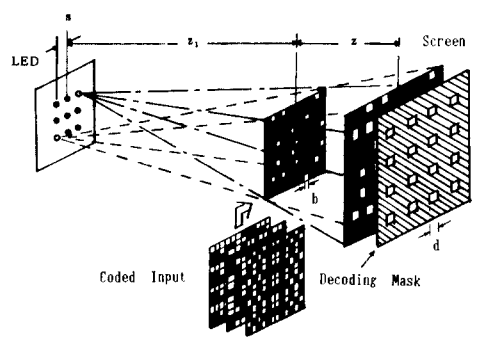

Fig.2. Goemetrical configuration of 3 input radix 2 system.

As an example, 3 input radix 2 system has 8 possible input combinations and 256 output functions, as shown in Table 1.

Fig.3 represents the S. Kozaitis and R. Arrathoon's coding method for 3 input radix 2

Table 1. Output functions for 3 input radix 2 system.

	F 0	F 1	F 2	F 3	F 4	F 5	F 6	F 7	F 8	......	F256	LED Number
ABC	A	B	C	$\bar{A}$	$\bar{B}$	$\bar{C}$	$A\bar{B}C$	AC	$\bar{A}B$	...	TRUE	
000	0	0	0	1	1	1	0	0	0	...	1	1
001	0	0	1	1	1	0	0	0	0	...	1	2
010	0	1	0	1	0	1	0	0	1	...	1	3
011	0	1	1	1	0	0	0	0	1	...	1	4
100	1	0	0	0	1	1	0	0	0	...	1	5
101	1	0	1	0	1	0	1	1	0	...	1	6
110	1	1	0	0	0	1	0	0	0	...	1	7
111	1	1	1	0	0	0	0	1	0	...	1	8

system, which is obtained by setting input A to zero in Fig.1(c). As shown in Fig.3, the number of useless pixels increases in case of three inputs because coding has to be done after fixing one input to zero among 4 inputs, and therefore the size of pixels should be decreased a quarter of that of two input binary system in Fig.1(a).

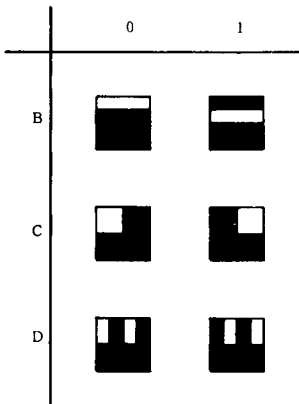This effect degrades the system performances such as possible input number and radix.

Fig.3. Coding patterns of R. arrathoon's.

III. Proposed Coding Algorithm

In this paper, a generalized coding algorithm for m input radix p shadow-casting system which can minimize the useless pixels is proposed and its principle is as follows:

i) Find the least natural number k which is larger than the number of possible input combinations p^m, but can be represented by k^2. That is, for the m input radix p system, find the natural number which satisfies

$$p^m < k^2 \qquad (1)$$

ii) Divide each input cell into k*k squares, and assign randomly one input combination to the each subdivided pixels. One possible assignment for 3 input radix 2 is shown in Fig.4.

iii) Among the assigned patterns, select the patterns which have the required input function and superimpose them. For example, coding pattern of A can be obtaied by superimposing $A\bar{B}\bar{C}$, $A\bar{B}C$, $AB\bar{C}$ and ABC patterns in Fig.4.

iv) For other input functions such as $\bar{A}$, B, $\bar{B}$, C and $\bar{C}$, repeat step iii)

This principle can be extended m input radix p system.

LED radiation pattern for each logic operation can be obtained by matching input combinations which has nonzero output function with related LED pattern, as shown in Fig.5

For example, logic operation of F7(AC) in Table 1 can be obtained by turning on LED 6, 8 whose output functions are not zero.

As an illustration of the proposed algorithm, we code three input radix 2 system by the following procedures:
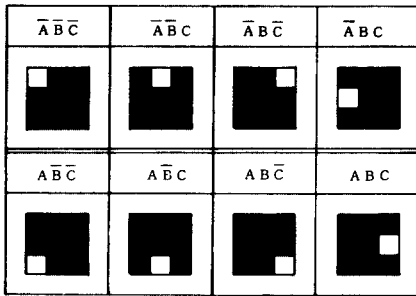
Fig.4. Method of input assignment.

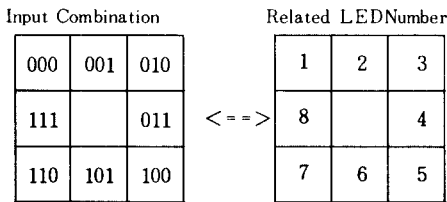**Fig.6.** One possible coding pattern of 3 input radix 2 system.

Fig.5. LED radiation pattern.

i) Possible input combinations are 2^3, therefore select the least natural number which can be expressed

$$2^3 < k^2$$

i.e. k=3

i i) Divide each input cell into 3*3 pixels, assign each input combination to the corresponding pixel. This assignment can be done randomly. One among 9 pixels is not used because possible input combinations for A,B and C are eight, i.e. 2^3.

iii) Coding pattern for A,Ā,B,B̄,C,C̄ can be obtained by superimposing assigned pixel according to the step iii), iv).

These results are shown in Fig.6.

Proposed coding method is not a fixed one because another coding pattern can be obtained by altering the method of assignment of step ii).

Table 2 shows the required number of pixels of the proposed algorithm for m input radix p system in comparison with the previous publication[4]. As shown in Table 2, necessary number
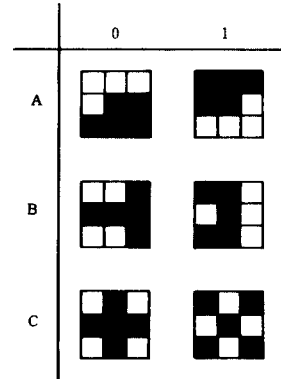
Table 2. Comparison of coding efficiency of the proposed algorithm and Ref. [4]

p		m	2	3	5	7	9	⋯
2		p	4	8	32	128	512	⋯
	N	*	4	16	64	256	1,024	⋯
		* *	4	9	36	144	529	⋯
3		p	9	27	243	2,187	19,683	⋯
	N	*	9	81	729	6,561	59,049	⋯
		* *	9	36	256	2,209	19,881	⋯
4		p	16	64	1,024	16,384	262,144	⋯
	N	*	16	256	4,096	65,536	1,048,576	⋯
		* *	16	81	1,089	16,641	263,169	⋯
⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮

N : Number of required pixels
* : Calculated from ref. [4]
* * : Proposed algorithm

of pixels for the proposed method are equal to the previous one in case that numbers of inputs are 2N (N is a natural number). But in other case, the proposed method is more efficient than the previous method.

IV. Experimental results

In order to illustrate the effectiveness of the proposed method, logic operations are performed for 8*8 three inputs shown in Fig.7. After subdividing each input cell into 9 pixels, coding is performed according to the proposed algorithm.
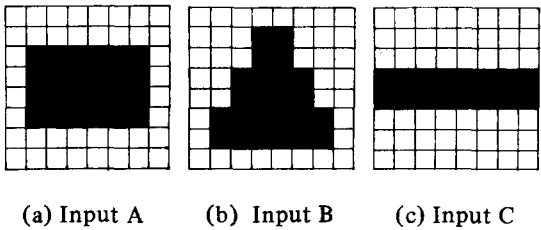
(a) Input A   (b) Input B   (c) Input C

Fig.7. Input patterns.

(a) F0 (A)   (b) F1 (B)   (c) F2 (C)

(d) F3 (Ā)   (e) F4 (B̄)   (f) F5 (C̄)

Fig.8 shows the resultant coded input and decoding mask. Designed system has s = 6 mm, b = 0.7 mm, d = 0.79, z = 9.2 mm, z1 = 70 mm. Photo 1 (a) - (g) shows the output of logic operations such as $F\theta(A)$, Fl(B) . . ., etc.
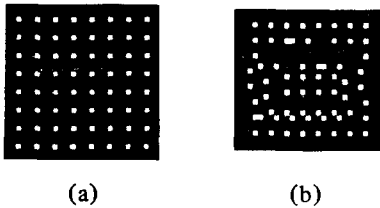

(g) F6 (ABC)   (h) F7 (AC)   (i) F8 (ĀB)

(a)   (b)

Fig.8. (a) Coded input and (b) Decoding mask.

(j) F11 (A + B)   (k) F12   (l) F255
                    (A + B + C)   (TRUE)

Photo 1. Experimental results

V. Conclusions

We have described a generalized coding algorithm based on shadow-casting which can minimize the useless pixels of m input radix p optical logic gate in case that m is not 2 N.

Theoretical analysis shows that the proposed coding method is superior to the previous publications in coding efficiency, therefore it is less susceptible to the diffraction effects and has relatively higher light efficiency.

By applying the proposed method, a generalized parallel optical logic processor such as adder, subtracter can also be realized. This work is now under way.

In order to illustrate the effectiveness of the proposed algorithm, several logic operations are performed for three binary input of $\delta*\delta$ data, and output results are presented.
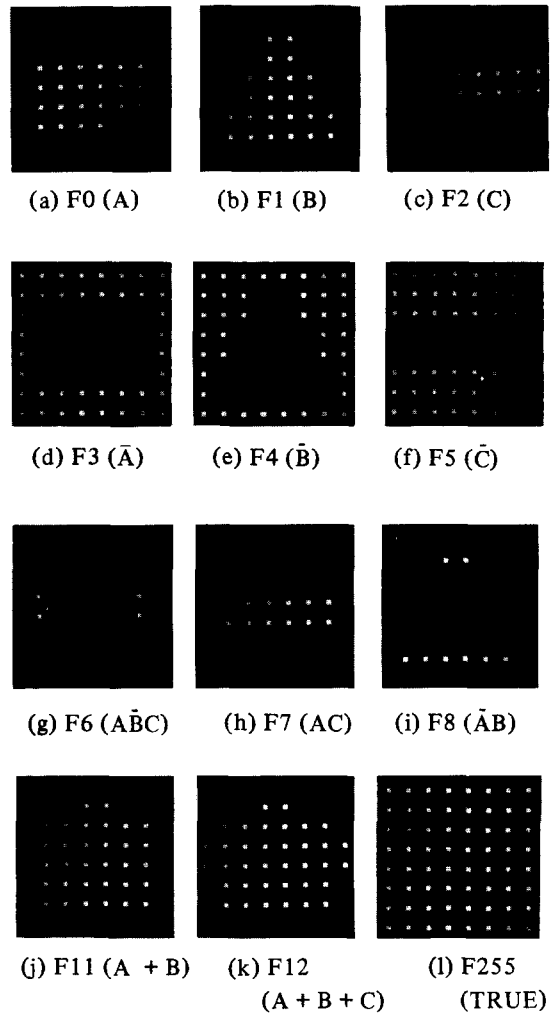
References

[1] D.R. Maure, "Optical Logic Function Generator," U.S. Patent, 3, 680, 080 July, 25, 1972.

[2] J. Tanida and Y. Ichoka, "Optical logic array processor using shadowgram," *J. Opt. Soc. Am.*, vol. 73, no. 6, pp. 800-809, June 1983.

[3] Y. Ichioka and J. Tanida, "Optical Parallel logic gate using a shadow-casting system for optical digital computing," *Proc. of the IEEE*, vol. 72, no. 7, pp. 787-801, July 1984.

[4] S. Kozaitis and R. Arrathoon, "Shadow-casting for direct table look-up and multiple-valued logic," *Appl. Opt.*, vol. 24, no. 20, pp. 3312-3314, Oct. 1985.

[5] R. Arrathoon and S. Kozaitis, "Shadow-casting for multiple-valued associative logic," *Opt. Eng.*, vol. 25, no. 1, pp. 29-37, Jan. 1986.

[6] Y. Li, G. Eichman and R.R. Alfano, "Optical Computing using hybrid encoded shadow casting," *Appl. Opt.*, vol. 25, no. 16, pp. 2636-2638, Aug. 1986.

[7] M.A. Karim, A.A.S. Awwal and Abdallah K. Cherri, "Polarization-encoded optical shadow-casting logic units: design," *Appl. Opt.*, vol. 26, no. 14, pp. 2720-2725, July 1987.

[8] Won Hyun Koun, "A study on the optical logic gate circuits using LED array," M.S. Thesis, Yonsei University, 1985.

[9] Do Hyung Choi, "A study on a shadow-casting method for optical computing," M.S, Thesis, Yonsei University, 1988.
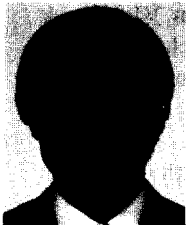
─────────── 著 者 紹 介 ───────────

崔 道 亨(正會員)
1963年 3月 20日生. 1986年 2月 연세대학교 전자공학과 졸업 공학사. 1988年 2月 연세대학교 대학원 전자공학과 졸업 공학석사학위 취득. 1988年 3月~현재 삼성반도체통신 연구원.

●

權 元 鉉(正會員)
1962年 8月 10日生. 1983年 2月 연세대학교 전자공학과 졸업 이학사. 1985年 2月 연세대학교 대학원 졸업 공학석사. 1986年 2月~현재 연세대학교 대학원 박사과정.

朴 漢 奎(正會員)
1941年 6月 21日生. 1964年 2月 연세대학교 전기공학과 (약전) 졸업. 1968年 7月 연세대학교 대학원 전기공학과 졸업. 1973年 10月 Paris VI Univ. (Sorbonne Univ.) 석사과정 수료(DEA). 1975年 7月 Paris VI Univ. 전자공학박사 학위 취득. 1974年 1月 불란서 국립 통신연구소(CNET)연구원, 미국 광학회(OSA), IEEE, Senior Member. 현재 연세대학교 전자공학과 교수. 주관심분야는 광컴퓨팅, 광통신, 광신호처리, 안테나 및 레이다신호처리 등임.