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Design of Dynamic NMOS Shift Register Used for Image Sensor

(Image Sensor에 사용되는 Dynamic NMOS Shift Register의 설계)

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要 約

Image sensor에서 주사 회로로 사용할 수 있는 shift register의 회로와 layout을 제시하였다. 이 회로가 정상적인 동작을 할 수 있는 p-well의 농도와 그에 따른 threshold voltage를 계산하였다. 최대의 동작 주파수를 계산하는 과정을 보이고, 이 회로에서 13MHz까지 threshold voltage loss가 없는 출력을 얻을 수 있음을 SPICE 모의 실험을 통하여 확인하였다.

Abstract

This paper describes the circuit and the layout of the shift register which can be used for a scanner of image sensor. P-well concentration and threshold voltage for proper operation are calculated on the basis of the fixed process and the layout design. The calculation procedure of maximum operation frequency is also carried out. It is ascertained by SPICE simulation that the shift register produces the output pulse without threshold voltage loss up to 13 MHz.

I. Introduction

Shift registers have been widely used in ICs since those operate relatively well in spite of large variation in the value of device parameters. A serial shift register has the simplest structure that can shift serial data. This paper will describe the design approach of an NMOS dynamic shift register to be used for the signal reading from pixels of image sensor.

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Starting from the discussion of the circuit and operation of a shift register in section II, we will show p-well concentration and threshold voltage in section III. Finally we will ascertain the operation of the shift register by means of SPICE simulation in section IV.

II. Circuit and Operation

Fig. 1 shows the circuit of an NMOS dynamic shift register composed of an input circuit and a unit stage. This shift register can be used for gating during sequential reading of video signals from image sensor. The features of shift register are to be designed by using: 1) a bootstrap to obtain the output voltage at each stage as high as the pulse height of clocks

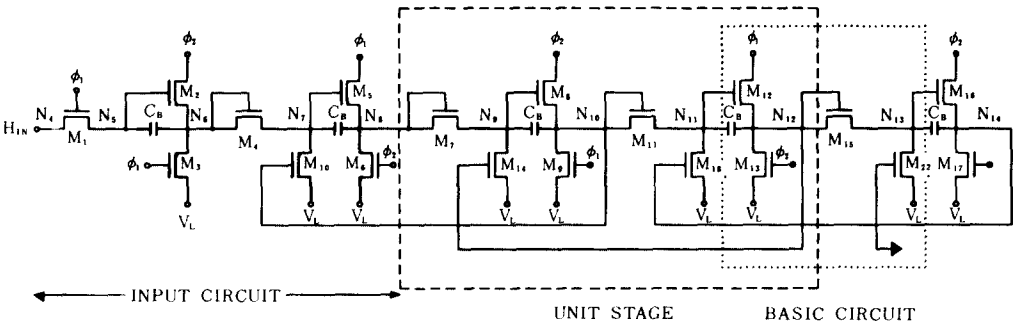

Fig. 1. Shift Register Circuit. ϕ_1 and ϕ_2 Stand for Clock Signals. V_L Denotes the Low Level Voltage of ϕ_1 and ϕ_2. The Outputs of the Input Circuit and the Unit Stage Can be Obtained at N_8 and N_{12} Respectively.

and to reduce the FPN (fixed pattern noise), 2) clock pulses to drive the shift register without power lines, 3) a n + pn structure to prevent from blooming phenomena [1] and cross-talking between sensor array and read-out circuit [2]. A unit stage consists of eight MOS transistors: the charging transistors (M_8, M_{12}), the discharging transistors (M_{14}, M_{18}), the pass transistors (M_7, M_{11}), the current path transistors (M_9, M_{13}) in charging and discharging capacitor C_B. The transistors M_2, M_3 and M_4 are used to make the output at node N_8 same as the output at node N_{12}. The capacitors in the circuit are used for bootstrapping.

One of the characteristics of MOSFET is that the source voltage to ground V_S is at most $V_G - V_T$ under ON condition where V_G is the gate voltage to ground and V_T is the threshold voltage. A bootstrap circuit is frequently adopted to compensate this threshold voltage loss and the resulting speed reduction [3].

Fig. 2. shows the bootstrap circuit with a MOSFET, a bootstrap capacitor C_B and a parasitic capacitor C_P. The gate voltage difference $\triangle V_G$ in the circuit is expressed with the source voltage difference $\triangle V_S$ which arises from the change of drain voltage to ground V_D.

$$\triangle V_G = \frac{C_B}{C_B + C_P} \triangle V_S \qquad (1)$$

If the initial voltage charged in the bootstrap capacitor is greater than V_T, V_S increases from V_L, and V_G will be

$$V_G = V_{GO} + K \triangle V_S \qquad (2)$$

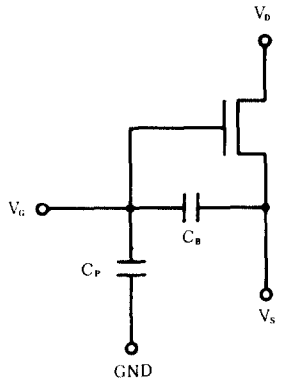

Fig. 2. A Bootstrap Circuit With a MOSFET, a Bootstrap Capacitor and a Parasitic Capacitor.

where V_{GO} is the initial value of V_G and $K = C_B/(C_B + C_P)$. The final value of V_G can be obtained from the following equation,

$$V_G = V_S + V_T = V_S + V_{TO} + \gamma \left[(2\Psi_B - V_B)^{1/2} - (2\Psi_B)^{1/2} \right] \qquad (3)$$

where V_B is the potential difference between source and substrate, V_{TO} is the V_T when $V_B = 0$, γ is the body effect constant and Ψ_B is the potential difference between intrinsic energy level and bulk Fermi level. V_S can be equal to V_D without threshold voltage loss if $V_D = V_S = -V_B$ and $(V_G - V_S) > V_T$. Driving pulse is composed of ϕ_1 and ϕ_2, and initial pulse H_{IN} is given to the input circuit.

Fig. 3 shows the timing diagram for the voltage of each node in input circuit. In phase I, C_1 is charged to high and M_2 turns on, since H_{IN} and ϕ_1 are high. While ϕ_2 is high, $C_2$is. charged to high and M_5 is at ON in phase II. N_5 becomes higher at this time. When ϕ_1 is high in phase III, Output is high and C_3 is charged to high. N_7 is also higher. As ϕ_2 is high, M_{10} turns on and N_7 is discharged to low in phase IV. As understood in the operation, an input pulse is transfered to next stage during one period of clock pulses to act as a shift register. It should be noted that the output level can be equal to that of clock pulse since a bootstrap circuit is used.

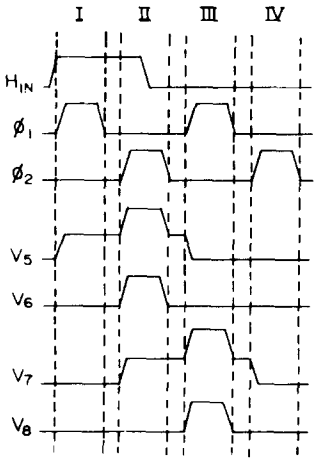

Fig. 3. Timing Diagram for the Voltage of Each Node in Input Circuit. V_5, V_6, V_7 and V_8 are the Voltages at N_5, N_6, N_7, N_8 in the Input Circuit Shown in Fig. 1.

III. P-well Concentration and Threshold Voltage

Fig. 4 shows the layout of the basic circuit surrounded by the dotted line in Fig. 1. The area occupied by a unit stage is approximately 23 x 700um.^{2} There are MOS capacitors parasitic capacitors and resistors, and NMOS transistors.

In the circuit the critical transistors in the sense of speed are the charging transistors (M8 and M12) and the pass transistors (M7, M11). All other transistors are designed to have the channel width (W) of 6um and the channel length (L) of 3um using the minimum feature size to save chip area. The channel length of pass transistor is chosen to be 4um in order not to cause the punch-through for the p-well concentration of 3.0E15/cm and the source-drain voltage of 5V (see section II). The channel width of charging transistors and pass transistors and pass transistors is taken to be 24um becauses the shift register has to operate at 13MHz.

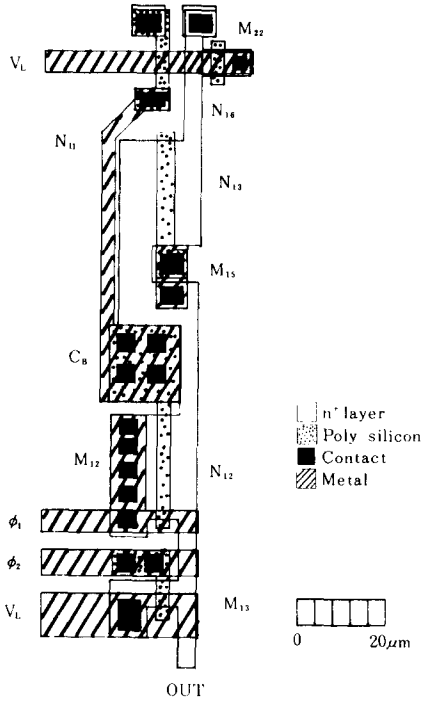

Fig. 4. Layout of the Basic Circuit Shown in Fig. 1.

A. Capacitances and Resistances

The bootstrap capacitor C_B with the structure of poly silicon/380Å oxide/n^+ silicon as well as the gate capacitor C_G has the unit area capacitance of 90.87 nF/cm^2. The capacitances of various field capacitors are calculated to the values of 6.91 nF/cm^2, 2.88 nF/cm^2, 4.933 nF/cm^2 and 4.933 nF/cm^2 depending on the capacitor structures (a)-(d) shown in Fig. 5.

The juction capacitance per unit area (n^+ layer/p-well) is estimated using the following equation:

$$C_J = \frac{1}{2}\left[\frac{2q\epsilon_{Si}N_A}{\phi_i - V}\right]^{1/2} \tag{4}$$

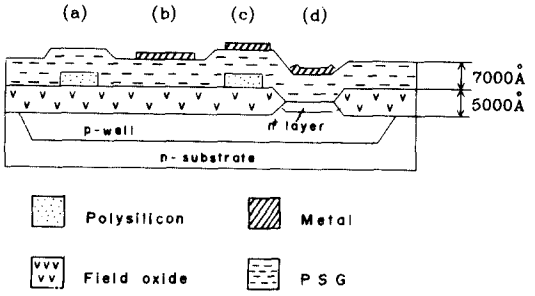

Fig. 5. Each Field Capacitor Structure for an Applied Process.

where q, ϵ_{Si}, N_A, ϕ_i and V are an electron charge, the permittivity of silicon, p-well concentration, the contact potential and applied voltage respectively. The applied voltage is about 1. 1Volt which is the low level voltage of the clock. The perimeter capacitance per unit length of the junction capacitor can be expressed as $C_{JP} = \pi \times C_J \times X_J/2$. The junction depth X_J is assumed as 0.25um for the calculation. The concentration of n+ layer ($1 \times 10^{20}/cm^3$) is very high compared with the concentration of p-well ($\sim x\, 10^{15}/cm^3$). It is neglected in the calculation of C_J and C_{JP}. The lateral diffusion length is taken as the same value of X_J[4].

The sheet resistances of n^+ diffusion line, polysilicon line and metal line are assumed to be 35 Ω/□, 20 Ω/□ and 0.05 Ω/□ respectively. Total parasitic capacitances C_1 and C_2 in Fig. 7 are obtained by summing junction capacitances, gate capacitances of MOS transistors and field capacitances. Total parasitic resistances R_1, R_2 and R_3 in Fig. 7 are also obtained by summing resistances of all the paths [4,5,6].

B. Threshold Voltages

The p-well concentration is mainly concerned to threshold voltage after fixing oxide thickness. The threshold voltage can be freely controlled by ion implantation. However, the high concentration of p-well increasees C_1 and the low concentration causes the punchthrough between source and drain of MOS transistor. To obtain the output level of each stage same as the high level of clock pulse without threshold voltage loss, the circuit must satisfy the next equation for 7V operation:

$$V_{GO} + \frac{C_B}{C_B + C_1} \Delta V_O - 7 \geq V_{TO} + \Delta V_T \tag{5}$$

where ΔV_O is the difference between the low and high level of output signal. The shift register also has to meet the following condition to maintain the repetition of operation through all stages.

$$V_O \geq V_{GO} + \Delta V_T + V_{TO} \tag{6}$$

where V_O is the high level output voltage.

If T_{OX} is fixed as 380Å for a given N_A, V_{TO} can be calculated using equation (5) and (6). The lower bound of N_A is taken as $2 \times 10^{15}/cm^3$ by considering the punchthrough between source and drain of pass transistors when source-drain voltage, built-in voltage and effective channel length are 5V, 0.9V and 3.2um respectively. Since V_{TO} greater than 0.5V is easily controlled, the upper bound of N_A is determined by taking V_{TO} as 0.5V. The values are $1.64 \times 10^{16}/cm^3$ for 7V operation and $8.2 \times 10^{15}/cm^3$ for 5V operation when threshold voltage is 0.5V. The results are shown in Fig. 6.

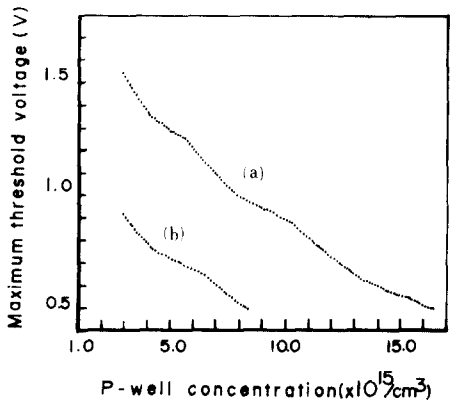

Fig. 6 A Plot for the Maximum Threshold Voltage Depending on p-well Concentration (a) for 7V Operation and (b) for 5V Operation.

C. The Calculation of Maximum Operation Frequency

The maximum operation frequency f_M in

worstcase can be approximately calculated considering the charging and discharging time of the bootstrap capacitor [8].

a) Charging time

Fig. 7(a) shows the charging and discharging circuit with the parasitic capacitors (C_1, C_2), the parasitic resistors (R_1, R_2 and R_3) and the bootstrap capacitors (C_B) [5, 7]. The equivalent resistors R_4, R_5 and R_6 to each channel resistance of M_8, M_{11} and M_{13} are used to calculate the charging time of the bootstrap capacitor in Fig. 7(b) where C_3 is given by $C_1C_B/(C_1 + C_B)$, R_7 is $R_5 + R_1$ and R_8 is $R_3 + R_6$. The resistance values (R_4, R_5 and R_6) are calculated from the DC characteristic curves of SPICE simulation assuming that the transistors are operating in saturation region.

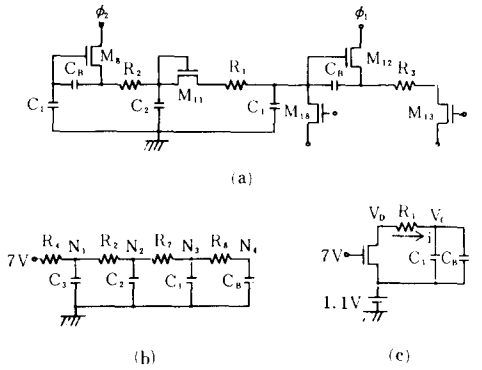

Fig. 7. The Charging and Discharging Part of the Shift Register (a). The Equivalent Circuits (b) and (c) for Calculating the Charging and the Discharging Time.

The current equations at node a,b,c,d in Fig. 7(b) can be written as follows.

$$\frac{V_1 - 7}{R_4} + C_3\frac{dV_1}{dt} + \frac{V_1 - V_2}{R_2} = 0 \qquad (7a)$$

$$\frac{V_2 - V_1}{R_2} + C_2\frac{dV_2}{dt} + \frac{V_2 - V_3}{R_7} = 0 \qquad (7b)$$

$$\frac{V_3 - V_2}{R_7} + C_1\frac{dV_3}{dt} + \frac{V_3 - V_4}{R_8} = 0 \qquad (7c)$$

$$\frac{V_4 - V_3}{R_8} + C_B\frac{dV_4}{dt} = 0 \qquad (7d)$$

The voltage V_3 at N_3 is calculated using the Laplace transformation where the initial charges in C_B are assumed to be zero. The rising time T_1 of V_3 can be regarded as the charging time of the bootstrap capacitor.

b) Discharging time

Fig. 7(c) shows the circuit used in calculating the discharging time of the bootstrap capacitor. The charges in C_1 and C_B are discharged through R_1 and M_{18}. The current in Fig. 7(c) can be written as the equations (8) and (9).

$$(C_1 + C_B)\frac{dV_C}{dt} = \frac{V_D - V_C}{R_1} \qquad (8)$$

$$\frac{V_D - V_C}{R_1} = -\beta\left[(7\text{-}1.1\text{-}V_T)(V_D - 1.1) - \frac{1}{2} \times (V_D - 1.1)^2\right] \qquad (9)$$

After separating variables and integrating, the time T_2 which V_D falls from 4.9V to 1.1V is calculated and regarded as the discharging time of the bootstrap capacitor for 7V operation, where 4.9V is determined by SPICE simulation at V_{TO} = 1.4V. The maximum operation frequency is $1/(2(T_1+T_2))$ since the clock pulse width must be at least $T_1 + T_2$. Taking N_A as $3.5 \times 10^{15}/cm^3$ and using the various parameters listed in Table 1, the maximum operation frequency f_M is about 14MHz.

IV. SPICE Simulation

The operation of the shift register is assured

Table 1. The Values of Capacitances and Resistances Used for the Calculation of T_1 and T_2

resistance (KΩ)	resistance (KΩ)	capacitance (pF)
R_1 0.616	R_5 42.170	C_B 0.334
R_2 0.560	R_6 1.730	C_1 0.126
R_3 0.560	R_7 42.800	C_2 0.254
R_4 26.470	R_8 2.300	C_3 0.092

by SPICE simulation. The equivalent circuit used for the simulation is shown in Fig. 8[7]. The process parameters used for the simulation are shown in Table 2.

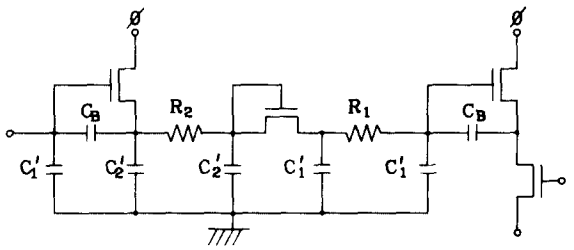

Fig. 8. Equivalent Circuit for SPICE Simulation. C_1' and C_2' are $(C_1-C_G)/2$ and $(C_2-C_G)/2$ Respectively.

Table 2. Process Parameters Used for the SPICE Simulation.

parameter	value
zero bias threshold voltage	1.4V
n^+ diffusion sheet resistance	35Ω/□
oxide thickness	380 Å
p-well concentration	$3.5\times10^{15}/cm^3$
S/D junction depth	0.25μm
lateral diffusion	0.2μm
surface mobility	$580cm^2/V\text{-}sec$

The rising or falling time of input pulse and driving clock signal is 15ns for 7.2MHz and 5ns for 13MHz. Since Fig. 9 shows the output pulses without threshold voltage loss at 7.2MHz and 13MHz, the shift register operates properly as we expected. The operations of the shift register at upper bound conditions are also made sure by the simulation; the upper bound conditions for N_A, V_{TO} and clock frequency are $1.64\times10^{16}/cm^3$, 0.5V, 13MHz for 7V operation and $8.2\times10^{15}/cm^3$, 0.5V, 10MHz for 5V operation.

V. Conclusions

We proposed the circuit and the layout of the dynamic NMOS shift register which can be used for reading the signals from image sensors. V_{TO} depends upon the p-well concentration. The upper bounds of N_A are $1.64\times10^{16}/cm^3$ for 7V operation and $8.2\times10^{15}/cm^3$ for 5V operation. The lower bound of N_A is $2\times10^{15}/cm^3$. SPICE assures that the maximum operation frequencies on the upper bound conditions are 13 MHz for 7V operation and 10 MHz for 5V operation. It also shows that the output pulse is the same as clock pulse without threshold voltage loss. The ranges of p-well concentrations and threshold voltages for proper operation are calculated and shown in Fig. 6.

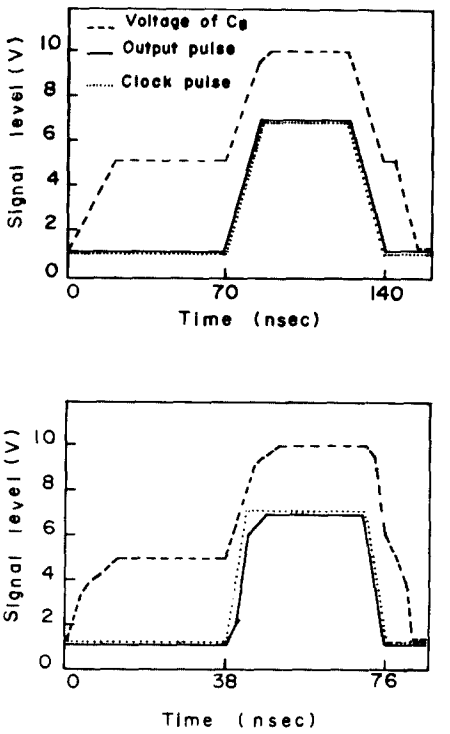

Fig. 9. SPICE Simulation Results: (a) at 7.2 MHz and (b) at 13 MHz.

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