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A Study on the Method for Evaluating the Signal Reliability of Digital System

(디지탈 계통의 신호적 신뢰도 계정 방법에 관한 연구)

高 瓊 植*, 吳 英 煥**

(Kyung Shik Koh and Young Hwan Oh)

要 約

디지탈 회로에 있어서는 그 내부에 결함이 존재할 때에도 올바른 출력 신호를 낼 수가 있는데, 이와같이 결함 유무에 불구하고 올바른 출력을 내는 확률을 신호적 신뢰도라고 한다. 본 논문에서는 신호적 신뢰도에 대해서 해석하고, 다음에 새로운 신호적 신뢰도 계정 방법을 제안하였다. 이 방법은 신뢰도 계정에 있어서의 계산을 간소화시키고 기계적인 처리가 가능하다.

Abstract

It is known that digital circuits may produce correct output signals even when some faults are present in them. A reliability measure, known as signal reliability, is the probability that the circuit output is correct. In this paper, the reliability measure is analyzed first and a new procedure for evaluation of the signal reliability is presented. This procedure simplifies signal reliability calculations and can easily be mechanized.

I. Introduction

The reliability of digital circuits can be evaluated using two different measures. The first measure is the functional reliability which means the probability that the circuit realizes the desired design function. The second measure is the signal reliability which means the probability that the circuit output is correct. The functional reliability measure assumes that the circuit fails whenever a fault is present in it. But it is known that a digital circuit may produce correct output signal even when some faults are present in it. Lately, some authors have introduced the methods for the evaluation of the signal reliability.[1-5] [10]

In this work a different approach to the evaluation of signal reliability is presented. The method derives functional description of each output of the circuit, which also represent the structure of the circuit. In order to include the effect of faults in the function realized by a circuit, three state variables are used to specify the state of each line in the circuit. This method evaluates the signal reliability in a recursive way.

*正會員, 仁荷大學校 電子工學科
(Dept. of Elec. Eng., Inha Univ.)
**正會員, 光云大學校 電子工學科
(Dept. of Elec. Eng., Kwang Woon Univ.)
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II. Preliminaries

The reliability of a logical circuit depends upon the possible failures and their probabilities of occurrence. We assume that the possible

failures are multiple lead failures of stuck-at type, i.e., any line X in the circuit may be stuck at one (s-a-1) or stuck at zero (s-a-0). Each line may take one of three states-normal, stuck at one, or stuck at zero. The variables are defined for these three states as follows:

$N_x = 1$: iff line X is normal
$F_x = 1$: iff line X is s-a-1
$f_x = 1$: iff line X is s-a-0

We note that the three states are disjoint, therefore

$$F_x' = N_x + f_x$$
$$f_x' = N_x + F_x$$

In terms of these variables, the proposition Px, which represents the totality condition under which the line X can have a signal value 1, is

$$P_x = X N_x + F_x$$

where X is the input proposition for the line X. What this says is that the line X will have a signal value 1 if X=1 and line X is fault-free or if the line X is s-a-1. The above expression Px is called P-operation on line X. Similarly, the totality condition under which the line X can have a signal value 0 is represented by the proposition

$$P_x' = X' N_x + f_x$$

which means that the line X have a value 0 if X=0 and line X is fault-free or if line X is s-a-0. The expression Px' is called P'-operation on line X. Next, we will give some definition relevant to the following discussions [1].

Definition: The signal reliability of a circuit is the probability that the logical output of the circuit is correct for every normal input.

Definition: Let Gn be the output proposition of the normal circuit G, and G_f be the output proposition of the circuit with faluts. Then the function $H=(Gn \oplus G_f)'$, and $E=G_n \oplus G_f$ are called signal reliability function and signal unreliability function of the circuit G respectively.

The signal reliability function is expressed as follows:

$$H = (G_n \oplus G_f)' = G_n G_f + G_n' G_f' = H_1 + H_0$$

where $H_1=G_n G_f$ and $H_0=G_n' G_f'$. Since $(G_n G_f)$ and $(G_n' G_f')$ are disjoint, the probability of H is the sum of probability that G_n is a 1 and G_f is also a 1, and the probability that G_n is a 0 and G_f is also equal to 0.

Similary, the signal unreliability function is expressed as follows:

$$E = G_n \oplus G_f = G_n G_f' + G_n' G_f = E_1 + E_0$$

where $E_1=G_n G_f'$ and $E_0=G_n' G_f$. Since $(G_n' G_f)$ and $(G_n G_f')$ are also disjoint, the pobability of E is the sum of probability that $G_n=1$ and $G_f=0$, and the probability that $G_n=0$ and $G_f=1$. In the next section we present a procedure for evaluating the signal reliability using a very simple example.

III. Signal Reliability of a Combinational Circuit

As an example for deriving signal reliability function, we consider an AND gate of Figure 1. having two inputs X and Y and its output Z.

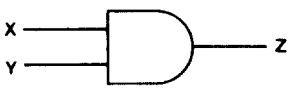

Fig. 1. An example AND gate circuit.

For simplicity we use the same letter for each line of the gate as its logical variable. Based on the discussion above, the proposition Pz and Pz' of the totality of conditions under which line Z can have a signal 1 and 0 are represented by

$$P_z = (P_x P_y) N_z + F_z$$
$$P_z' = (P_x' + P_y') N_z + f_z$$
$$= (P_x' + P_x P_y') Z_n + f_z$$

respectively, where

$$P_x = X N_x + F_x$$
$$P_x' = X' N_x + f_x$$
$$P_y = Y N_y + F_y$$
$$P_y' = Y' N_y + f_y$$

The signal reliability function of AND gate is determined by developing H_1-function and H_0-function as follows.

$$\begin{aligned} H_1 &= G_n G_f = (XY) P_z \\ &= XY [(X N_x + F_x)(Y N_y + F_y) N_z + F_z] \\ &= XY [(N_x + F_x)(N_y + F_y) N_z + F_z] \\ &= XY (f_x' f_y' N_z + F_z) \end{aligned}$$

$$\begin{aligned} H_0 &= G_n' G_f' = (XY)' P z' \\ &= (X' + Y') [(P_x' + P_y') N_z + f_z] \\ &= (X' + XY') [(P_x' + P_x P_y') N_z + f_z] \\ &= (X' + XY') [[(X' N_x + f_x) + (X N_x + F_x) \\ &\quad (Y' N_y + f_y)] N_z + f_z] \\ &= X' [[F_x' + F_x (Y' N_y + f_y)] N_z + f_z] \\ &\quad + XY' [[(f_x + f_x' F_y'] N_z + f_z] \end{aligned}$$

Here we will use the conventions that K_n, K_1, and K_0 correspond to the probabilities of the state variables N_k, F_k and f_k, and that lower case letters represent the probabilities of input signals. Then signal reliability of AND gate is

$$\begin{aligned} P_r[H] &= P_r[H_1] + P_r[H_0] \\ &= xy [(1-X_0)(1-Y_0) Z_n + Z_1] \\ &\quad + (1-x) [[(1-X_1) + X_1 ((1-y) Y_n + \\ &\quad Y_0)] Z_n + Z_0] \\ &\quad + x(1-y) [[X_0 + (1-X_0)(1-Y_1)] \\ &\quad Z_n + Z_0] \end{aligned}$$

If we assume that the probability of a fault occurring is the same for all lines, i.e., $X_1=X_0=Y_1=Y_0=Z_1=Z_0=s/2$, and the probability of a signal is the same for all input lines, i.e., $x=y=z=1/2$, the signal reliability is further simplified as follows.

$$\begin{aligned} P_r[H] = &\ 1/4 [(1-s/2)^2 (1-s) + s/2] \\ &+ 1/2 [[(1-s/2) + s/4] (1-s) + s/2] \\ &+ 1/4 [[s/2 + (1-s/2)^2] (1-s) + s/2] \\ = &\ 1 - s + 5s^2/8 - s^3/8 \end{aligned}$$

We note the result that the signal reliability of an AND gate is 50 percent even when a fault always exists on every line ($s=1$).

The signal reliability can be determined by developing signal unreliability function, but almost the same amount of calculation is required.

We have discussed the procedure for evaluating the signal reliability of a combinational logic circuit by basic AND gate. This procedure can be applied to a general combinational network. We will give the algorithm for producing signal reliability expression of a general network in the next section.

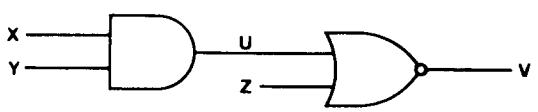

Fig. 2. Illustrating example circuit.

IV. Algorithm for Derivation of Disjoint Form of H_1 (or H_0) Function

Algorithm:

1) Find the minimal disjoint form of output function of normal circuit G_n (or G_n') using sum of products of input variables.

2) Find the output funciton of the circuit with faults G_f (or G_f') using path-sensitizing form.

3) Obtain the product of G_n (or G_n') and G_f (or G_f').

In this step, the following relations are used:

$$X P_x = X f_x', \quad X P_x' = X f_x$$
$$X' P_x = X' F_x, \quad X' P_x' = X' F_x'$$

4) Transform the above expression into disjoint form and perform P- and P′-operation.

Illustrating Example:

Consider the circuit shown in Figure 2.

A. Derivation of the minimal disjoint form of H_1-function.

1) $G_n = (XY + Z)' = X'Z' + Y'Z' = X'Z' + XY'Z'$

2) $G_f = [(P_x P_y)u + P_z]'v = [(P_x' + P_y')u' P_z']v$

3) $H_1 = X'Z'[(P_x' + P_y')u' P_z']v + XY'Z'[(P_x' + P_y')u' P_z']v$
$= X'Z'[(F_x' + P_y')u' F_z']v + XY'Z'[(f_x + F_y')u' F_z']v$

4) $H_1 = X'Z'[[(F_x' + F_x P_y')N_u + f_u] F_z' N_v + F_v] + XY'Z'[[(f_x + f_x' F_y')N_u + f_u] F_z' N_v + F_v]$

B. Derivation of the minimal disjoint form of H_0-function

1) $G_n' = XY + Z = Z + XYZ'$

2) $G_f' = [[(P_x P_y)u + P_z]'v]' = [(P_x P_y)u + P_z]v'$

3) $H_0 = Z[(P_x P_y)u + P_z]v' + XYZ'[(P_x P_y)u + P_z]v' = Z[(P_x P_y)u + f_z']v' + XYZ'(f_x' f_y')u + F_z]v'$

4) $H_0 = Z[[(P_x P_y N_u + F_u)f_z + f_z']N_v + f_v] + XYZ'[[(f_x' f_y' N_u + F_u)F_z' + F_z]N_v + f_v]$

If we assume that the probability of a fault occuring is the same for all lines, i.e., $X_1 = X_0 = Y_1 = Y_0 = Z_1 = Z_0 = s/2$, and the probability of a signal is the same for all input lines, i.e., $x = y = z = 1/2$, the signal reliability is further simplified as follows.

$$\begin{aligned}\Pr[H] = {} & 1/4\,[[[(1-s/2)+s/4](1-s)+s/2](1-s/2)(1-s)+s/2] \\ & + 1/8\,[[[(s/2+(1-s/2)^2](1-s)+s/2](1-s/2)(1-s)+s/2] \\ & + 1/2\,[[[1/4(1-s)+s/2]s/2 + (1-s/2)](1-s)+s/2] \\ & + 1/8\,[[[(1-s/2)^2(1-s)+s/2](1-s/2)+s/2](1-s)+s/2] \\ = {} & 1-11s/8+3s^2/2-27s^3/32 + s^4/4-s^5/32\end{aligned}$$

V. Conclusion

Generally the evaluation of signal reliability of a digital system is very complex and difficult. Several methods have been proposed to reduce the calculations by now, but they were still not so efficient. In this paper, three binary variables are introduced to specify the state of each line in the circuit and, as a result, the calculations are lessend considerably. It seems that this method provides a new insight into the problem of digital system reliability.

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