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Fault Diagnosis of Multistage Baseline Network

(다단 베이스라인 네트워크의 오류진단)

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要 約

지금까지는 다단 상호 결합 네트워크에서 단일 스택 오류를 검출하고 위치를 찾기위해서는 4번의 테스트가 필요하였으나 본 논문에서는 3번의 테스트로써 필요 충분함을 보였다. 다단 상호 결합 네트워크에서 4개의 확실한 상태를 가지고 오류를 진단하는 방법을 제시하였으며 이 방법을 이용하여 단일 링크 오류와 스위칭 소자 오류를 찾는데는 $4\log_2 N+3$ 테스트가 요구되었다. 그리고 단일 오류의 위치와 유형을 찾는 과정을 예제로써 나타냈으며 확실치 않는 부분의 위치를 찾을 수 없는 확률을 보였다.

Abstract

It was shown previously that four tests are required in order to detect single fault and to locate single link stuck fault for a class of multistage interconnection networks. In this paper, we show that only three tests are necessary and sufficient both to detect single fault and to locate single link stuck fault. A fault diagnosis method with four valid state for a class of multistage interconnection networks is presented.

Using this method, all single link stuck fault or all single switching element faults, can be detected by at most $4\log_2 N+3$ tests. In the example, the location and type of single fault are pinpointed, and unlocatable probabilities of questionable regions are given.

I. Introduction

Advances and decreasing cost of VLSI circuit encourage to have a larger number of processing elements to be included in highly parallel processor system. In these systems, various techniques are utilized in implementing restructurable data paths between processing units and memory modules. Recently, Multistage interconnection networks are used in providing programmable data paths between functional modules in multiprocessor systems. The multistage interconnection network are usually segmented into several stages, and the linkages between various stages are assigned so that any input can access any one of the outputs.

Each stage connects inputs to appropriate links of the next stage so that the cumulative effect of all stages satisfies input-output connection requirements.

Several such networks have been described in the literature[6-9,12,14] and various issues related to these networks have recently been addressed[1,2,5,15,16]. But, not much attention has been paid to the fault-diagnosis of these networks.

The reliability aspect is important for successful operation of a computing system and the interconnection networks being the heart of a parallel processing system[3], their fault-diagnosis becomes extremely important. The fault-diagnosis for a class of rearrangeable

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switching has been described by Opferman and Tsao-Wu[11]

They have used 2-input, 2-output switches as basic building blocks and they utilize test permutations to check for the possible two states of each switching element.

In this way, they consider faulty state of a switching element to be unalterable parallel or cross-connection of the switch. Wu and Feng[17] have introduced their fault model by illustrating 16 possible states of 2x2 switch. They consider only two of them to be allowable states and the remaining 14 states are assumed as a faulty situation. In their novel approach, they keep all the switches in one state and then all of them in the second state and at each state, they require only two input test sequences.

Their effective of 1-out of-2 code is demonstrated by the fact that they require a total of only 4 tests for a network at any size. But this paper is to show that only tests are actually necessary and sufficient to detect and locate such faults.

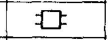
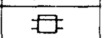
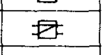
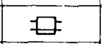
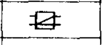
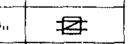
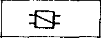
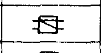
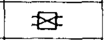
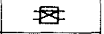
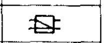
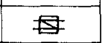
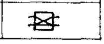
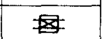
A fault diagnosis method for the multistage interconnection network with four valid states is presented. It is more complicated than any previous methods, because there are 16^4 state combinations for each 4 valid state element as compared with 16^2 state combinations for 2 valid state element, and only one out of 16^4 state combination is fault-free, the others are faulty. It is shown in the example that location and type of single fault are pinpointed, and unlocatable probabilities of questionable region are given.

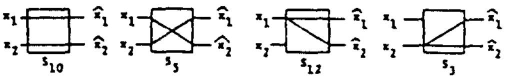
II. Fault Models and Test Sets

In a multistage interconnection networks, each switching element has 16 possible states as shown in Table 1. Four of 16 states are considered as valid state i.e., straight s_{10}, exchange s_5, lower broadcast s_{12}, and upper broadcast s_3 as shown in Fig. 1.

Each faulty link, a faulty switching element can cause fault (s) in an interconnection networks. The fault of a link may be one of two kinds of link stuck faults: stuck-at-zero and stuck-at-one. Moreover, when a switching elements is at a valid state, the other 15 states are considered faulty states.

Table 1. Set of 16 states and relative logical symbols of a 2 × 2 switching element.

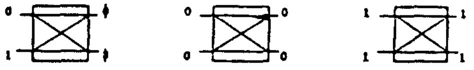
State name	Logical symbol	State name	Logical symbol
s_0		s_8	
s_1		s_9	
s_2		s_{10}	
s_3		s_{11}	
s_4		s_{12}	
s_5		s_{13}	
s_6		s_{14}	
s_7		s_{15}	



x_1 : Upper input $\hat{x}_1$: Upper output
x_2 : Lower input $\hat{x}_2$: Lower output

Fig. 1. A switching element with four valid states.

In an interconnection network with 4 valid states, the fault models of a switching element are shown in Table 2, 3, 4 and 5. In these Tables, "*" is a kind of stuck output responses coming from a stuck link; "–" is another kind of stuck output responses coming from a faulty switching element, in which there is no logical connection between a certain input and output; "ϕ" is an indeterminate output response coming from a faulty switching element, in which an output connects with both inputs at the same time. It is not a stuck faulty output response like * and –, but can be changed when the inputs are at different input test combinations as shown in Fig. 2. In order to detect a single fault, only two kinds of test vectors are needed: t=(0, 1) and $\bar{t}$=(1, 0). In this paper, additional test vectors are needed: t=1 or t=0.



ϕ : Indetermined(o or 1)

Fig. 2. The possible output responses of a ϕ type of fault element.

Table 2. The fault models of a switching element at S_{10}

Fault		Test		Output			
		x_1	x_2	Normal $\hat{x}_1$	$\hat{x}_2$	Faulty $\hat{x}_1$	$\hat{x}_2$
STUCK LINK	$x_1^*, \hat{x}_1^*$	0	1	0	1	*	1
		1	0	1	0	*	0
		0	0	0	0	*	0
		1	1	1	1	*	1
	$x_2^*, \hat{x}_2^*$	0	1	0	1	0	*
		1	0	1	0	1	*
		0	0	0	0	0	*
		1	1	1	1	1	*
SWITCHING ELEMENT FAULT	$S_{10}-S_0$	0	1	0	1	–	–
		1	0	1	0	–	–
		0	0	0	0	–	–
		1	1	1	1	–	–
	$S_{10}-S_1$	0	1	0	1	1	–
		1	0	1	0	0	–
		0	0	0	0	0	–
		1	1	1	1	1	–
	$S_{10}-S_2$	0	1	0	1	–	1
		1	0	1	0	–	0
		0	0	0	0	–	0
		1	1	1	1	–	1
	$S_{10}-S_3$	0	1	0	1	1	1
		1	0	1	0	0	0
	$S_{10}-S_4$	0	1	0	1	–	0
		1	0	1	0	–	1
		0	0	0	0	–	0
		1	1	1	1	–	1
	$S_{10}-S_5$	0	1	0	1	1	0
		1	0	1	0	0	1
	$S_{10}-S_6$	0	1	0	1	–	ϕ
		1	0	1	0	–	ϕ
		0	0	0	0	–	0
		1	1	1	1	–	1
	$S_{10}-S_7$	0	1	0	1	1	ϕ
		1	0	1	0	0	ϕ
		0	0	0	0	0	0
		1	1	1	1	1	1
	$S_{10}-S_8$	0	1	0	1	0	–
		1	0	1	0	1	–
		0	0	0	0	0	–
		1	1	1	1	1	–
	$S_{10}-S_9$	0	1	0	1	ϕ	–
		1	0	1	0	ϕ	–
		0	0	0	0	0	–
		1	1	1	1	1	–
	$S_{10}-S_{11}$	0	1	0	1	ϕ	1
		1	0	1	0	ϕ	0
		0	0	0	0	0	0
		1	1	1	1	1	1
	$S_{10}-S_{12}$	0	1	0	1	0	0
		1	0	1	0	1	1
	$S_{10}-S_{13}$	0	1	0	1	ϕ	0
		1	0	1	0	ϕ	1
		0	0	0	0	0	0
		1	1	1	1	1	1
	$S_{10}-S_{14}$	0	1	0	1	0	ϕ
		1	0	1	0	1	ϕ
		0	0	0	0	0	0
		1	1	1	1	1	1
	$S_{10}-S_{15}$	0	1	0	1	ϕ	ϕ
		1	0	1	0	ϕ	ϕ
		0	0	0	0	0	0
		1	1	1	1	1	1

Table 3. The fault models of a switching element at S_5

Fault		Test		Output			
		x_1	x_2	Normal $\hat{x}_1$	$\hat{x}_2$	Faulty $\hat{x}_1$	$\hat{x}_2$
STUCK LINK	$x_1^*, \hat{x}_2^*$	0	1	1	0	1	*
		1	0	0	1	0	*
		0	0	0	0	0	*
		1	1	1	1	1	*
	$x_2^*, \hat{x}_1^*$	0	1	1	0	*	0
		1	0	0	1	*	1
		0	0	0	0	*	0
		1	1	1	1	*	1
	S_5-S_0	0	1	1	0	–	–
		1	0	0	1	–	–
		0	0	0	0	–	–
		1	1	1	1	–	–
	S_5-S_1	0	1	1	0	1	–
		1	0	0	1	0	–
		0	0	0	0	0	–
		1	1	1	1	1	–
SWITCHING ELEMENT FAULT	S_5-S_2	0	1	1	0	–	1
		1	0	0	1	–	0
		0	0	0	0		0
		1	1	1	1	–	1
	S_5-S_3	0	1	1	0	1	1
		1	0	0	1	0	0
	S_5-S_4	0	1	1	0	–	0
		1	0	0	1	–	1
		0	0	0	0	–	0
		1	1	1	1	–	1
	S_5-S_6	0	1	1	0	–	ϕ
		1	0	0	1	–	ϕ
		0	0	0	0	–	0
		1	1	1	1	–	1
	S_5-S_7	0	1	1	0	1	ϕ
		1	0	0	1	0	ϕ
		0	0	0	0	0	0
		1	1	1	1	1	1
	S_5-S_8	0	1	1	0	0	–
		1	0	0	1	1	–
		0	0	0	0	0	–
		1	1	1	1	1	–
	S_5-S_9	0	1	1	0	ϕ	–
		1	0	0	1	ϕ	–
		0	0	0	0	0	–
		1	1	1	1	1	–
	S_5-S_{10}	0	1	1	0	0	1
		1	0	0	1	1	0
	S_5-S_{11}	0	1	1	0	ϕ	1
		1	0	0	1	ϕ	0
		0	0	0	0	0	0
		1	1	1	1	1	1
	S_5-S_{12}	0	1	1	0	0	0
		1	0	0	0	1	1
	S_5-S_{13}	0	1	1	1	ϕ	0
		1	0	0	0	ϕ	1
		0	0	0	0	0	0
		1	1	1	0	1	1
	S_5-S_{14}	0	1	1	1	0	ϕ
		1	0	0	0	1	ϕ
		0	0	0	0	0	0
		1	1	1	0	1	1
	S_5-S_{15}	0	1	1	1	ϕ	ϕ
		1	0	0	0	ϕ	ϕ
		0	0	0	0	0	0
		1	1	1	1	1	1

Table 4. The fault models of a switching element at S_{12}

Fault		Test		Output			
		x_1,	x_2	Normal $\hat{x}_1$,	$\hat{x}_2$	Faulty $\hat{x}_1$,	$\hat{x}_2$
STUCK LINK	x_1^*	0	1	0	0	*	*
		1	0	1	1	*	*
		0	0	0	0	*	*
		1	1	1	1	*	*
	x_2^*	0	1	0	0	0	0
		1	0	1	1	1	1
		0	0	0	0	0	0
		1	1	1	1	1	1
	$\hat{x}_1^*$	0	1	0	0	*	0
		1	0	1	1	*	1
		0	0	0	0	*	0
		1	1	1	1	*	1
	$\hat{x}_2^*$	0	1	0	0	0	*
		1	0	1	1	1	*
		0	0	0	0	0	*
		1	1	1	1	1	*
	$S_{12}-S_0$	0	1	0	0	–	–
		1	0	1	1	–	–
		0	0	0	0	–	–
		1	1	1	1	–	–
	$S_{12}-S_1$	0	1	0	0	1	–
		1	0	1	1	0	–
		0	0	0	0	0	–
		1	1	1	1	1	–
	$S_{12}-S_2$	0	1	0	0	–	1
		1	0	1	1	–	0
		0	0	0	0	–	0
		1	1	1	1	–	1
	$S_{12}-S_3$	0	1	0	0	1	1
		1	0	1	1	0	0
	$S_{12}-S_4$	0	1	0	0	–	0
		1	0	1	1	–	1
		0	0	0	0	–	0
		1	1	1	1	–	1
	$S_{12}-S_5$	0	1	0	0	1	0
		1	0	1	1	0	1
SWITCHING ELEMENT FAULT	$S_{12}-S_6$	0	1	0	0	–	ϕ
		1	0	1	1	–	ϕ
		0	0	0	0	–	0
		1	1	1	1	–	1
	$S_{12}-S_7$	0	1	0	0	1	ϕ
		1	0	1	1	0	ϕ
		0	0	0	0	0	0
		1	1	1	1	1	1
	$S_{12}-S_8$	0	1	0	0	0	–
		1	0	1	1	1	–
		0	0	0	0	0	–
		1	1	1	1	1	–
	$S_{12}-S_9$	0	1	0	0	ϕ	–
		1	0	1	1	ϕ	–
		0	0	0	0	0	–
		1	1	1	1	1	–
	$S_{12}-S_{10}$	0	1	0	0	0	1
		1	0	1	1	1	0
	$S_{12}-S_{11}$	0	1	0	0	ϕ	1
		1	0	1	1	ϕ	0
		0	0	0	0	0	0
		1	1	1	1	1	1
	$S_{12}-S_{13}$	0	1	0	0	ϕ	0
		1	0	1	1	ϕ	1
		0	0	0	0	0	0
		1	1	1	1	1	1
	$S_{12}-S_{14}$	0	1	0	0	0	ϕ
		1	0	1	1	1	ϕ
		0	0	0	0	0	0
		1	1	1	1	1	1
	$S_{12}-S_{15}$	0	1	0	0	ϕ	ϕ
		1	0	1	1	ϕ	ϕ
		0	0	0	0	0	0
		1	1	1	1	1	1

Table 5. The fault models of a switching element at S_3

Fault		Test		Output			
		x_1,	x_2	Normal $\hat{x}_1$,	$\hat{x}_2$	Faulty $\hat{x}_1$,	$\hat{x}_2$
STUCK LINK	x_1^*	0	1	1	1	1	1
		1	0	0	0	0	0
		0	0	0	0	0	0
		1	1	1	1	1	1
	x_2^*	0	1	1	1	*	*
		1	0	0	0	*	*
		0	0	0	0	*	*
		1	1	1	1	*	*
	$\hat{x}_1^*$	0	1	1	1	*	1
		1	0	0	0	*	0
		0	0	0	0	*	0
		1	1	1	1	*	1
	$\hat{x}_2^*$	0	1	1	1	1	*
		1	0	0	0	0	*
		0	0	0	0	0	*
		1	1	1	1	1	*
SWITCHING ELEMENT FAULT	S_3-S_0	0	1	1	1	–	–
		1	0	0	0	–	–
		0	0	0	0	–	–
		1	1	1	1	–	–
	S_3-S_1	0	1	1	1	1	–
		1	0	0	0	0	–
		0	0	0	0	0	–
		1	1	1	1	1	–
	S_3-S_2	0	1	1	1	–	1
		1	0	0	0	–	0
		0	0	0	0	–	0
		1	1	1	1	–	1
	S_3-S_4	0	1	1	1	–	0
		1	0	0	0	–	1
		0	0	0	0	–	0
		1	1	1	1	–	1
	S_3-S_5	0	1	1	1	1	0
		1	0	0	0	0	1
	S_3-S_6	0	1	1	1	–	ϕ
		1	0	0	0	–	ϕ
		0	0	0	0	–	0
		1	1	1	1	–	1
	S_3-S_7	0	1	1	1	1	ϕ
		1	0	0	0	0	ϕ
		0	0	0	0	0	0
		1	1	1	1	1	1
	S_3-S_8	0	1	1	1	0	–
		1	0	0	0	1	–
		0	0	0	0	0	–
		1	1	1	1	1	–
	S_3-S_9	0	1	1	1	ϕ	–
		1	0	0	0	ϕ	–
		0	0	0	0	0	–
		1	1	1	1	1	–

Fault		Test	Output	
		x_1, x_2	Normal $\hat{x}_1, \hat{x}_2$	Faulty $\hat{x}_1, \hat{x}_2$
SWITCHING ELEMENT FAULT	$s_3 - s_{10}$	0 1	1 1	0 1
		1 0	0 0	1 0
	$s_3 - s_{11}$	0 1	1 1	ϕ 1
		1 0	0 0	ϕ 0
		0 0	0 0	0 0
		1 1	1 1	1 1
	$s_3 - s_{12}$	0 1	1 1	0 0
		1 0	0 0	1 1
	$s_3 - s_{14}$	0 1	1 1	ϕ -.0
		1 0	0 0	ϕ 1
		0 0	0 0	0 0
		1 1	1 1	1 1
	$s_3 - s_{14}$	0 1	1 1	0 ϕ
		1 0	0 0	1 ϕ
		0 0	0 0	0 0
		1 1	1 1	1 1
	$s_3 - s_{15}$	0 1	1 1	ϕ ϕ
		1 0	0 0	ϕ ϕ
		0 0	0 0	0 0
		1 1	1 1	1 1

III. Single Fault-diagnosis

1. Diagnosis procedure for link stuck fault.

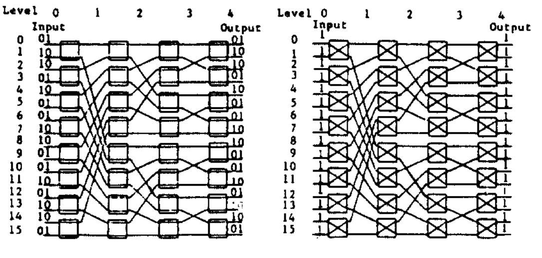
Single fault diagnosis procedure for a multistage baseline network with 4 valid states are considered below.

In a NxN ($N=2^n$) networks, there are $N(\log_2 N+1)$ links and $N(\log_2 N)/2$ switching elements[17]. For each element, there are 16 possible state combinations [4 valid state], but only one of them is normal, the other (16^4-1) state combinations is faulty, In a complicated situation such as this, it is very important to choose fault-diagnosis procedure properly. This method can be divided into two main diagnosis procedures : one for link stuck fault with s_{10} and s_5, the other for switching element fault with s_{12} and s_3[17]. When setting the multistage network into phase 1 test and phase 2 test and generating the input test sets, if the network is fault-free, the fault-free output responses are shown in Fig. 3, and an alternate test scheme is shown in Fig. 4.

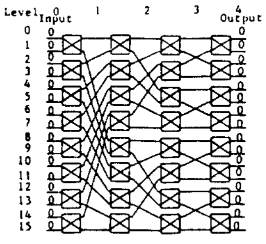
If a single stuck-at-zero fault is detected during phase 1 test the phase 2 test for s-a-0 fault is selected, if a single stuck-at-one fault is detected during phase 1 test the phase 2 for s-a-1 fault is selected and an alternate phase scheme is the same.

Fig. 5 gives an example of the detection and location of link faults. Since phase 1 test identifies the link fault to be a stuck-at-0 type, every output terminals then receives a 1 during the phase 2 test. From the two test the possible faulty link are identified to be (6,6,3,5,6) for phase 1 and (7,6,2,0,1) for phase 2.

Intersecting these two set we find that the link stuck-at-0 fault is located at link 6 of level 1.

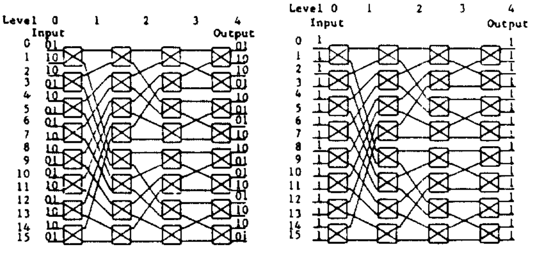


(a) Phase 1 test. (b) Phase 2 test for s-a-0 fault.

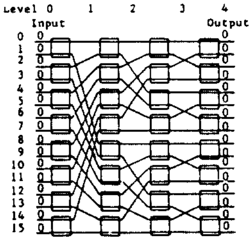


(c) Phase 2 test for s-a-1 fault.

Fig. 3. Fault-free response.

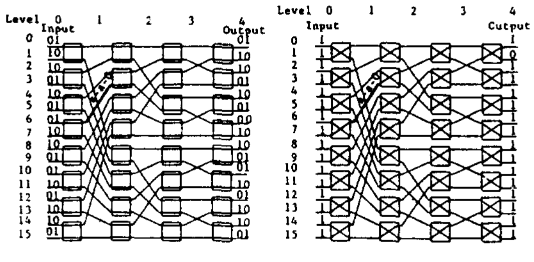


(a) Phase 1 test (b) Phase 2 test for s-a-0 fault



(c) Phase 2 test for s-a-1 fault

Fig. 4. Fault-free response of an alternate test scheme.



(a) Phase 1 test. (b) Phase 2 test.

Fig. 5. Locating the link stuck fault.

Therefore, in a NxN networks, much similar method is used to locate the link stuck fault. Hence, it is obvious that only three tests are required to detect and to locate the single link stuck fault.

The existance of a fault can be determined by looking at the information in the output responses. The type and location of the fault may then be pinpointed.

2. *Diagnosis procedure for switching element fault with s_{12} and s_3.*

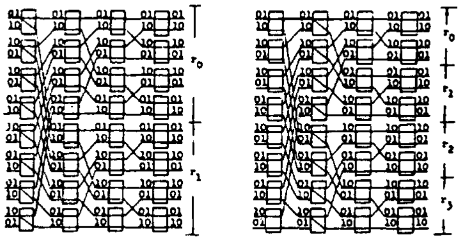
In a multistage network, switching elements at valid state s_{12} or s_3 make some input disconnect from its any outputs whatsoever, therefore some fault information is thereby isolated from the output responses of the network. This make fault diagnosis for s_{12} and s_3 more complicated than for s_{12} and s_5.

A stage-sequential diagnosis method is considered below for valid states s_{12} and s_3. A network at phase s_{10} test (or phase s_5 test), which has already been tested in the previous procedure, is chosen as a reference network. A multistage network is fault-free at valid states s_{10} and s_5. A 16x16 multistage baseline network is used as an example to describe the diagnosis procedure as follows: To set the reference network to phase 12-0 test as shown in Fig. 6(a), the elements at stage 0 are set to test state s_{12}. The others remain at s_{10} and are fault-free. If fault-free output response appear in the output of the network, all elements at stage 0 are fault free at s_{12}. If faulty output responses appear, there is a faulty element at stage 0. According to the faulty output responses, the fault location and type of a fault element can be pinpointed by two tests. Of course, if there are "ϕ" or "–" types of fault output responses, two additional tests are needed to distinguish them.

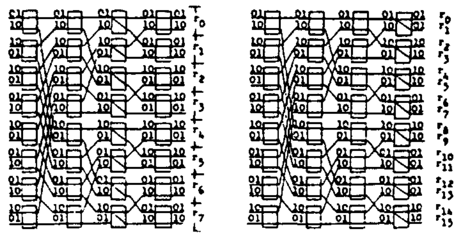
When changing states of the elements at stage 12-i ($1 \leqq i \leqq \log_2 N-1$) as shown stage by stage in Fig. 6(b), (c), (d) and repeating in a similar way, all switching elements can be tested for state s_{12}.

The diagnosis procedure for stage s_3 is called phase 3-i tests and similar to the procedure for s_{12}.

The location and type of a fault element at s_{12} and / or s_3 can be determined by at the most $4\log_2 N+3$ tests. Because each element is tested independently in the diagnosis procedure, multiple faulty elements can also be detected and pinpointed in the same way.



(a) Phase 12-0 Test (b) Phase 12-1 Test



(c) Phase 12-2 Test (d) Phase 12-3 Test

Fig. 6. Output responses of fault-free network at Phase 12-i test.

IV. An Example for Diagnosis

In the fault-diagnosis procedure of phase 1 test and phase 2 test, the fault location has already been pinpointed. But a questionable regions, shown in Fig. 7, consisting of a questionable stuck link and two questionable faulty elements has been considered. As shown in Table 6, there are 4 kinds of faulty element at s_{10} and s_5 mixed up with 4 kinds of stuck

Table 6. Four paisr of indistinguished fault sources

No.	Faulty Output Responses		Equivalent Fault Sources and Fault State Combinations
	Phase 10 Test	Phase 5 Test	
1			Stuck upper input link
			Element at ($S_{10}-S_2$ S_5-S_1)
2			Stuck lower input link
			Element at ($S_{10}-S_8$ S_5-S_4)
3			Stuck upper output link
			Element at ($S_{10}-S_2$ S_5-S_4)
4			Stuck lower output link
			Element at ($S_{10}-S_8$ S_5-S_1)

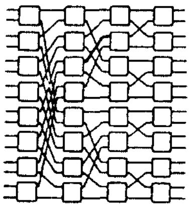
links, so there are one model of questionable region as shown in Fig. 7.

Two questionable switching elements are at stages (i-1) and i and the questionable stuck link connects the upper output of the questionable element i-1 to the upper input of the questionable element i.

Step 1. First, set the reference network of phase 12-(i-1) test as shown in Fig. 8(b).

There are only two possible faulty paths which are called the upper (fault) path and the lower (fault) path, and are represented by darkened lines. The possible situations of output responses of the network are as follows:

1. If the output responses are fault free at phase 12-(i-1), it is determined that both the questionable stuck link and the questionable element i are fault-free.
   The fault is determined at the questionable element i-1 with such a faulty state combination as (s_{10}-s_2, s_5-s_4, s_{12}), i.e., s_{10} is mistaken for s_2, s_5 for s_4 and s_{12} is fault free. The location and type of a single fault element are pinpointed.



Model 1

Fig. 7. The models of the questionable regions.

2. If there is a "ϕ" type or binary type of fault on the upper path, or a fault on the lower path, or one fault each on both the upper path and the lower path, it is determined that the questionable stuck link and the questionable element i are fault-free. The location and type of a single fault are pinpointed at the questionable element i-1 with such a faulty state combination as (s_{10}-s_2, s_{12}-s_r), here s_r is a fault state relevant to the faulty output responses and can be determined according to Table 4.
3. If a "–" type of fault is found on the upper path only, it is still a questionable situation. In the questionable region, the possible faulty state combination for the questionable element i-1 is (s_{12}-s_2, s_5-s_4, s_{12}-s_4) and another one for the questionable elements is (s_{10}-s_2, s_5-s_1).

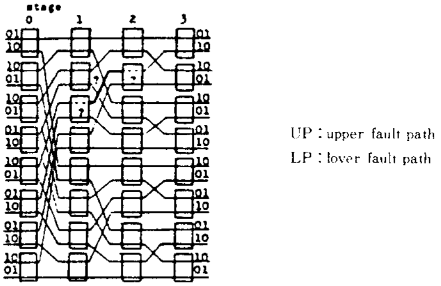
Now it is obvious that the fault of a network has been pinpointed at the questionable element i-1 in situation 1 and 2, thus only one more phase 3-(i-1) test for element i-1 at s_3 is further needed. After this, all the diagnosis procedure for four valid state are completed. For situation 3, because a questionable stuck link and two questionable elements are still mixed up, further diagnosis step is then needed as shown in step 2 below.

Step 2. Set the reference network to phase 3-(i-1) test as shown in Fig. 8(c). The diagnosis procedure is similar to that of step 1 above. It is obvious that a fault of the network is pinpointed at element i-1 in situation 1 and 2, and all the diagnosis procedure of the network with four valid states is now completed.

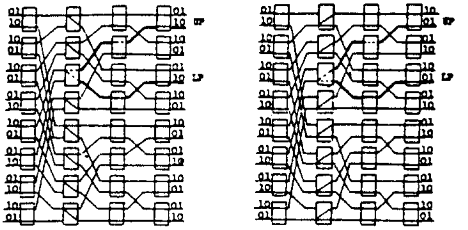
However, the situation 3 is still a questionable one. A further diagnosis step is needed as shown in step 3 below.

Step 3. Set the reference network to phase 12-i test as shown is Fig. 8(d), using the way similar to that of step 1 above. In situation 1 and 2, the fault location and fault type of the network are pinpointed at element. One more phase 3-i test for faulty elements s_3 is needed. However, there is a questionable region remaining in situation, and a further diagnosis step 4 is needed as shown below.

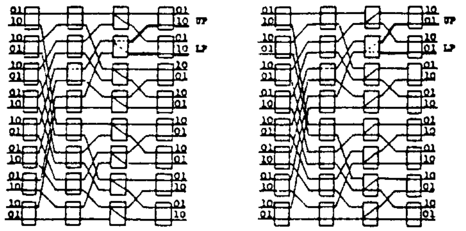
Step 4. Set the reference network to phase 3-i test as shown in Fig. 8(e), using the way similar to that of step 1 above. In situation



(a) Questionable region model 1 and reference network.



(b) Phase 12-1 test (c) Phase 3-1 test



(d) Phase 12-2 test (e) Phase 3-2 test

Fig. 8. Diagnosis procedure for questionable region model 1 at s_{12} and s_3

1, a single fault of the network is pinpointed at elements. However, in situation 2 the output responses of the network are fault-free, it is estimated that the questionable elements is fault free only at s_3. Because of some diagnosis information to be isolated, we cannot determine whether the element i is fault-free at the other 3 valid state, and what happens to the questionable stuck link and the questionable element i-1.

Therefore, there is a questionable region finally remaining in the network in situation 2.

As mentioned in Section II, if a "–" type of fault is found an upper path only (up) as shown Fig. 8(b).

It is still a questionable situation.

In the questionable region, we know that the possible faulty state combination for questionable element i-1 is (s_{12}-s_2, s_5-s_4, s_{12}-s_4) and another one for the questionable element i is (s_{12}-s_2, s_5-s_1).

Now lets assume that faulty state combination for the questionable element i-1 . (s_{12}-s_2) is detected on the upper path.

We can find that the questionable element i-1 is disconnected with the questionable element i because of no logical connection. We cannot locate the stuck link fault and the fault type of the questionable element i-1 and the questionable element i is the one of the 16 state combinations.

It is evident that in a certain questionable region the unlocatable probabilities of these questionable sequences are as follows:

a) The questionable stuck link 1
b) The questionable element i-1 ..... $1/16^4$
c) The questionable element i .... $1/16^4$

The diagnosis procedures for network with four valid states have been completed.

V. Conclusion

We have shown that only three tests are necessary and sufficient to detect and locate a single link stuck fault.

In the single fault-diagnosis method for a multistage baseline network, both the single link stuck fault and the single switching element fault with four valid state can be detected, but all link stuck faults and four kinds of element faults relevant to four kinds of faults combinations cannot be pinpointed.

However, the location and types of all other element fault can be pinpointed. The unlocatable probabilities are equal to 1 for a stuck link, to $1/16^4$ for a element with four valid states as compared to $1/16^2$ for a element with two valid states.

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