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The Study of Factors that Influence the Surface Electric Field of High Voltage Planar PN Junctions

(고전압 평면형 pn접합의 표면전계에 영향을 미치는 요인에 관한 고찰)

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要 約

평면형 pn접합의 최대 표면전계를 감소시키는데 있어서, field plate와 window tapering의 효과를 2차원 컴퓨터 시뮬레이션에 의해 고찰하였다. 또한 SiO_2절연체 두께의 영향도 제시되었다.

Abstract

The effectiveness of field plate and window tapering in reducing the maximum surface electric field of planar pn junctions has been studied by two dimensional computer simulation. The influence of silicon dioxide insulator thickness is also presented.

I. Introduction

One of the main problems of high voltage planar devices that contain pn junctions is that the surface breakdown fields of these devices are generally smaller than their bulk breakdown fields. This fact is basically due to the greater imperfections and instabilities that are located at the surface of the planar device. Therefore, one of the goals of high voltage planar device design is to reduce the electric field at the bulk region rather than on the surface. The objective of this paper is to study the effects of field plate, window tapering, and silicon dioxide thickness on the surface electric field of a planar device.

A pn junction operated in the reverse bias mode is used as the base structure. The potential distribution and electric field of a device can be obtained by solving Poisson's equation. In the general approach of semiconductor device physics analysis, the total charge density is determined by solving Poisson's equation, the transport equations for electrons and holes, and the continuity equation simultaneously[1]. But for the case of a reverse biased pn junction where applied voltage is much larger than the built in potential, the device can be broken into a neutral region where the charge is zero and regions that have a space charge density approximately equal to the net impurity concentration given by a doping profile such as the Gaussian function. The problem is basically, then, simplified to simultaneously finding a solution to Poisson's equation and locating the space charge boundary.

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The potential distribution and electric field for various conditions of the pn junction device will be obtained through the two dimensional computer simulations. Finite difference method is used to linearize Poisson's equation while the iterative numerical technique of successive overrelaxation[2] is used to obtain the solution.

II. Device Structure and Basic Equations

A diagram of the basic pn junction structure is shown in Fig. 1. Using the approximation of zero variation in the z-direction, the device can be treated as a two dimensional problem in rectangular coordinate. Since the pn junction is also symmetric with respect to the y-axis, the device can be divided down the middle without introducing any significant errors. This reduction in the device model size will reduce the amount of computer storage space and computational time that are required during the simulation. Note that the lateral out diffusion of the p+ region is assumed to equal to the junction depth. This is not a really bad approximation since for heavily doped junction, the lateral diffusion length is usually about eighty to ninety percent of the junction depth[3]. The final model along with its coordinate system is shown in Fig. 2.

The model used in the simulation divides the device into various basic regions. Included in these regions are the lightly doped n-type bulk silicon, the more heavily doped p-type silicon, silicon dioxide insulator, metallization lines, air, and various interfaces between the different regions. Poisson's equation for individual region will be unique. Metal lines are considered equipotential regions and their potentials are defined by the bias voltage applied to them. An interface can mathematically be approximated by a single line even though that is physically untrue. And finally, to simplify Poisson's equation in the silicon regions, a constant doping profile is used to approximate the p+ diffusion region rather than the more accurate Gaussian profile.

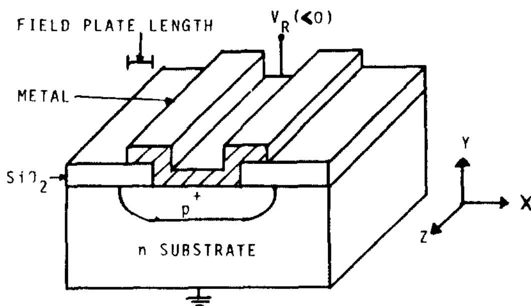

Fig. 1. Basic pn junction device.

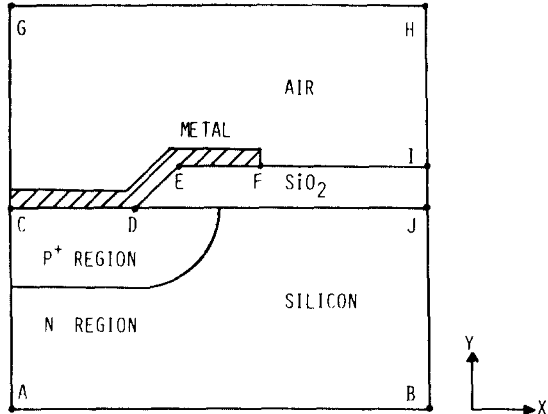

Fig. 2. Two-dimensional model of the pn junction device.

The primary equation used in the simulation of the reverse biased pn junction is Poisson's equation. Using the assumption that the dopant atoms are fully ionized, the two dimensional equations in the silicon regions are given as:

$$\frac{\partial^2\Phi}{\partial X^2}+\frac{\partial^2\Phi}{\partial X^2}=-\frac{q(N_D-n(\phi_n,\ \Phi))}{\varepsilon_s},\quad \text{for n region}$$

$$\frac{\partial^2\Phi}{\partial X}+\frac{\partial^2\Phi}{\partial Y^2}=-\frac{q(p(\phi_p,\ \Phi)+N_D-N_A)}{\varepsilon_s},\quad \text{for p region}$$

where Φ is the potential of the system, ξ_S the dielectric constant of silicon, n the electron concentration, p the hole concentration, N_D the n-type doping concentration, N_A the p-type doping concentration, ϕ_n and ϕ_p the quasi-Fermi levels in the n and p regions, respectively. But in the dielectric regions of SiO_2 and air, Poisson's equation becomes Laplace's equation. That is,

$$\frac{\partial^2\Phi}{\partial X^2}+\frac{\partial^2\Phi}{\partial Y^2}=0,\quad \text{for dielectric regions}$$

III. Numerical Method

1. Finite Difference Equations

The finite difference numerical technique has been used in the calculation of the potential distribution within the pn junction. The goal is to solve the two dimensional Poisson's equation of the form:

$$\frac{\partial^2 \Phi}{\partial X^2} + \frac{\partial^2 \Phi}{\partial Y^2} = F(X, Y, \Phi)$$

where $F(X, Y, \Phi)$ is a function of position and electric potential. The basic approach of the finite difference method is to transform differential equations into difference equations which then can be applied to a mesh of grid lines.

First, the regions of the device under consideration are divided into two dimensional array of grid points as shown in Fig. 3. The grid spacings h_1, h_2, h_3, and h_4 can be all different, but they are chosen to be equal in this case for simplicity. The size of the spacings will determine the truncation errors of the simulation. Therefore, finer grid spacings are usually used in areas like the depletion region where the potentials can change quickly.

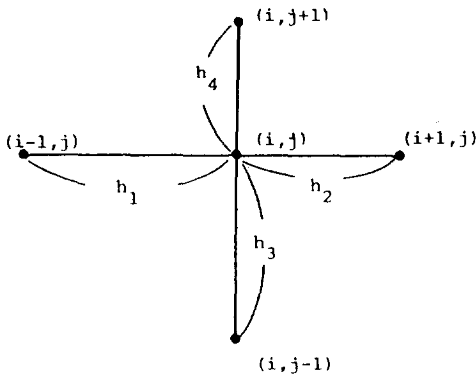

Fig. 3. Arrangement of grid points for the five-point approximation.

For every point in the network, a particular electric potential $\Phi_{i,j}$ has been assigned to it. The five-point finite difference formation is applied by expanding $\Phi_{i-1,j}$, $\Phi_{i+1,j}$, $\Phi_{i,j-1}$, and $\Phi_{i,j+1}$ in Taylor's series to the second order about the central point (i, j). The explicit finite difference approximation to the Poisson's equation then becomes

$$\frac{\Phi_{i-1,j} + \Phi_{i+1,j} + \Phi_{i,j+1} + \Phi_{i,j-1} - 4\Phi_{i,j}}{h^2} = F_{i,j},$$

where $F_{i,j}$ is the approximated value of $F(X,Y,\Phi)$ at the point (i, j).

2. Boundary Conditions

Since Poisson's equation is a nonlinear elliptic differential equation, a set of boundary conditions is needed to solve for the unique potential distribution of the device. Therefore, the potentials around the perimeter of the pn junction structure must be specified in order to obtain the potential distribution inside the boundary.

For the boundary conditions surrounding the silicon region, the bottom metal electrode is considered to be grounded (AB in Fig. 2:V=0) while the metal input electrode (CDEF) has the potential of the input V_R. For the boundary far away from the junction (JB), the potential along that edge is zero. Finally, the potential distribution for a one-dimensional two-sided abrupt pn junction is used as the boundary condition at the edge of the junction. The above approximation for the junction boundary condition was based on the assumption that there are no free carriers inside the space charge region and that charge neutrality exists in the neutral regions. It also assumes that for the normal range of reverse currents passing through the structure, the electric field in the neutral regions is practically zero and that the entire applied voltage exists over the space charge region.

For the air region, earlier works by Adler et al[4] have shown that the potential distribution along the perimeter of this region does not have a strong influence on the potential distribution solution within the silicon if the thickness of the air region (CG) is larger than that of the semiconductor region (AC). Therefore, the potential along the edge (CG) was chosen to vary linearly from $V=V_R$ at the input electrode to V=0 at the top boundary. The potentials along the boundary (GH) and far edge (HIJ) are also at zero.

For the silicon-SiO_2 interface and the SiO_2-air interface,, continuity of tangential electric

field and normal displacement vector through the interfaces are required when there is no surface charge. Thus along the interface edges:

$$\text{(DJ)}: \quad E_t^S = E_t^d \text{ and } \epsilon^s E_n^s = \epsilon^d E_n^d$$

$$\text{(FI)}: \quad E_t^d = E_t^a \text{ and } \epsilon^d E_n^d = \epsilon^a E_n^a$$

where ϵ is the permittivity and E the electric field. Superscripts s, d, and a in order denote the silicon, dielectric (SiO_2), and air regions while subscripts t and n represent the tangential and normal components of the electric field at the interface, respectively.

When the boundary conditions are established, an initial guess potential is assigned to each grid point in the matrix. Then the difference equations in the various regions are solved using the successive overrelaxation method.

3. Successive Overrelaxation Technique

To obtain the potential distribution of the pn junction, the finite difference equations in the various regions are solved iteratively using the successive overrelaxation method. For a fixed ω, $1 < \omega < 2$, the successive overrelaxation method is defined by the following iteration scheme:

$$\Phi_{i,j}^{t+1} = \Phi_{i,j}^{t} - \left(\frac{f_{i,j}(\Phi_{i-1,j}^{t+1},\ \Phi_{i+1,j}^{t},\ \Phi_{i,j-1}^{t+1},\ \Phi_{i,j+1}^{t},\ \Phi_{i,j}^{t})}{\dfrac{\partial f_{i,j}}{\partial \Phi_{i,j}}} \right)$$

where the superscripts are iteration indices.

Since the potentials with superscript (t+1) represent the values obtained during the current iteration while those with superscript (t) represent the values obtained during the last iteration, the application of the various equations to the points in the matrix must go from left to right while scanning from bottom to top. Therefore, the first point of the matrix, (1,1), is located at the bottom left hand corner of the pn junction structure. The appearance of the superscript (t+1) on the right hand side of the equation, when combined with the order of computation, implies that the improved or most recent potential values are used as soon as they are computed. From trying various values between 1 and 2, an overrelaxation factor (ω) of 1.97 was used because it gives a faster convergence in the simulations.

The final potential distribution is obtained when the change in potential at all grid points between two successive iterations is smaller than a prescribed value δ:

$$|\Phi_{i,j}^{k+1} - \Phi_{i,j}^{k}| < \delta$$

where k is the superscript denoting the order of iteration. A maximum error value of 0.256V was used for δ. Once the potential distribution is calculated, the electric field at each point can be obtained easily. The finite difference expression for the electric field at a grid point (i, j) can be written as the change in potential per unit length:

$$E_X = \frac{\Phi_{i+1,j} - \Phi_{i-1,j}}{2h}$$

$$E_Y = \frac{\Phi_{i,j+1} - \Phi_{i,j-1}}{2h}$$

where E_X and E_Y are the electric fields in the X and Y directions, respectively. Then the total field magnitude, E_T is:

$$E_T = \sqrt{E_X^2 + E_Y^2}$$

IV. Results and Discussions

1. Influence of Field Plate

The results of the computer simulation for various length of field plate are shown in Fig. 4a-c. Each figure plots the intensity of the electric field along the surface of the device as well as the potential distribution around the pn junction region. In all these cases, the junction depth and curvature were both 2 μm while the substrate doping was 1.0×10^{15} cm^{-3} and the applied voltage V_R was -100 V. Also, the oxide insulator was set at 1 μm thick. Fig. 4a shows the situation when there was no field plate and the device is just a basic pn junction.

Since the p^+ region (N_A=1.0x10^{18} cm^{-3}) is so much more heavily doped than the n substrate, most of the depletion region is located on the substrate side of the junction. As a result, the surface electric field has the shape of a typical p^+n junction with the maximum field occurring at the p^+n junction interface. Since only a very small portion of the depletion region resides on the p^+ side, the electric field rises very sharply from just inside of the p^+ diffusion. Notice that the potential lines are much more crowded together near the junction surface and a little more spread out in the flatter bulk region resulting in a higher field intensity at the surface.

For the case of a 1 μm field plate, simulation result shows that a field plate with length too small to overlap the junction out diffusion region only has a very small effect in reducing the surface electric field. But when the field plate was increased to 5 μm (Fig. 4b) and 8 μm (Fig. 4c), the results show that the peak surface electric field at the interface is reduced significantly while a second surface electric field peak now appears at the edge of the field plate. Notice that the longer field plate had effectively widened the potential lines at the surface which was the main reason for the reduction of the surface electric field strength.

Computer simulations also have shown that the strength of the extra surface electric field at the edge of the field plate is approximately constant if it is beyond the edge of the junction out diffusion. Results have also shown that a 8 μm or 9 μm field plate will cause the peak surface electric fields at the junction interface and plate edge to be roughly equal. Therefore, any further increase of the field plate length will only reduce the peak field at the junction interface while the peak field at the edge of the plate will remain just about constant.

Since field plate causes the potential distribution to be more spread out at the surface region, the maximum electric field of the device is also reduced while its location still remains in the junction curvature bulk region but with a slight shift away from the surface.

Finally, Fig. 5(a) summarizes the results of the field plate by plotting the surface peak electric field versus plate length for the constant junction depth and out diffusion of 2 μm.

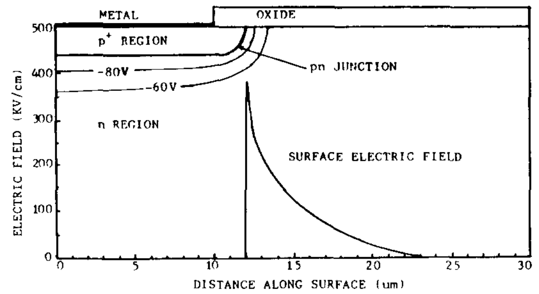

Fig. 4 (a). Plots of surface electric field and electric potential for the case of no field plate.

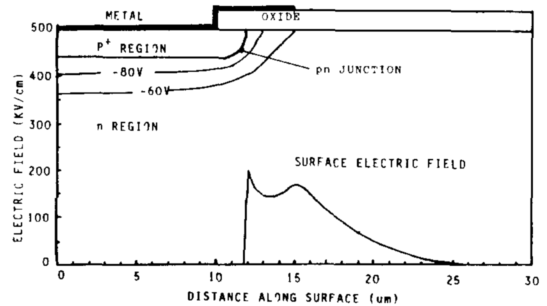

Fig. 4 (b). Plots of surface electric field and electric potential for the case of 5μm field plate.

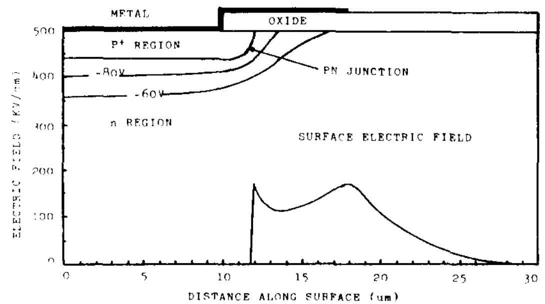

Fig. 4 (c). Plots of surface electric field and electric potential for the case of 8μm field plate.

2. *Influence of Tapered Window*

Another method that can be used to reduce the surface electric field of the pn junction is the tapered window [5] as shown in Fig. 6. additional advantage of this approach is the

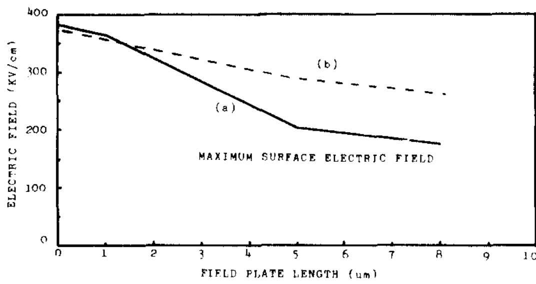

Fig. 5. Plot of field plate length versus maximum surface electric field (a) for the case of 1 μm thick oxide, and (b) for the case of 2.5 μm thick oxide.

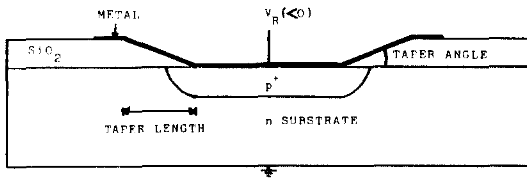

Fig. 6. pn junction device with a tapered window.

fact that it can provide a better step coverage for metallization than the normal vertical step window. This factor may be important in terms of increased reliability of the device.

The results for tapered window length of 5 μm (11.3 degree) are shown in Fig. 7. The surface electric field once again has two peaks, one at the junction interface and the other at the edge of the metallization. In this case, the two peaks are approximately equal and the use of any other lower tapering angles will result in the maximum surface electric field being located at the edge of the metal overlap. But notice that the results for these two cases are just about identical to those of 5 μm and 8 μm field plate overlapping a 2 μm junction. And the tapered window approach only required a 5 μm metal overlap of the junction. Therefore, the results seem to indicate that once the metalization is beyond the edge of the junction out diffusion, the tapered window approach has a stronger effect in reducing the surface electric field than the field plate method. This result is similar to the case of a Schottky diode where simulations done in this study along with results from Choi[6] showed that tapering is more effective than field plate in reducing the surface electric field. Fig. 8 again summarizes the results for the tappered window method.

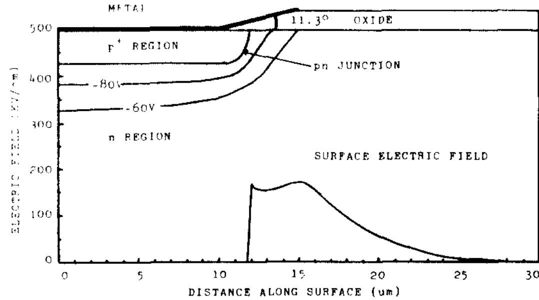

Fig. 7. Plots of surface electric field and electric potential for the case of 11.3 degree tapering.

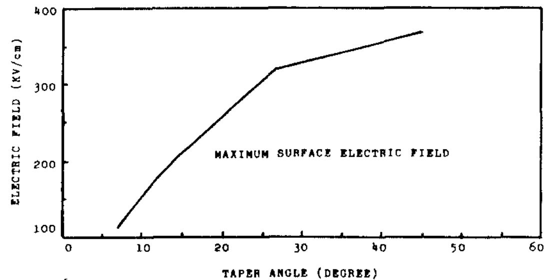

Fig. 8. Plot of taper angle versus maximum surface electric field.

3. Influence of Oxide Thickness

The general tendency for increasing oxide thickness is that the maximum surface electric field is reduced [7]. But reduction is very small and the effect of oxide thickness on the normal junction is not too significant. This is shown in Fig. 9 where the reduction of maximum field is small. However, the increase of oxide thickness does have an important impact on cases where the junction has a field plate.

Results for 2 μm junction with field plates of 5 μm and 8 μm show that when the oxide thickness was increased to 2.5 μm from 1 μm, the maximum surface electric field at the junction interface did not decrease as much compared to the normal 1 μm thick oxide case.

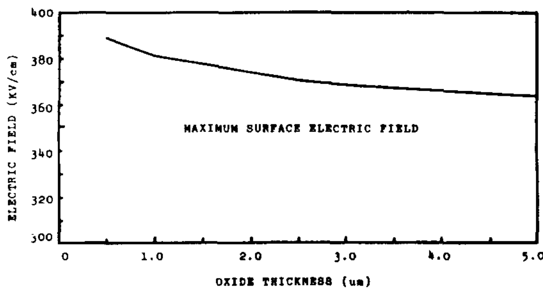

Fig. 9. Plot of oxide insulator thickness versus maximum surface electric fields.

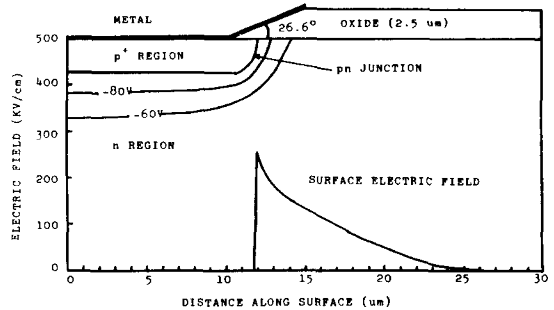

Fig. 10. Plots of surface electric field and electric potential for the case of 26.6 degree tapering with 2.5 μm thick oxide.

This is shown in Fig. 5(b). Also, the second surface electric field peak that usually occur at the edge of the field plate was not observed. Therefore, the plot of the surface electric field for the cases of the 2 μm junction with 2.5 μm thick oxide and 5 μm field plate looked just like the case of a normal junction without any field plate. However, further simulation of the 8 μm field plate case using an oxide thickness of 1.75 μm instead of 2.5 μm show that while the maximum surface electric field was reduced, a small peak electric field once again appear at the edge of the field plate. The results seem to indicate that while the oxide thickness only has a mild influence on the maximum surface electric field of a normal junction, it does have a strong effect on a device that has an overlapping field plate. For the case with the field plate, increasing oxide thickness will decrease the second electric field peak at the edge of the field plate.

However, for the case of the tapered window, results seem to show that increasing the oxide thickness does not really influence its effectiveness in reducing the surface electric field at the junction interface. Fig.10 shows the case of a 5 μm tapered window length (26.6 degree) with a 2.5 μm thick oxide. Notice that with a thicker oxide, the taper angle is increased. At the surface, the resulting maximum electric field is smaller than the case of 2 μm tapered window length (26.6 degree but 1 μm thick oxide) but larger than the 5 μm tapered window length (11.3 degree and 1 μm thick oxide). But notice how the thicker oxide has now significantly reduce the second surface electric field peak at the edge of the metal overlap as well as causing a greater reduction in the maximum surface electric field for the same angle of tapering. Therefore, this combination of tapered window and thicker oxide appears to be quite effective in reducing the maximum surface electric field.

V. Conclusion

Two methods that can substantially reduce the maximum surface electric field are utilization of field plate and tapered window. Simulation results indicate that the tapered window approach has a greater effect on reducing the surface electric field than the field plate method. However, in both cases the reduction of the surface field is limited by the second surface electric field peak located at the edge of the metal overlap. But this problem can possibly be solved by the use of thicker silicon dioxide insulator. Results show that even though thicker oxide does reduce the effectiveness of the field plate, it still has a large influence in reducing the second electric field peak located at the edge of the metal overlap. Therefore, if reducing surface electric field is the only consideration when using a field plate, then the approach that combines all the above factors will have a pn junction with a long overlapping field plate and a thick silicon dioxide insulator. But because of the existence of the two conflicting effects of reduced field plate effectiveness and decreased surface field at the metal plate edge for increasing oxide thickness, the choice of the oxide thickness will have to be

made carefully to maximize the result.

However, if the tapered window method is used, the thicker oxide does not cause any problem because it does not really affect the ability of the tapered window to reduce the peak surface electric field at the junction interface. Therefore in this case, the preferred combination of a small taper angle and a thick oxide insulator would be the best technique of those that were studied in this paper in reducing the maximum surface electric field of a high voltage planar pn junction.

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