Study on the Fabrication of EPROM and Their Characteristics

(EPROM의 제작 및 그 특성에 관한 연구)

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要 約

프로팅 게이트 위에 컨트롤 게이트를 갖는 n-채널 이중 다결정 실리콘게이트 EAROM을 제작하였다. 채널 길이는 4-8μm, 채널 폭은 5-14μm로 하여 5μm design rule에 따라 설계하였으며 서로 다른 4가지 컨트롤게이트 구조를 갖는 채널 주입형 기억소자를 얻었다. 그리고 소자의 punch through 전압과 게이트에 의해 조절되는 채널파괴 전압을 증가시키기 위해 이중 이온주입(double ion implantation)과 active 영역에 보론이온을 주입하였다.

프로그래밍을 위해 드레인 전압 및 게이트 전압이 각각 13-17V 및 20-25V 정도 필요하였다. 그리고 제조된 기억소자의 소거는 광학적 방법뿐 아니라 전기적 방법으로도 가능하였으며 125℃에서 200시간 유지하였을 때 축적된 전자가 약 4%정도 감소함을 알 수 있었다.

Abstract

EAROM device is an n-channel MOS transistor with a control gate stacked on the floating gate. On account of channel injection type, channel lengths are designed 4-8 μm and channel widths 5-14 μm. These devices which have fourstructures of different type control gate are designed by NMOS 5 μm design rule and fabricated by double polysilicon gate NMOS process. Double ion implantation is applied to increase punchthrough voltage and gate-controlled channel break-down voltage.

The drain and gate voltage for programming was 13-17V and 20-25V, respectively. EPROM cell fabricated could be erased not by optical method but by electrical method. The result of charge retention test showed decrease in stored charges by 4% after 200 hours at 125°C.

I. Introduction

In recent years, many works have been carried out competitively for development of nonvolatile memory devices which have drawn keen interest in the application to integrated circuits.[1-14] The first nonvolatile memory device was proposed by Kahng and Sze in 1967.[3] They used floating gate structure (MIMIS) in which semipermanent charge storage was possible. And Frohman-Bentchkowsky[2] made advent of FAMOS (floating gate avalanche injection MOS) of which floating gate material was polysilicon and based on the avalanche injection of electrons

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from the p-n junction. But using these types of devices it was impossible to erase the charges stored in floating gate.

To compensate this shortcoming, Iizuka et, al.[5] made p-channel Electrically Alterable Read Only Memory(EAROM) as an avalanche injection type in which two polysilicon gate layers separated by insulation layers were introduced. The additional second gate which enables the erasing of stored charges is called as control gate. Of late, owing to the successful improvement of NMOS process technology, n-channel EAROMs were developed. And we are now on the step of using Electrically Erasable and Programmable Read Only Memories(EEPROM).[8]

In this paper, described the fabrication of EAROMs which have geometrically different four types of double polysilicon gate structures by the use of NMOS technology. And to increase the punchthrough and breakdown voltage, double and deep ion implantation technique was applied. And the electrical characteristics of EPROM devices concerning programming, erasing, and charge retention are reported. The drain and control gate voltage for programming was 13-17V and 20-25V, respectively. The control gate voltage of 35-45 was needed for electrical erasing. And the result of charge retention test showed decrease in stored charges by 4% after 200 hours at 125°C.

II. Theory

Fig. 1 shows the cross section of EAROM device. As illustrated in this figure this device has two gates. The floating gate is quite isolated by insulating oxide and the electrons injected could be stored, and the control gate on the upper side plays the role of enhancing the efficiency of electron injection and erasing electrically the charges stored on the floating gate. These two gates are made of polysilicon.

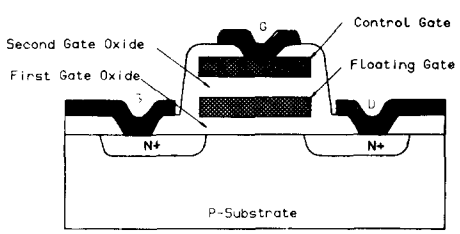


Fig. 1. Cross sectional view of two level polysilicon EAROM cell.

Fig. 2 illustrates schematic diagram and equivalent circuit for explaining the programming.[9-14] The symbols used in this figure explained as follows.

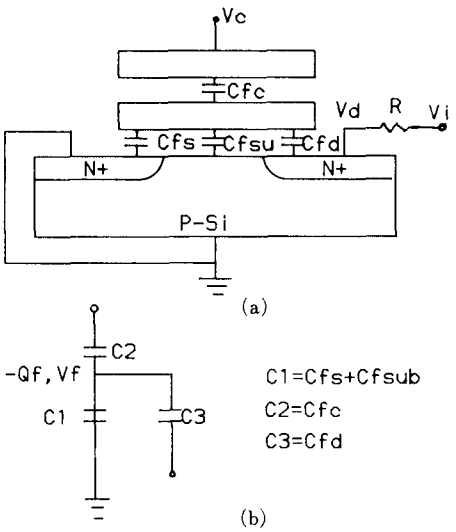


Fig. 2. Schematic diagram (a) and equivalent circuit (b) for programming.

Vf : potential of floating gate
−Qf: charge stored on floating gate
Vc : potential of control gate
Vd : potential of drain
C_{fc} : electric capacitance between floating gate and control gate
C_{fs} : electric capacitance between floating gate and source
$C_{f_{sub}}$: electric capacitance between floating gate and substrate
C_{fd} : electric capacitance between floating gate and drain

The floating gate potential Vf, electric field in the first gate oxide, E_1 and the electric field in the second gate oxide, F_2 could be expressed as follows.[9]

$$V_f = \frac{C_2V_c+C_3V_d-Q_f}{C_1+C_2+C_3} \quad (1)$$

$$E_1 = \frac{C_1+C_3}{S_1\epsilon_{ox}} \cdot \frac{C_2V_c+C_3V_d-Q_f}{C_1+C_2+C_3} \quad (2\text{-a})$$

$$E_2 = \frac{C_2}{S_2\epsilon_{ox}} \frac{(C_1+C_3)V_c-C_3V_d+Q_f}{C_1+C_2+C_3} \quad (2\text{-b})$$

where,

ϵ_{ox} ; electric permittivity of oxide
S_1 ; floating gate area
S_2 ; control gate area

From equation (1), the control gate potential Vc could be expressed as following.

$$V_c = \frac{C_1+C_2+C_3}{C_2} V_t + \frac{Q_f}{C_2} = V_{to} + \frac{Q_f}{C_2}$$

$$= V_{tm} \quad (3)$$

where,

Vt ; threshold voltage when floating gate used as conventional gate
V_{to} ; threshold voltage in case no stored charges on floatnss gate
V_{tm} ; threshold voltage when charges stored on floating gate.

As the process of charge store progresses, the potential difference between channel and floating gate comes to decrease gradually and finally no potential difference occurs. The control gate potential when no potential difference between channel and floating gate is expressed as V_{cp}. In this stage as the control gate potential, V_c increased, E_2 would be much increased and electric field emission of electrons occurs.

Accordingly, the threshold voltage, V_{tm} becomes decreased.[5] In injection limitting region ($V_c<V_{cp}$),

$$Q_f = \frac{C_1+C_2+C_3}{C_1C_3} S_1$$

$$\epsilon_{ox}E_{1i}+C_2V_c-C_3V_d(E_1-E_{1i}) \quad (4\text{-a})$$

$$V_{tm} = V_{to} + \frac{Q_f}{C_2} \quad (4\text{-b})$$

here, E_{1i} is electric field when no channel injection occurs due to no potential difference between channel and floating gate. And in the emission limitting region ($V_c \geq V_{cp}$)

$$Q_f = \cdot - \frac{C_1+C_2+C_3}{C_2} S_2\epsilon_{ox}E_{2c}-(C_1+C_3)V_c-C_3V_d$$

$$(E_2 \leq E_{2c}) \quad (5\text{-1})$$

$$V_{tm} = V_{to} + \frac{Q_f}{C_2} \quad (5\text{-b})$$

here, E_{2c} is electric field in second gate oxide when electrons move from floating gate to control gate.

III. Design and Fabrication of Memory Devices

1. Memory Cell Design

Design of n-channel double polysilicon memory cells was carried out on the basis of 5μm design rule. A cross section and top view of EAROM cell are shown in Fig. 3. The cross

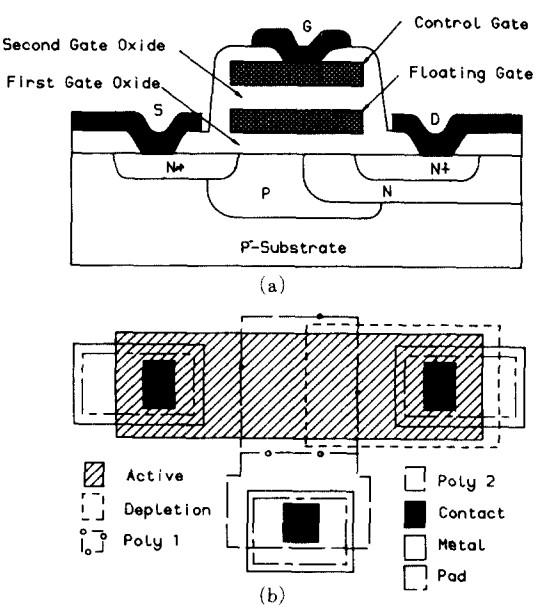


Fig. 3. Cross section (a) and top view (b) of EAROM cell.

Table 1. Gate sizes of the EAROM devices.

Model	No.	Channel Length (μm)		Channel Width	Depletion
		Poly 1	Poly 2	(μm)	Mask
C_1	1	5	5	6	Yes
	2	4	4	6	Yes
	3	4	4	6	No
	4	5	5	6	No
	11	4	4	24	No
	12	4	4	14	No
	16	6	6	6	Yes
	17	7	6	6	Yes
	18	8	6	6	Yes
C_2	6	4	7	6	Yes
	7	4	7	5	Yes
	8	4	5	6	Yes
	9	5	5	6	No
	15	5	7	6	Yes
	21	4	4	6	No
C_3	5	5	7	6	Yes
	10	4	8	6	Yes
	13	5	7	6	No
C_4	14	6	4	6	No
	19	7	5	6	Yes
	20	7	5	5	Yes
	22	6	4	14	Yes

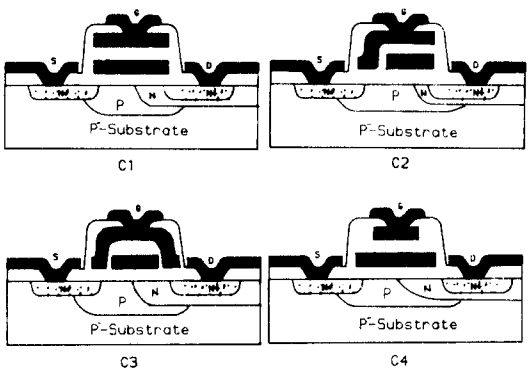


Fig. 4. EAROM cell with
(C_1) ; same poly gate 2 on 1
(C_2) ; partially covered poly one
(C_3) ;completely covered poly 1
(C_4) ;small poly 2 gate on poly a gate.

sections of four different gate configurations; C_1, C_2, C_3 and C_4, which designed for comparing their electrical properties, are shown in Fig. 4. Table 1 illustrates cell models with various channel length and width designed and they were classified into two groups; i.e., cell with depletion mask and one without it.

2. Device Fabrication

1) Mask preparation

Firstly, patterns magnified by 500 times as large as chip size were drawn and digitized using CAD stystem. Generating patterns through this system, reticles 10 times larger than chip size were prepared and hard masks obtained using step and repeat equipment. The number of masks obtained was seven sheets; active, depletion, poly 1, poly 2, contact, metal and pad mask.

2) Oxide layer growth rate on polysilicon

To form the double polysilicon gates, oxide layers must be grown on polysilicon layers. In this section the growth rate of oxide layer on polysilicon would be described. Fig. 5 shows process sequence for checking the growth rate. The temperature maintained during this process was 925°C. Fig. 5(A) indicates the checking sequence of oxide growth rate by the use of α-step method, and 5(B), and 5(c) indicate the sequence of checking the errors occured durng the measurements of oxide growth rate on doped wafer using the α-step and Nanospec.

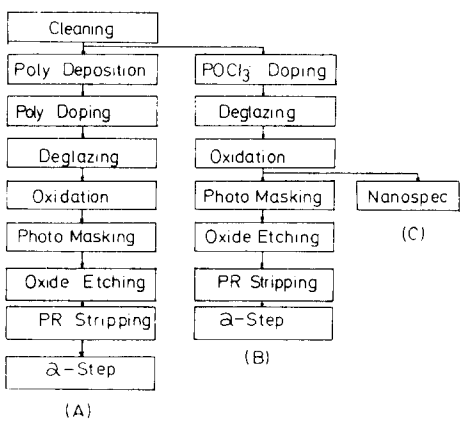


Fig. 5. Process sequence for measuring oxide growth rate.

Fig. 6. illustrates the grow rates with three different substrates on which the oxide layers grown. As shown in Fig. 6. the ratio of growth rate on undoped wafer (A), on doped polysilicon (B) and on doped single crystal wafer (C) 1:2:3 approximately.

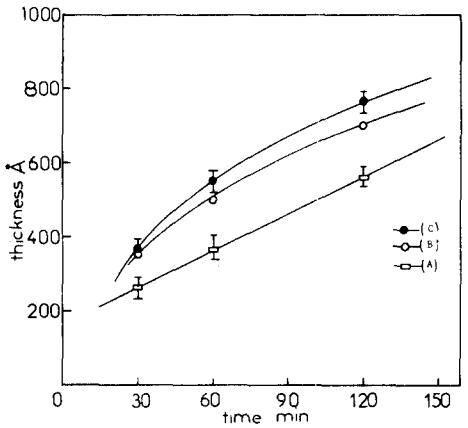


Fig. 6. Oxide growth rate on undoped wafer (A) doped polysilicon (B) and doped single crystal (C).

3) EAROM fabrication

Fig. 7 illustrates the process sequence of EAROM device. The devices are made on 6-9 Ωcm p-type silicon of (100) orientation. Each step of fabrication process will be described.

(i) Initial cleaning and initial oxide layer growth

Dust-free wafers were dipped in the solution of $4H_2SO_4:1H_2O_4$ at 100°C for 10 min and in DI water for ten min. And the thin oxide layers on them were removed by dipping in the solution of $10H_2O:1HF$ for ten sec and in DI water for 10 min. After spin-drying the wafers were osidized initially in O_2 gas at 1,000°C for 3 hrs. and TCE oxidation, with N_2 bubbé TCE in O_2 gas for 90 min., was done. Thus oxide layers of 850Å were obtained. The purpose of initial oxidation is to decrease the leakage current due to stress caused by field oxidation.

(ii) Growth of silicon nitride

Silicon nitride of about 1,000Å was grown by flowing NH_3 for 2 min. at 800°C anc SiH_2Cl_2 for 27 min and also NH_4 for 2 min.

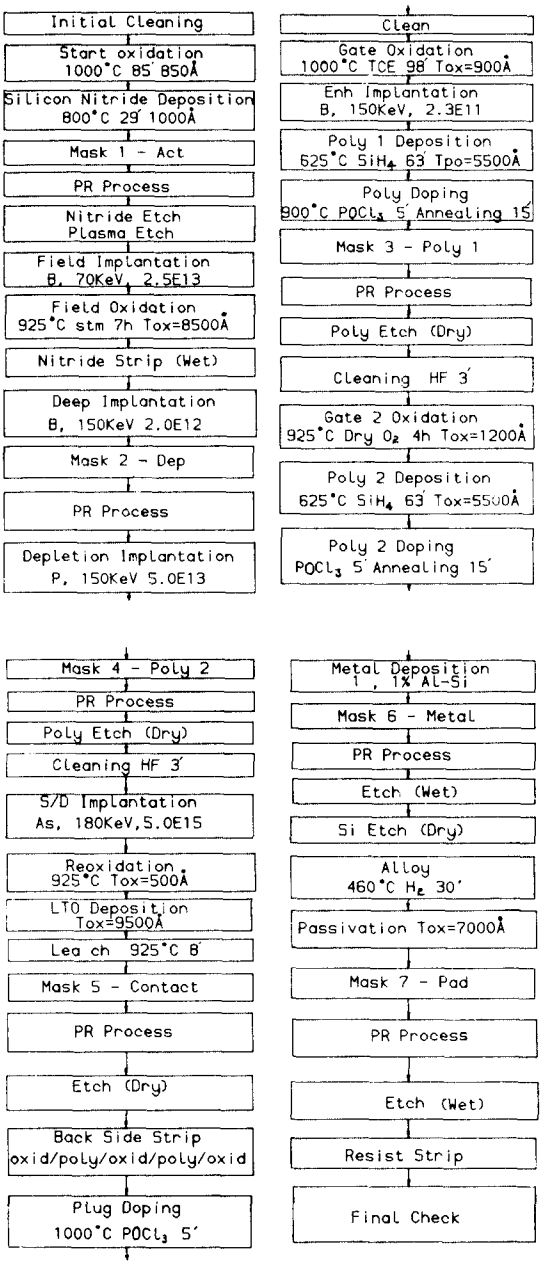


Fig. 7. EAROM cell fabrication sequence.

(iii) Mask 1 and nitride etching

To define the active area Mask 1 was used and photolithography working was done. The photoresist used was positive shipley 1400-26. PR coated was dried for 5 min. at 90°C. And the step of aligning, exposure and developing

(MF 312, 100 min.) were followed. After finishing photholithography unnecessary nitride layer etched away with plasma of CF_4 (3 min.).

(iv) Field implanation and field oxide growth

To increase the parasitic threshold voltage for field area, boron ion was implanted into field area at 70 KeV with $2.5x10^{13}$ ions/cm^2 dose resulting the threshold voltage 33V. After removing PR (dipping in the solution of $4H_2SO_4:1H_2O_2$ at 120°C for 20 min.), field oxide of 8,500Å was grown by maintaining the wafer at 925°C for 3 hrs. in O_2 gas and for 7 hrs. in H_2O steam.

(v) Nitride strip and deep implantation

Nitride was stripped by dipping in H_3PO_4 solution at 165°C for 1 hr. And to increase the punchthrough voltage of short channel device boron ions of 150 keV and $2x10^{13}$ ions/cm^2 were implanted. The junction depth thus obtained was 1.2 μm.

(vi) Depletion mask (mask 2) and depletion implantation

Depletion implantation was carried out using mask 2. The purpose of this process is to increase the channel breakdown voltage and enhance the efficiency of programming. Phosphorous ions of 150 KeV and $5x10^{13}$ ions/cm^2 were implanted, and the junction depth formed was 1 μm.

(vii) First gate oxidation and enhancement implantation

Before the gate oxidation process, the initial oxide layer should be removed completely by dipping the water in the solution of $10H_2O$: 1HF for 4 min. Firstly, initial oxidation was carried out at 1,000°C in O_2 and TCE oxidation at 1,000°C for 30 min. Thus the gate oxide layer of 900Å was obtained.

To control the threshold voltage, borons of 50 KeV and $2.3x10^{11}$ ions/cm^2 were implanted. The thershold voltage after this process was about 1.5V.

(viii) Floating gate and doping

Polysilicon layer of 5,500Å was grown by thermal decomposition of SiH_4 at 625°C for 65 min. And $POCl_3$ doped at 900°C for 5 minutes on the polysilicon layer in N_2 and annealed for 15 min. The sheet resistance was 28-30 Ω/□.

(ix) Poly 1 mask and second gate oxidation

Defined the floating gate using poly 1 mask and the unnecessary polysilicon layer was removed by plasma etcher.

(x) Control gate and doping

The same process as floating gate forming.

(xi) Poly 2 mask and cleaning

The control gate was defined using poly 2 mask and photoresist was stripped by plasma. The unnecessary part of oxide layer was etched by dipping in the solution of $10H_2O$:1HF for 3 min.

(xii) Drain-source implantation.

Arsenic ions of 180 KeV and $5.0x10^{15}$ ion/cm^2 were implanted for source and drain forming. The junction depth was 0.5μm.

(xiii) Oxide layer growth and low temperature oxidation

About 500Å of oxide was grown at 925°C for 50 min in O_2. And then low temperature oxidation was done at 600°C for 10 min. in SiH_4, O_2, PH_3 and N_2. The thickness of vapox deposited was about 1μm.

(xiv) Contact cut

Oxide layer of 3000Å was grown by maintaining at 925°C for 3 min in O_2 and 5 min. in H_2O. This is to promote the uniformity of the vapox surface and to reduce the fast-surface-state charge density.[6] And then contact areas were opened by plasma etching.

(xv) Backside etching

On the backside of wafer, there are many layers formed during the process described hitherto. To remove these layers, after the front side coated with PR plasma is used for backside etching.

(xvi) Metal evaporation

To improve the step coverage conditions at the edges of contact cuts, samples were maintained at 1,000°C for 3 min. in N_2 and O_2, and $POCl_3$ predeposited for 5 min. in N_2 as carrier. And thermally treated for 2 min. in N_2. The oxide layer formed during the process was etched and about 1 μm thickness

of 1.0% Si contained Al was evaporated on the samples which is maintained at the temperature of 210°C. The sheet resistance of evaporated Al was 26-28 x 10^{-3} Ω/□.

(xii) Metal delineation

Al was etched in the solution of $16H_3PO_4$: $1HNO_3$:$1CH_3COOH$:$2H_2O$ for 2.5 min. to define the metal patterns 1% silicon contained could be etched away by plasma etching for 1 min.

(xiii) Metal annealing

To reduce the contact resistance between N^+ layer and metal layer, annealing at 460°C for 30 min. in H_2 was carried out.

(xix) Pad mask and passivation

To protect the chip surface against physical and chemical attacks, about 7,000Å of vapox was deposited. Pads were opened using pad mask.

Fig. 8 shows the cross sectional-views of each step for EAROM fabrication.

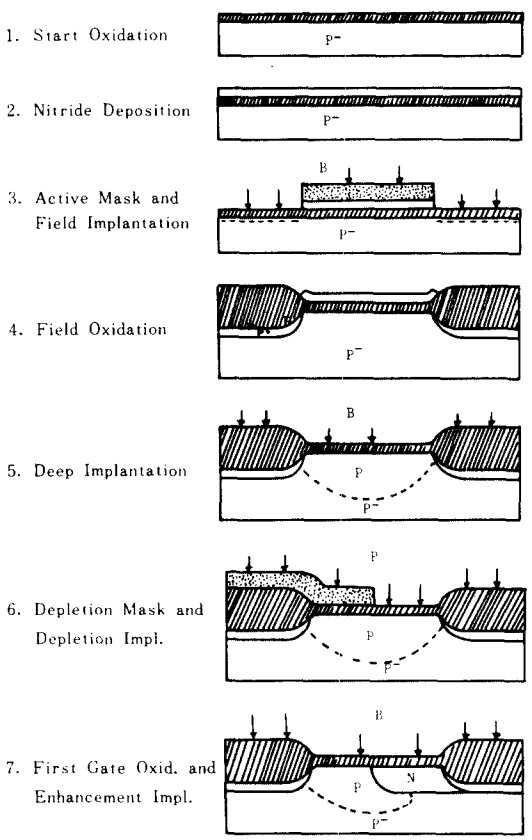
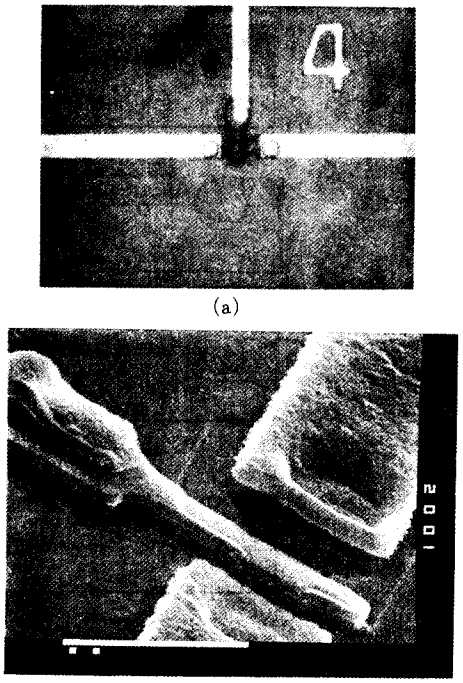


Fig. 8. Cross-sectional views of each step for EAROM fabrication.

Fig. 9 (a) is a photomicrography (x400) of the EAROM cell fabricated and 9 (b) is SEM micrograph of a device of which channel length is 4 μm. The length of shite for on the bottom of SEM microphotograph is 10 μm. The white layer in the middle part of gate shown in Fig. 9 (b) is the oxide layer between control gate and floating gate and the parts recessed on the substrate are active and depletion region.



(a)

(b)

Fig. 9. (a) Is a photomicrograph (x400) of the EAROM cell fabricated.
(b) Is SEM micrograph of a device of which channel length is μm.

IV. Measurements of Device Characteristics

Fig. 10 shows the block diagram of equipment for measuring the device characteristics. For proprammming the pulses generated at pulse counter were applied to the drain and gate of memory device through the amplifier independently. At this time the source was grounded, and the substrate was grounded or biased. And for erasing the pulses were applied to the gate under the condition of floated drain, or the source and drain connected together to the ground. The threshold voltages and I-V characteristics were measured using transistor curve tracer.

The I-V characteristics of EPROM cell before programming was shown in Fig. 11(a). And that for programming state shown in Fig.11(b). From there figures it can be seen that the device current much decreased by the programming.

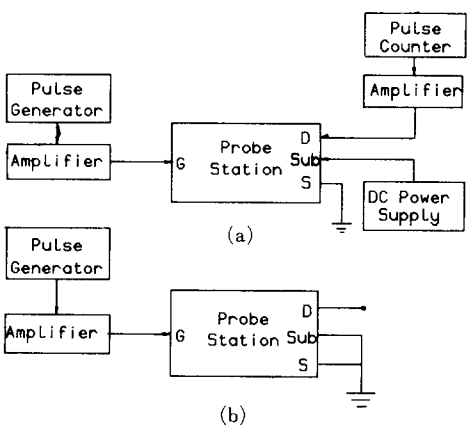


Fig. 10. EPROM cell (a) programming (b) erasing block diagram.

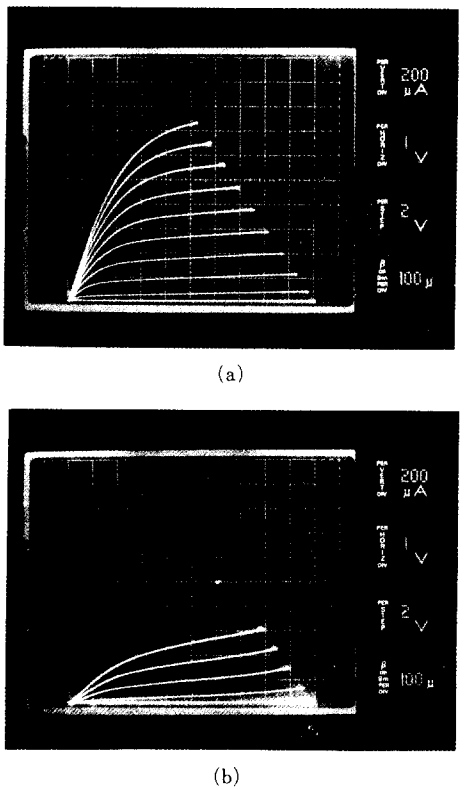
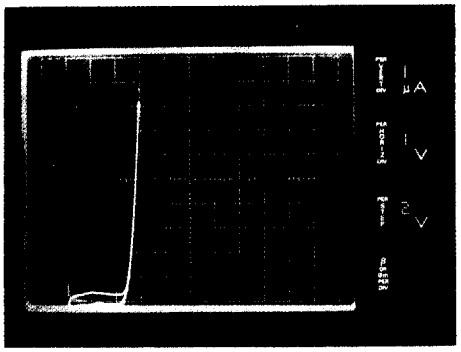
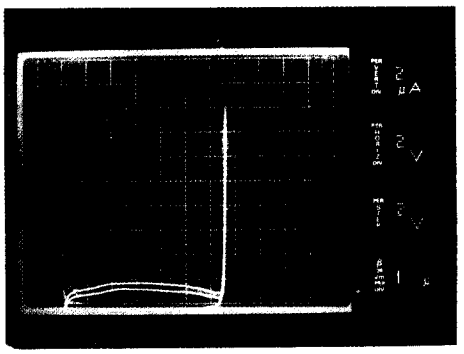


Fig. 11. I-V characteristics of EPROM cell.
(a) Before programming.
(b) After programming.

Fig. 12 (a) and (b) illustrate the threshold voltage before programming and that after programming, respectively. The threshold voltage shift is about 10.4V (2.2V-12.6V)



(a)



(b)

Fig. 12. Threshold voltage of EPROM cell.
(a) Before programming.
(b) After programming.

Fig. 13 shows the relationship between the threshold voltage and effective programming time. In this figure, it is informed that the threshold voltage would be saturated after pulse (1ms) applying time of 30-35 ms.

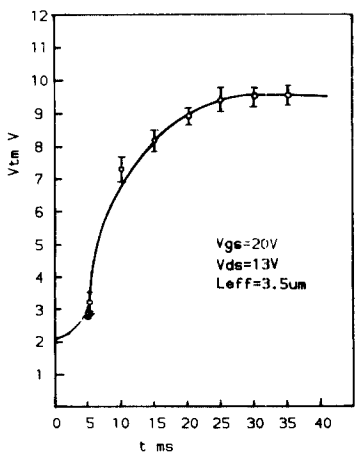


Fig. 13. Thereshold voltage vs. effective programming time.

Fig. 14 illustrates the effect of channel length on the punchthrough voltage. The punchthrough phenomena occured in the voltage range of 16-20V.

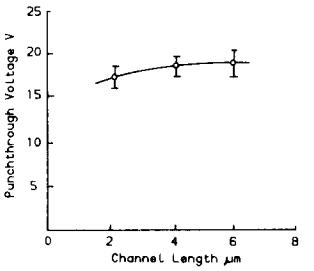


Fig. 14. Punchthrough voltage vs. channel length.

The relationship between threshold voltage of memory cell fabricated and control gate voltage was shown in Fig. 15. In this experiment 13V was applied between source and drain and 20 pulses of 5 ms were applied to the drain varying the pulse voltages to be applied to control gate. This figure says there

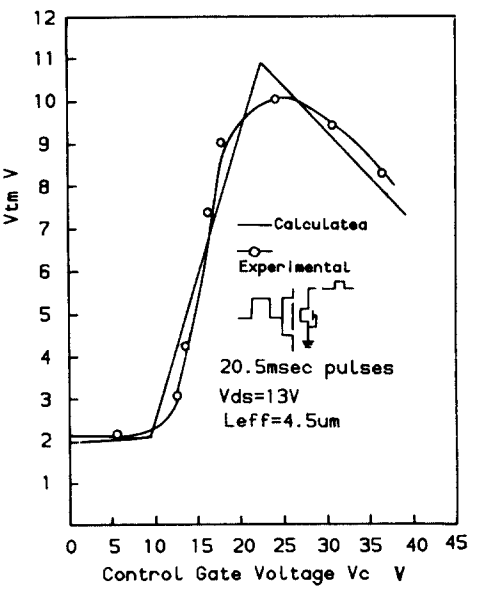


Fig.15. Saturated shift in threshold voltage of a EPROM cell versus control gate voltage.

exists maximum threshold voltage of 9.8V when gate voltage is 23V.

Fig. 16 shows the threshold voltage versus control gate voltage with effective channel length as a parameter. In this figure it is known that the programming efficiency of short channel devices is higher than long ones due to the high electric field in short channel.

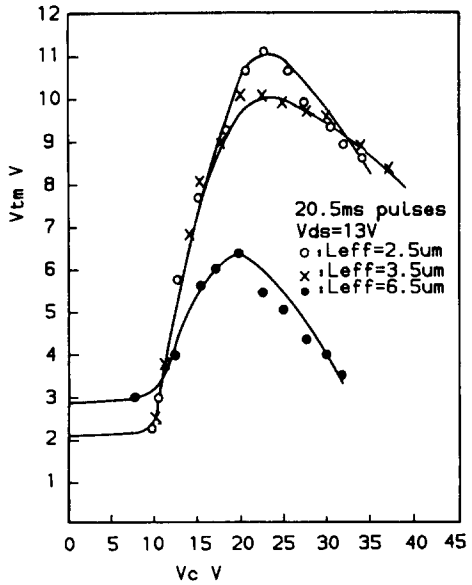


Fig.16. Threshold voltage of a EPROM cell versus control gate voltage with effective channel length as a parameter.

The control gate voltage versus threshold voltage characteristics for model C_1, C_2, C_3 and C_4 were shown in Fig. 17. This figure says model C_1 and C_3 have much higher programming efficiency than C_4.

Fig. 18 shows the effect of substrate bias. This result says the programming efficiency becomes augmented by biasing the substrate.

In order to erase the program optically, UV source (mercury lamp; 10W, 3,000Å) was used. Fig. 19 is the results of measuring the time necessary for optical erasing. The distance maintained between the wafer and lamp was about 6 cm. Although the erasing time for sample C_4 is about 14 minutes and

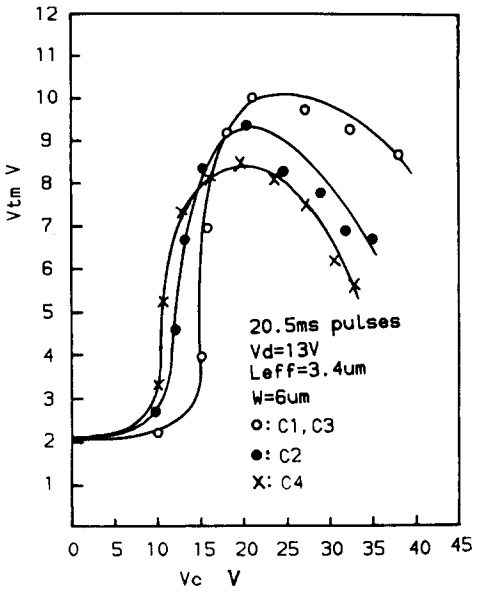


Fig17. Threshold voltage, Vtm versus control gate voltage of sample C_1, C_2, C_3 and C_4.

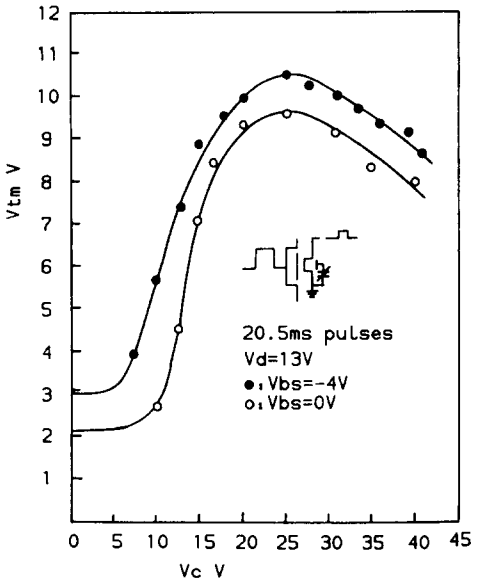


Fig.18. Thereshold voltage versus control gate voltage of EPROM with or without back bias Vbs.

that for C_2 is 20 minutes, the erasing time for C_3 is much longer. These results could be explained by the device geometry as shown in Fig. 4.

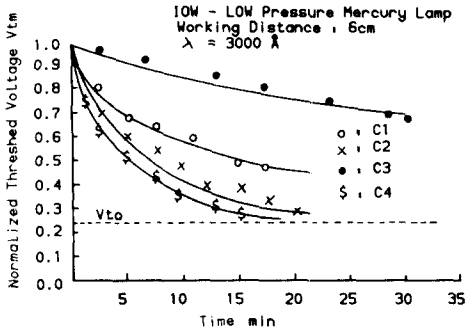


Fig.19. Threshold voltage Vtm, versus time during U V irradiation.

The electrical erasing of the program in the memory device could be also carried out by applying gate voltage as shown in Fig. 19. Regardless of the device gate configurations, the gate voltage for complete electrical erasing was in the range of 35-45V

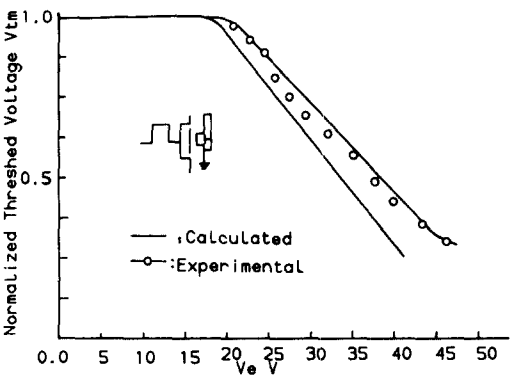


Fig.20. Threshold voltage versus gate voltage for electrical erasing.

And the test of charge retention was carried out at room temperature and 125°C under N_2 ambient. The result showed negligible change of threshold voltage even after 1,000 hours at room temperature. But the threshold voltage of device maintained at 125°C was decreased by 4% after 200 hours.

V. Conclusions

Double poly silicon gate EAROM cells which have four different gate configurations, as channel injection types were fabricated by the use of NMOS technology. The operation of programming was discussed and the process sequences for the device fabrication were described in detail. The ratio of oxide growth rate on undoped wafer, on doped poly silicon and on doped single crystal was about 1:2:3 respectively. To increase the punchthrough voltage and gate controlled channel breakdown voltage, double ion implantation technique was applied.

The drain and control gate voltage for programming was 13-17V and 20-25V, respectively. The threshold voltage shift due to programming was about 10.4V. And the memory devices fabricated could be erased by applying the voltage of 35-45 V to the control gate. The result of charge retention test showed decrease in the threshold voltage by 4% after 200 hrs. at 125°C.

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